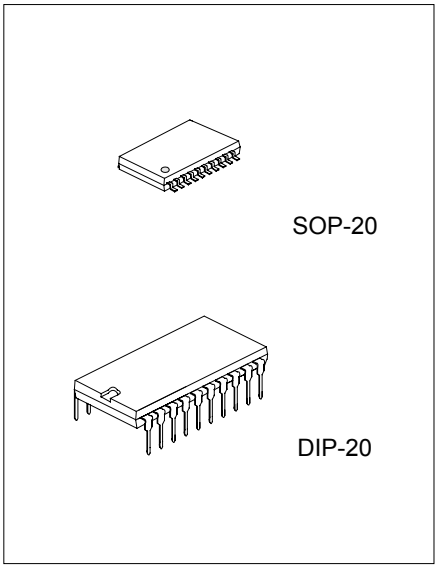
UTC 75323 LINEAR INTEGRATED CIRCUIT

MULTIPLE RS-232 DRIVERS AND RECEIVERS



DESCRIPTION

The UTC 75323 combines five drivers and three receivers. The flow-through design of the UTC 75323 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the UTC 75323 provide a rugged, low-cost solution for this function.

The UTC 75323 complies with the requirements of the ANSI TIA/EIA-232-Fand ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signal rates up to 20 Kbit/s. The switching speeds of the UTC 75323 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of ANSI Standard TIA/EIA-423-B and TIA/EIA-422-B and ITU Recommendations V.10 and V.11 are recommended.

The UTC 75323 is characterized for operation over a temperature range of 0℃ to 70℃.

FEATURES

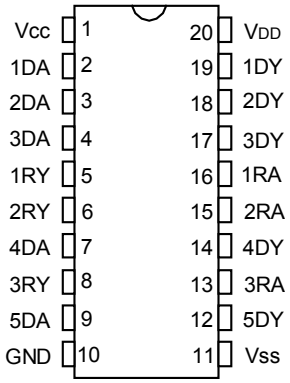
*Single Chip With Easy Interface Between UART and Serial-Port Connector of an External Modem or Other Computer Peripheral

*Five Drivers and Three Receivers Meet or Exceed the Requirements of ANSI Standard TIA/EIA-232-F and ITU Recommendation V.28 Standards.

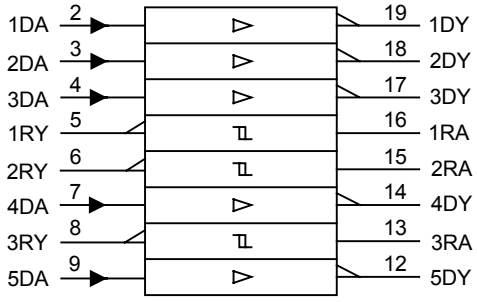
*Supports Data Rates up to 120 kbit/s.

*Complement to the UTC 75232.

PIN CONFIGURATION

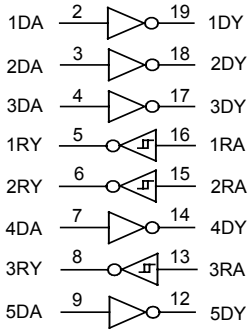


LOGIC SYMBOL *

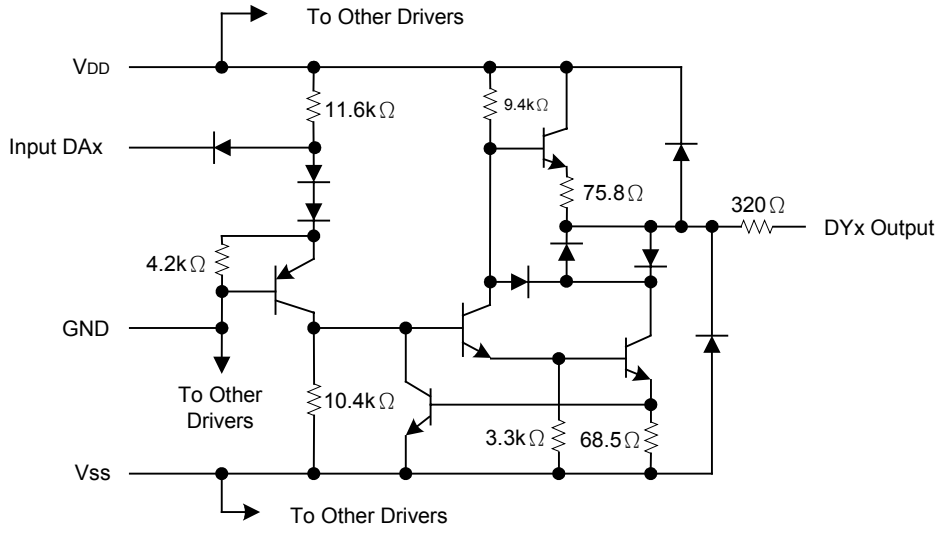


* This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)

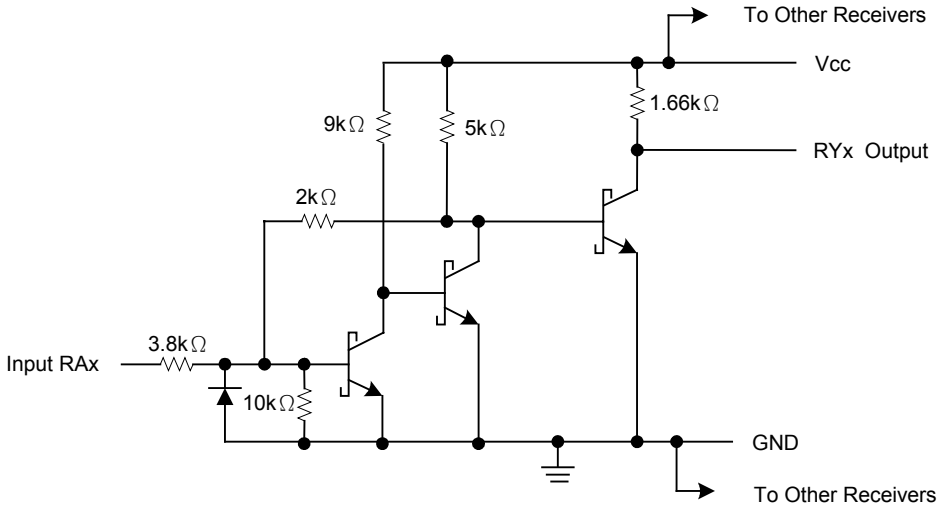


SCHEMATIC (EACH DRIVER)



Resistor values shown are nominal.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage (see Note 1)	Vcc	10	V
Supply voltage (see Note 1)	V_{DD}	15	V
Supply voltage (see Note 1)	Vss	-15	V
Input voltage range: Driver Receiver	V_I	-15 ~ 7 -30 ~ 30	V
Output voltage range, (Driver)	Vo	-15 ~ 15	V
Low-level output current (Receiver)	I_{OL}	20	mA
Package thermal impedance SOP-20 DIP-20	θ_{JA}	 97 67	°C/W
Lead temperature 1.6mm(1/6 inch) from case for 10 seconds	T_{lead}	260	°C
Storage temperature range	Tstg	-65 ~ 150	°C

note: 1. All voltages are with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{DD}	7.5	9	13.5	V
		Vss	-7.5	-9	-13.5	
		Vcc	4.5	5	5.5	
High-level input voltage	Driver	V_{IH}	1.9			V
Low-level input voltage	Driver	V_{IL}			0.8	V
High-level output current	Driver	I_{OH}			-6	mA
	Receiver				-0.5	
High-level output current,	Driver	I_{OL}			6	mA
	Receiver				16	
Operating free-air temperature		T_a	0		70	℃

SUPPLY CURRENTS OVER OPERATING FREE-AIR TEMPERATURE RANGE

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Supply current from V_{DD}	I_{DD}	All inputs at 1.9V, No load	V_{DD}=9V, Vss=-9V		25	mA
			V_{DD}=12V, Vss=-12V		32	
		All inputs at 0.8V, No load	V_{DD}=9V, Vss=-9V		7.5	mA
			V_{DD}=12V, Vss=-12V		9.5	
Supply current from Vss	Iss	All inputs at 1.9V, No load	V_{DD}=9V, Vss=-9V		-25	mA
			V_{DD}=12V, Vss=-12V		-32	
		All inputs at 0.8V, No load	V_{DD}=9V, Vss=-9V		-5.3	mA
			V_{DD}=12V, Vss=-12V		-5.3	
Suppy current from Vcc	Icc	Vcc=5V,All inputs at 5V, No load			20	mA

ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD}=9V, Vss=-9V, Vcc=5V (UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	V_{OH}	V_{IL}=0.8V, RL=3kΩ (See Figure 1)	6	7.5		V
Low-level output voltage(see Note 2)	V_{OL}	V_{IH}=1.9V, RL=3kΩ (See Figure 1)		-7.5	-6	V
High-level Input current	I_{IH}	V_I=5V (See Figure 2)			10	μA
Low-level input current	I_{IL}	V_I=0 (See Figure 2)			-1.6	mA
High-level short-circuit output current (see Note 3)	$I_{OS(H)}$	V_{IL}=0.8V, Vo=0 (See Figure 1)	-4.5	-9	-19.5	mA
Low-level short-circuit output current	$I_{OS(L)}$	V_{IH}=2V, Vo=0 (See Figure 1)	4.5	9	19	mA
Output resistance (see Note 4)	r_o	Vcc=V_{DD}=Vss=0, Vo=-2V to 2V	300			Ω

Notes: 2.The algebraic convention, where the more positive(less negative) limit is designated as maximum, is used in this data sheet for logic levels only,e.g.,if-10V is maximum, the typical value is a more negative voltage.
3.Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
4.Test conditions are those specified by TIA/EIA-232-F and as listed above.

SWITCHING CHARACTERISTICS (Ta=25℃, VDD=12V, Vss=-12V, Vcc=5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low- to high-level output	t_{PLH}	RL=3kΩ to 7kΩ, CL=15pF (See Figure 3)		315	500	ns
Propagation delay time, high-to low-level output	t_{PHL}			75	175	
TTLH Transition time, low-to high-level output	t_{TLH}	RL=3kΩ to 7kΩ, CL=15pF (See Figure 3)		60	100	ns
		RL=3kΩ to 7kΩ, CL=2500pF (See Figure 3 and Note 5)		1.7	2.5	μs
Transition time, high-to low-level output	t_{THL}	RL=3kΩ to 7kΩ, CL=15pF (See Figure 3)		40	75	ns
		RL=3kΩ to 7kΩ, CL=2500pF (See Figure 3 and Note 6)		1.5	2.5	μs

Note: 5. Measured between-3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions),all unused inputs are tied either high or low.
6. Measured between 3-V and –3-V points of the output waveform (TIA/EIA-232-F conditions),all unused inputs are tied either high or low

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP*	MAX	UNIT
Positive-going input threshold voltage	V_{IT+}	See Figure5	Ta=25℃	1.75	1.9	2.3	V
			Ta=0℃ to 70℃	1.55		2.3	
Negative-going input threshold voltage	V_{IT-}	See Figure5		0.75	0.97	1.25	
Input hysteresis voltage(V_{IT+} - V_{IT-})	Vhys			0.5			
High-level output voltage	V_{OH}	I_{OH}=-0.5mA	V_{IH}=0.75V	2.6	4	5	V
			Inputs open	2.6			
Low-level output voltage	V_{OL}	I_{OL}=10mA, V_I=3V			0.2	0.45	V
High-level input current	I_{IH}	V_I=25V.		3.6		8.3	dB
		V_I=3V		0.43			mA
Low-level input current	I_{IL}	V_I=-25V		-3.6		-8.3	mA
		V_I=-3V		-0.43			mA
Short-circuit output current	Ios	See Figure 4			-3.4	-12	mA

* All typical values are at Ta=25℃, Vcc=5V, V_{DD}=9V, Vss=-9V

SWITCHING CHARACTERISTICS (Ta=25℃,VCC=5V,VDD=12V,VSS= -12V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low-to high-level output	t_{PLH}	CL=50pF,RL=5kΩ		107	500	ns
Propagation delay time, high- to low-level output	t_{PHL}	See Figure 6		42	150	ns
Transition time, low-to high-level output	t_{TLH}			175	525	ns
Transition time, high- to low-level output	t_{THL}			16	60	ns

PARAMETER MEASUREMENT INFORMATION

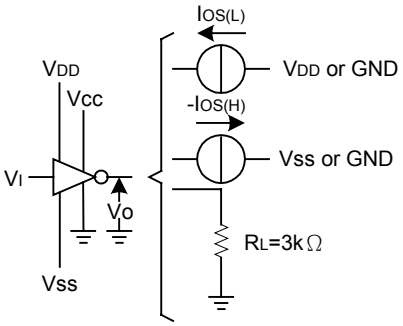


Figure 1. Driver Test Circuit for V_{OH},V_{OL},$I_{OS(H)}$,and $I_{OS(L)}$

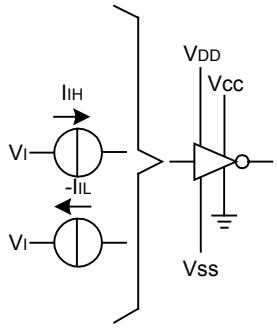
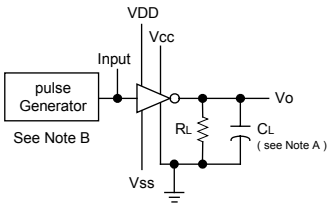
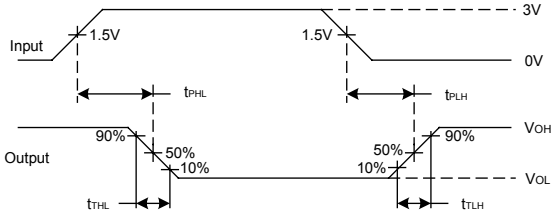


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics(t_w=25μs,PRR=20kHz,Zo=50Ω,tr=tf<50ns)

Figure 3. Driver Test Circuit and Voltage Waveforms

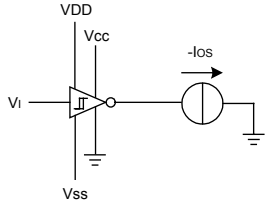


Figure 4. Receiver Test Circuit for Ios

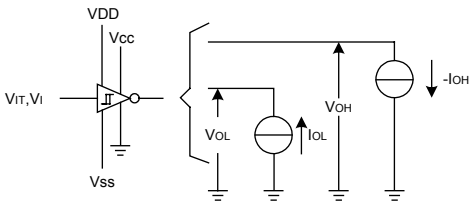
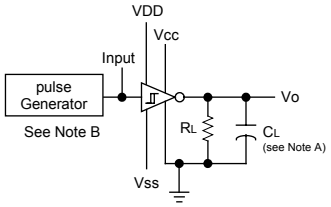
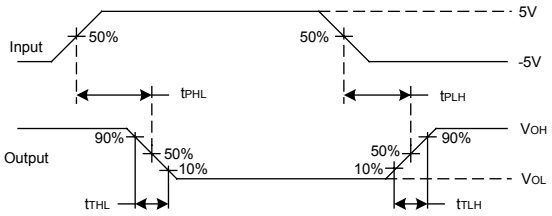


Figure 5. Receiver Test Circuit for VIT,VOH,and VOL



TEST CIRCUIT

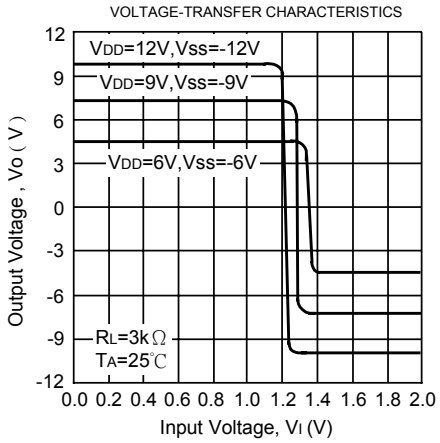


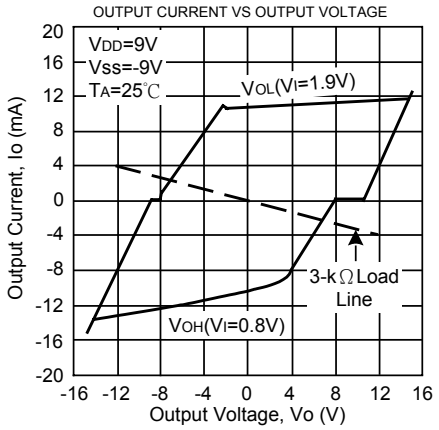
VOLTAGE WAVEFORMS

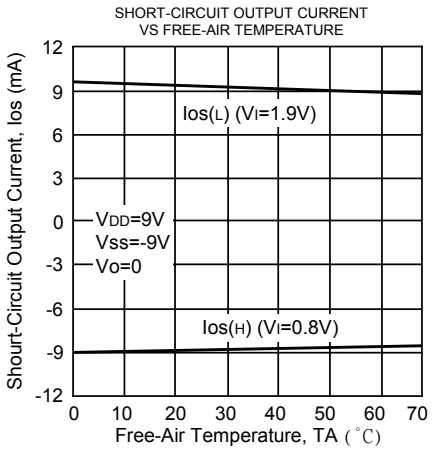
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics(t_w=25 μs,PRR=20kHz,Zo=50Ω,tr=tf<50ns)

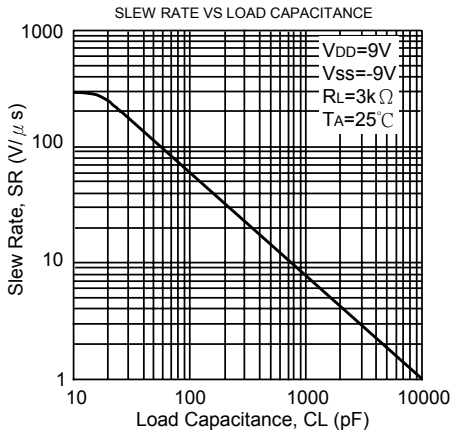
Figure 6. Receive Propagation and Transition Times

TYPICAL CHARACTERISTICS DRIVER SECTION

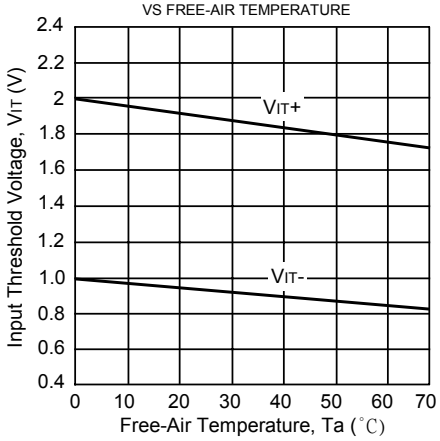




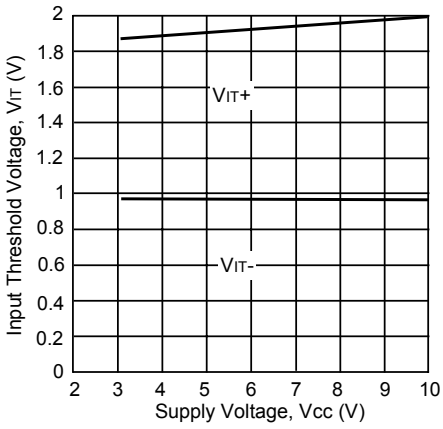




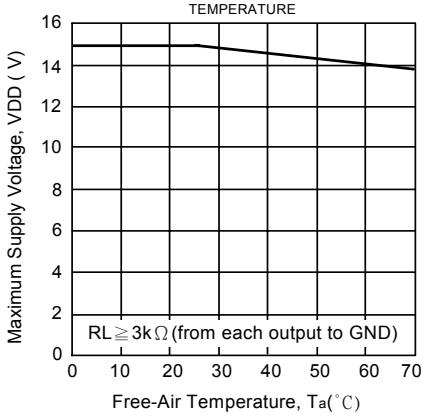
SHORT-CIRCUIT OUTPUT CURRENT VS FREE-AIR TEMPERATURE



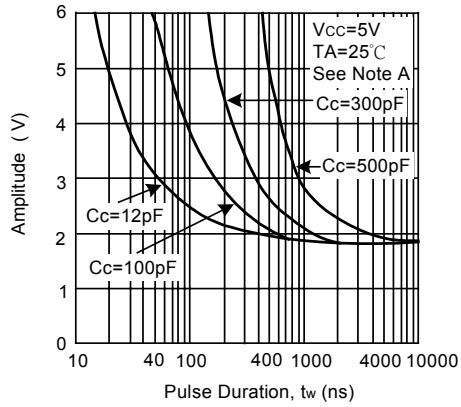
INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



MAXIMUM SUPPLY VOLTAGE VS FREE-AIR TEMPERATURE



NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0V, does not cause a change of the output level.

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and Vss leads protect the UTC GD75323 in the fault condition in which the device output are shorted to V_{DD} or Vss, and the Power supplies are at low and provide low-impedance paths to ground(see Figure 15)

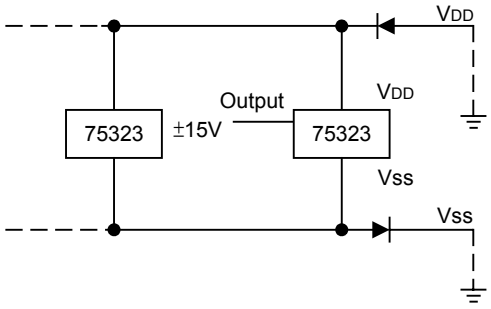
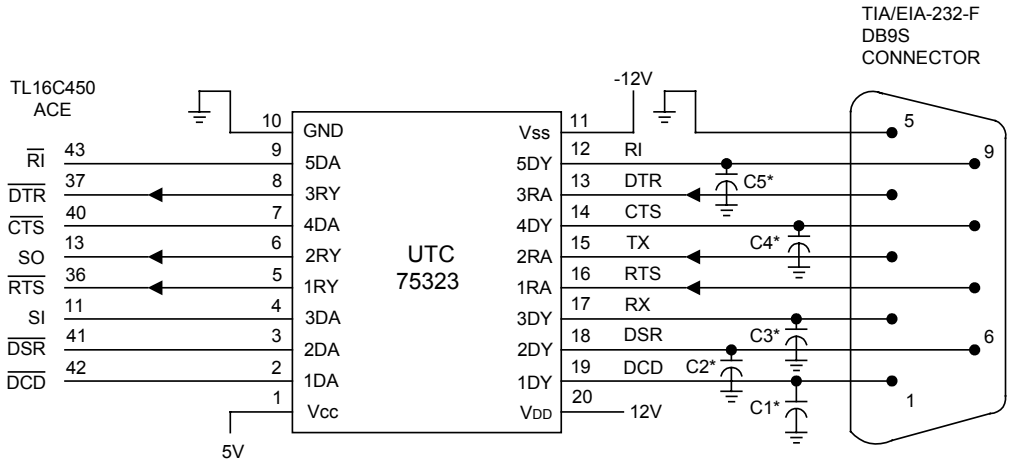


Figure 7. Power-Supply Protection to Meet Power-Off Fault Condition of TIA/EIA-232-F



*See Figure10 to select the correct values for the loading capacitors(C1,C2,C3,C4 and C5),which may be required to meet the RS-232 maximum slew-rate requirement of 30V/us.The value of the loading capacitors res required depends upon the line length and desired slew rate,but is typically 330pF.

NOTE C:To use the receivers only,V_{DD} and Vss both must be powered or tied to ground.

Figure 8. Typical Connection