

Dual P-Channel 1.8-V (G-S) MOSFET

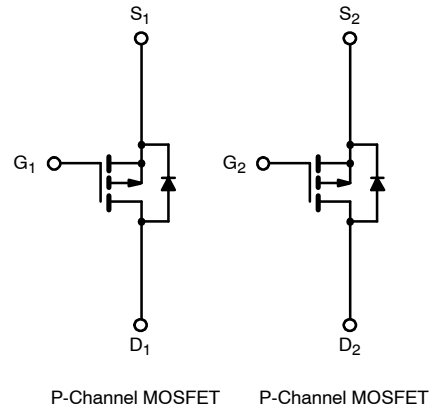
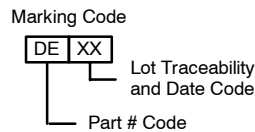
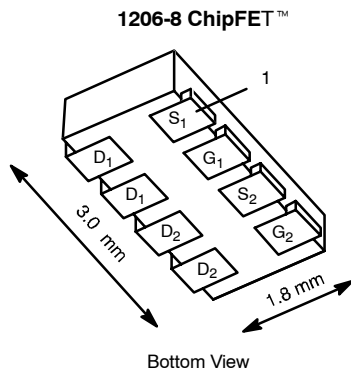
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-8	0.070 @ $V_{GS} = -4.5$ V	-4.6
	0.108 @ $V_{GS} = -2.5$ V	-3.7
	0.162 @ $V_{GS} = -1.8$ V	-3.0

FEATURES

- TrenchFET® Power MOSFET
- Low Thermal Resistance
- 40% Smaller Footprint Than TSOP-6

APPLICATIONS

- Load Switch or PA Switch for Portable Devices



Ordering Information: Si5915DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-8		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-4.6	-3.4	A
		$T_A = 85^\circ\text{C}$	-3.3	-2.5	
Pulsed Drain Current	I_{DM}	-10		A	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.8	-0.9		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.1	1.1	W
		$T_A = 85^\circ\text{C}$	1.1	0.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	50	60	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes

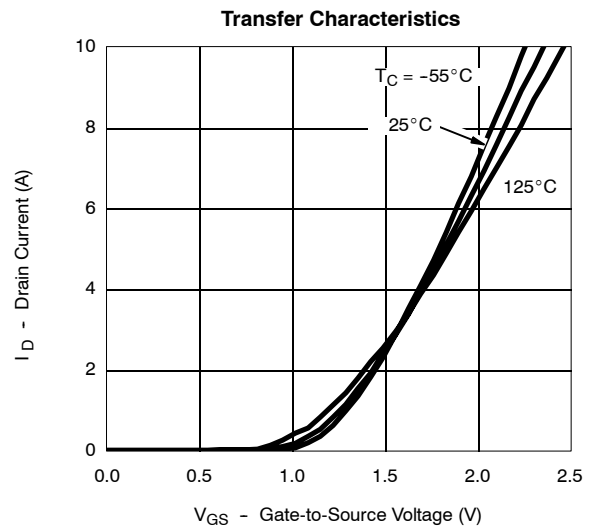
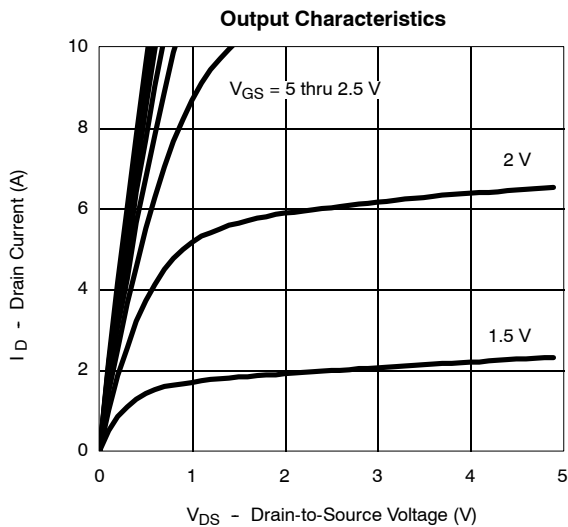
- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -6.4 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -6.4 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-10			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.4 A		0.058	0.070	Ω
		V _{GS} = -2.5 V, I _D = -2.7 A		0.090	0.108	
		V _{GS} = -1.8 V, I _D = -1 A		0.131	0.162	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -3.4 A		8		S
Diode Forward Voltage ^a	V _{SD}	I _S = -0.9 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -4 V, V _{GS} = -4.5 V, I _D = -3.4 A		5.9	9	nC
Gate-Source Charge	Q _{gs}			1.3		
Gate-Drain Charge	Q _{gd}			1.4		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -4 V, R _L = 4 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		20	30	ns
Rise Time	t _r			70	110	
Turn-Off Delay Time	t _{d(off)}			35	55	
Fall Time	t _f			35	55	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -0.9 A, di/dt = 100 A/μs		30	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

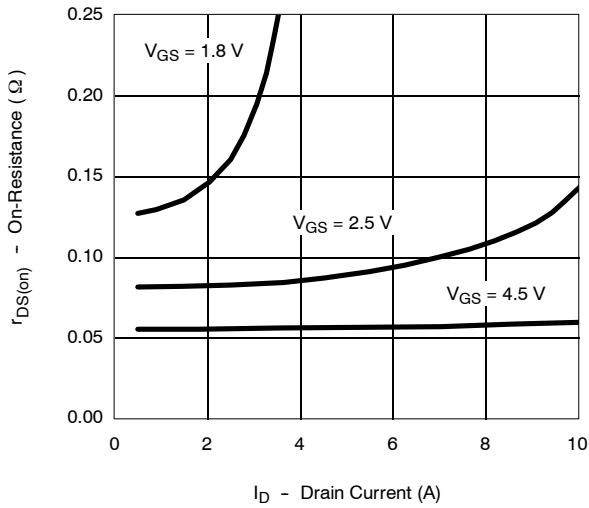
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



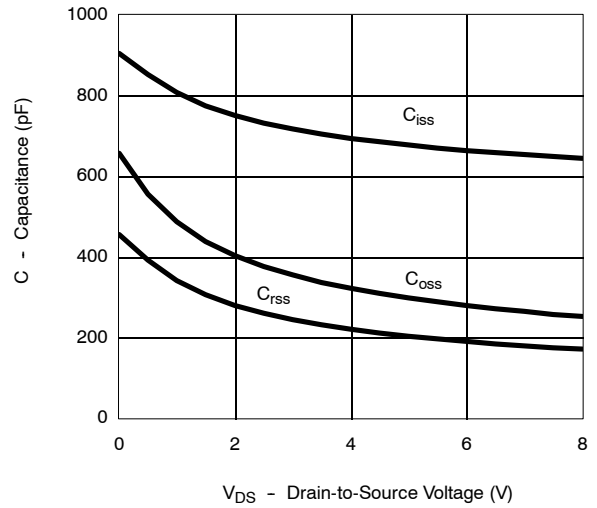


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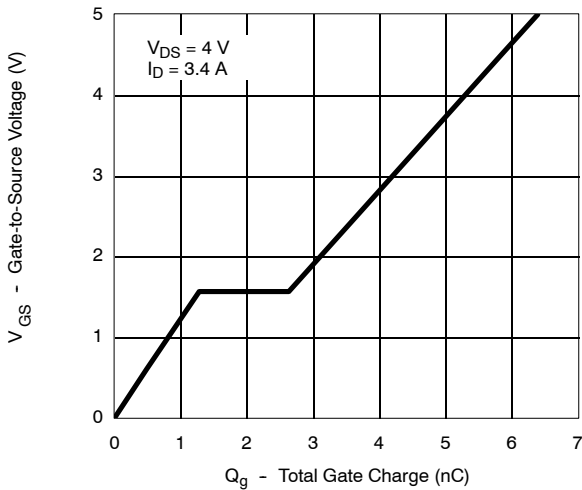
On-Resistance vs. Drain Current



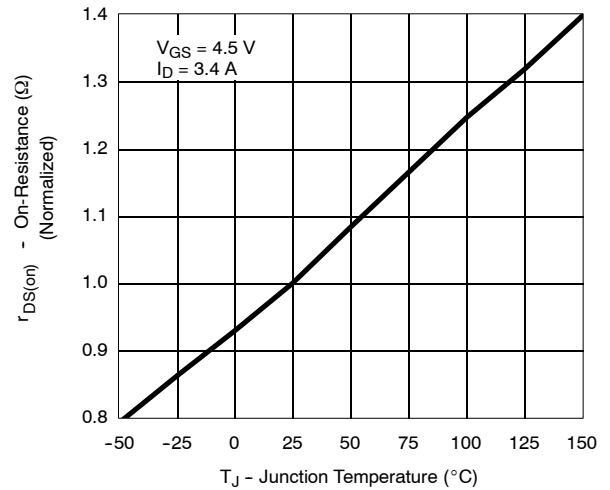
Capacitance



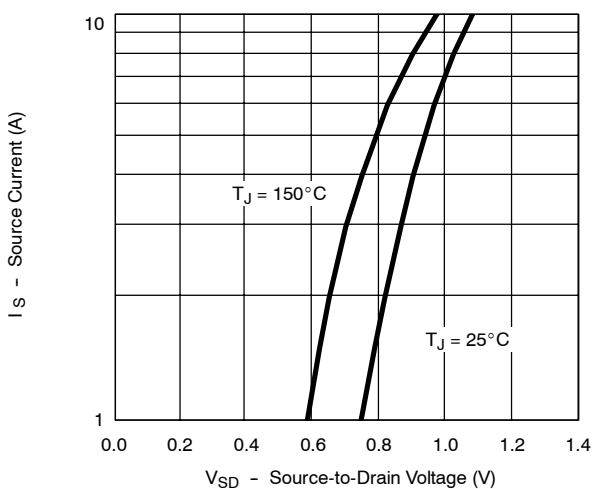
Gate Charge



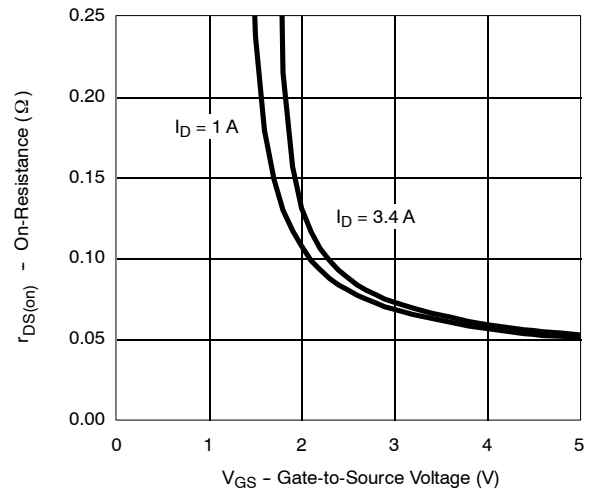
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

