OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM7602

Echo Canceler

GENERAL DESCRIPTION

The MSM7602 is an improved version of the MSM7520 with the same basic configuration. The MSM7602 uses a 19.2 MHz clock frequency to meet PHS, the 3 V power supply (2.7 V to 5.5 V), and compact packaging. Also, this device adds the howling detecter control pins and main clook output pins. (See the Appendix)
The MSM7602 is a low-power CMOS IC device for canceling echo (in an acoustic system or telephone line) generated in a speech path.
Echo is canceled, in digital signal processing, by estimating the echo path and generating a pseudo echo signal.
When used as an acoustic echo canceler, the device cancels the acoustic echo between the loud speaker and the microphone which occurs during hands free communication such as with a cellular phone or a conference system phone.
When used as a line echo canceler, the device cancels the line echo caused by impedance mismatching in a hybrid.
In addition, the MSM7602 makes possible a quality conversation by controlling the noise level and preventing howling with howling detector, double talk detector, attenuation function, and a gain control function. The devise also controls the low level noise with a center clipping function.
Further, the MSM7602 I/O interface supports μ-law PCM . The use of a single chip CODEC, such as the MSM7566/7704 (3 V) or MSM7543/7533 (5 V), allows an economic and efficient echo canceler configuration.

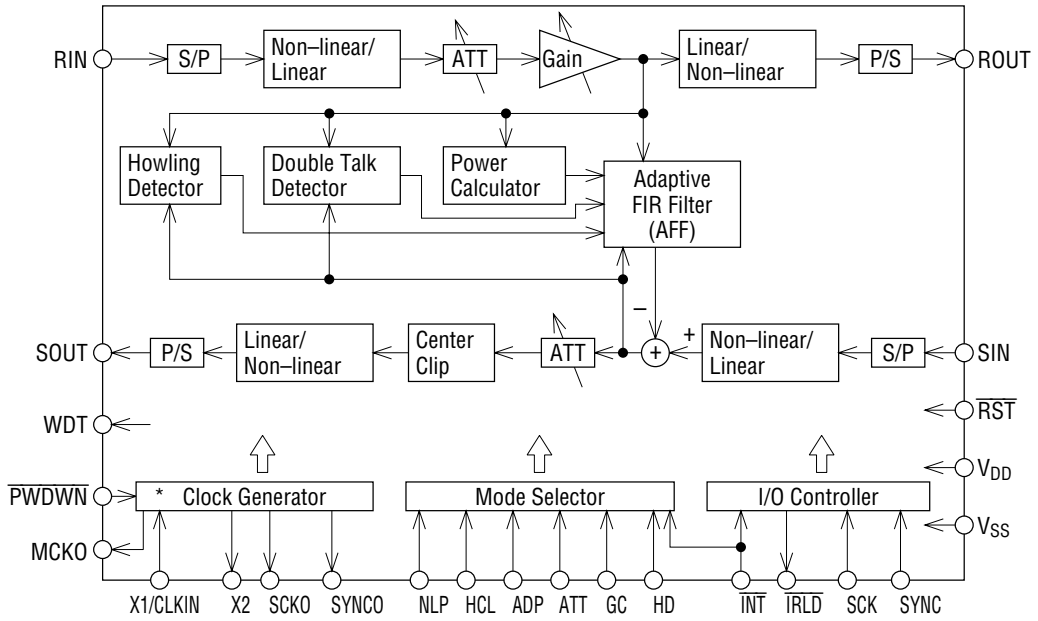
FEATURES

- Handles both acoustic echoes and telephone line echoes.
- Cancelable echo delay time:
  MSM7602-001 ..... For a single chip: 23 ms (max.)
  MSM7602-011 ..... For a cascade connection (can also be used for a single chip)
  Master chip: 23 ms (max.)
  Slave chip: 31 ms (max.)
  Cancelable up to 209 ms (1 master plus 6 slaves)
  For a single chip: 23 ms (max.)
- Echo attenuation : 30 dB (typ.)
- Clock frequency : 19.2 MHz
  External input and internal oscillator circuit are provided.
- Power supply voltage : 2.7 V to 5.5 V
- Package options:

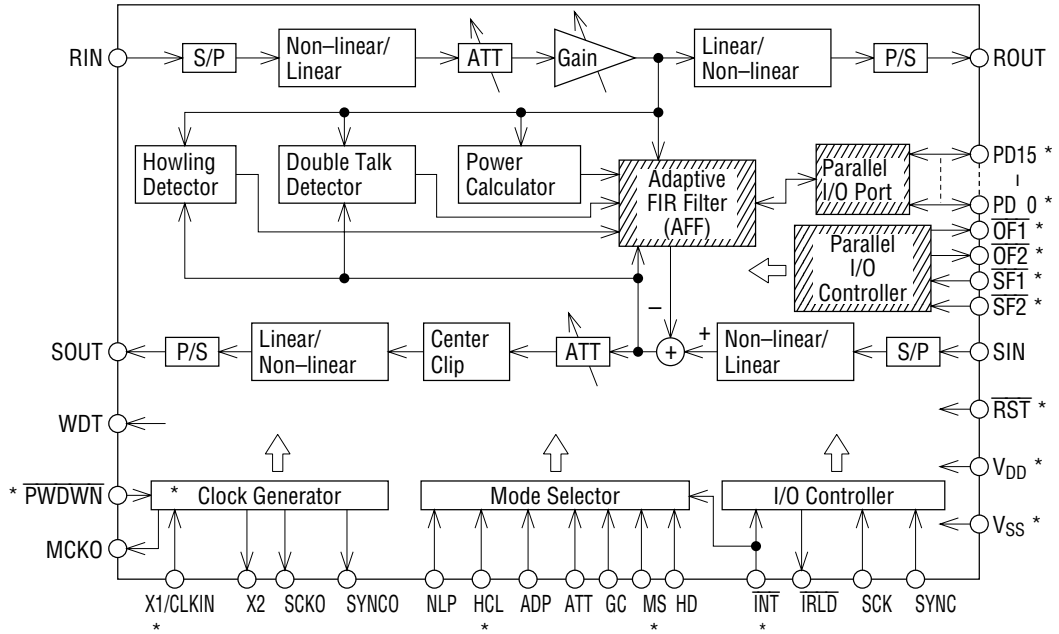
28-pin plastic SSOP	(SSOP28-P-485-0.65-K)	(Product name : MSM7602-001GS-K)
56-pin plastic QFP	(QFP56-P-910-0.65-2K)	(Product name : MSM7602-011GS-2K)

BLOCK DIAGRAM

MSM7602-001 (Single chip only)

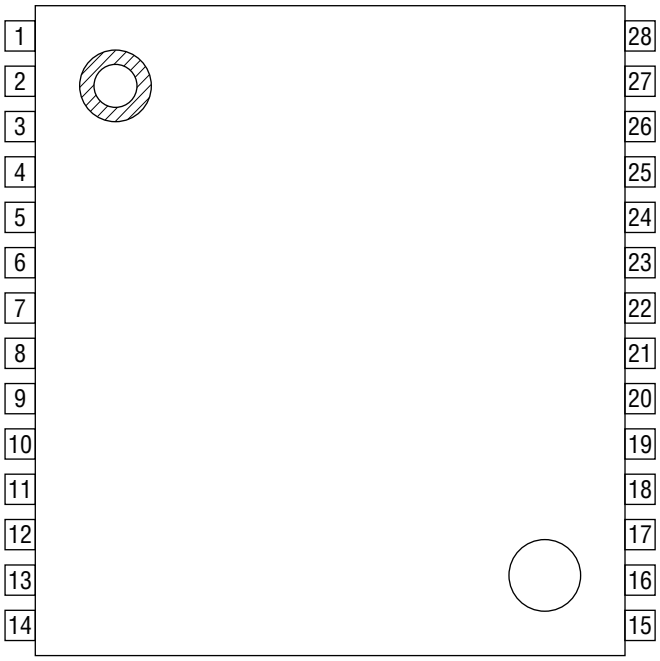


MSM7602-011 (Cascade connection or single chip)



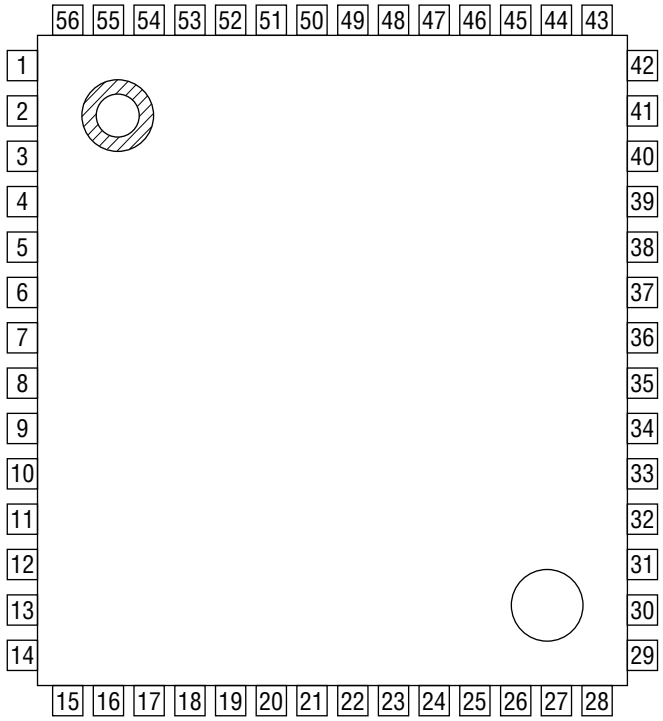
* If the MSM7602-011 is used in the slave mode, only the diagonally hatched blocks and the pins marked with * are used.

PIN CONFIGURATION (TOP VIEW)



28-Pin Plastic SSOP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NLP	8	SIN	15	V_{SS}	22	SYNCO
2	HCL	9	RIN	16	HD	23	SCKO
3	ADP	10	SCK	17	X1/CLKIN	24	$\overline{RST}$
4	V_{DD}	11	SYNC	18	X2	25	WDT
5	ATT	12	SOUT	19	V_{DD}	26	GC
6	$\overline{INT}$	13	ROUT	20	$\overline{PWDWN}$	27	V_{DD}
7	$\overline{IRLD}$	14	V_{SS}	21	V_{SS}	28	MCKO



56-Pin Plastic QFP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NLP	15	PD0	29	PD12	43	*
2	HCL	16	PD1	30	PD13	44	PD14
3	ADP	17	PD2	31	X1/CLKIN	45	PD15
4	MS	18	PD3	32	X2	46	MCKO
5	ATT	19	PD4	33	V_{DD}	47	$\overline{SF2}$
6	$\overline{INT}$	20	PD5	34	$\overline{PWDWN}$	48	$\overline{OF1}$
7	$\overline{IRLD}$	21	V_{SS}	35	V_{SS}	49	V_{SS}
8	SIN	22	PD6	36	SYNCO	50	*
9	RIN	23	PD7	37	SCKO	51	V_{SS}
10	SCK	24	PD8	38	$\overline{RST}$	52	$\overline{SF1}$
11	SYNC	25	PD9	39	WDT	53	$\overline{OF2}$
12	SOUT	26	PD10	40	GC	54	V_{DD}
13	ROUT	27	PD11	41	V_{DD}	55	V_{DD}
14	V_{SS}	28	HD	42	V_{DD}	56	*

*: No connect pin

PIN DESCRIPTIONS (1/5)

Pin		Symbol	Type	Description
28-pin SSOP	56-pin QFP			
1	1	NLP	I	Control pin for the center clipping function. This pin forces the SOUT output to a minimum value when the SOUT signal is below –54 dBm0. Effective for reducing low-level noise. • Single Chip or Master Chip in a Cascade Connection "H": Center clip ON "L": Center clip OFF • Slave Chip in a Cascade Connection Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
2	2	HCL	I	Through mode control. When this pin is in the through mode, RIN and SIN data is output to ROUT and SOUT. At the same time, the coefficient of the adaptive FIR filter is cleared. • Single Chip or Master Chip in a Cascade Connection "H": Through mode "L": Normal mode (echo canceler operates) • Slave Chip in a Cascade Connection Same as master This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
3	3	ADP	I	AFF coefficient control. This pin stops updating of the adaptive FIR filter (AFF) coefficient and sets the coefficient to a fixed value, when this pin is configured to be the coefficient fix mode. This pin is used when holding the AFF coefficient which has been once converged. • Single Chip or Master Chip in a Cascade Connection "H": Coefficient fix mode "L": Normal mode (coefficient update) • Slave Chip in a Cascade Connection Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
—	4	MS	I	Select signal. This pin selects between the master chip and slave chip when used in a cascade connection. "L": Single chip or master chip "H": Slave chip

(2/5)

Pin		Symbol	Type	Description
28-pin SSOP	56-pin QFP			
5	5	ATT	I	Control for the ATT function. This pin prevents howling by attenuators (ATT) for the RIN input and SOUT output. If there is input only to RIN, the ATT for the SOUT output is activated. If there is no input to SIN, or if there is input to both SIN and RIN, the ATT for the RIN input is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. • Single Chip or Master Chip in a Cascade Connection "H": ATT OFF "L": ATT ON "L" is recommended if performing echo cancellation. • Slave Chip in a Cascade Connection Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
6	6	$\overline{INT}$	I	Interrupt signal which starts 1 cycle (8 kHz) of the signal processing. Signal processing starts when "H"-to-"L" transition is detected. • Single Chip or Master Chip in a Cascade Connection Connect the $\overline{IRLD}$ pin. • Slave Chip in a Cascade Connection Connect the $\overline{IRLD}$ pin of the master chip. $\overline{INT}$ input is invalid for 100 μs after reset due to initialization. Refer to the control pin connection example.
7	7	$\overline{IRLD}$	O	Load detection signal output when the SIN and RIN serial input data is loaded in the internal registers. • Single Chip Connect to the $\overline{INT}$ pin. • Master Chip in a Cascade Connection Connect to the $\overline{INT}$ pin of the master chip and all the slave chips. • Slave Chip in a Cascade Connection Leave open. Refer to the control pin connection example.
8	8	SIN	I	Transmit serial data. Input the PCM signal synchronized to SYNC and SCK. Data is read in at the falling edge of SCK.
9	9	RIN	I	Receive serial data. Input the PCM signal synchronized to SYNC and SCK. Data is read at the falling edge of SCK.
10	10	SCK	I	Clock input for transmit/receive serial data. This pin uses the external SCK or the SCKO. Input the PCM CODEC transmit/receive clock (64 to 2048 kHz).

(3/5)

Pin		Symbol	Type	Description
28-pin SSOP	56-pin QFP			
11	11	SYNC	I	Sync signal for transmit/receive serial data. This pin uses the external SYNC or SYNCO. Input the PCM CODEC transmit/receive sync signal (8 kHz).
12	12	SOUT	O	Transmit serial data. Outputs the PCM signal synchronized to SYNC and SCK. This pin is in a high impedance state during no data output.
13	13	ROUT	O	Receive serial data. Outputs the PCM signal synchronized to SYNC and SCK. This pin is in a high impedance state during no data output.
— — — — — — — —	15 | 20 22 | 27 29 30 44 45	PD0 | PD5 PD6 | PD11 PD12 PD13 PD14 PD15	I/O	This is the bidirectional bus pin for parallel data transfer between the master chip and slave chip when used in a cascade connection. The PD15 pin corresponds to MSB. This pin is in a high impedance state during no data output. Data is loaded in at the falling edge of $\overline{SFx}$.
16	28	HD	I	Controls the howling detect function. This pin detets and cancels a howling generated during hand-free talking for acoustic system. This function is used to cancel acoustic echoes. • Single Chip or Master Chip in a Cascade Connection "L": Howling detector ON "H": Howling detector OFF • Slave Chip in a Cascade Connection Fixed at "L"
17	31	X1/CLKIN	I	External input for the basic clock (17.5 to 20 MHz) or for the crystal oscillator. When the internal sync signal (SYNCO, SCKO) is used, input the basic clock of 19.2 MHz.
18	32	X2	O	Crystal oscillator output. Used to configure the oscilation circuit. Refer to the internal clock generator circuit example. When inputting the basic clock externally, insert a 5 pF capacitor with excellent high frequency characteristics between X2 and GND.

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Pin		Symbol	Type	Description
28-pin SSOP	56-pin QFP			
20	34	$\overline{\text{PWDWN}}$	I	Power-down mode control when powered down. "L": Power-down mode "H": Normal operation mode During power-down mode, all input pins are disabled and output pins are in the following states : High impedance : SOUT, ROUT, PD0 to 15 "L": SYNCO, SCKO, MCKO "H": $\overline{\text{OF1}}$, $\overline{\text{OF2}}$, X2 Holds the last state : WDT, $\overline{\text{IRLD}}$ Reset after the power-down mode is released.
22	36	SYNCO	O	8 kHz sync signal for the PCM CODEC. Connect to the SYNC pin and the PCM CODEC transmit/receive sync pin. Leave it open if using an external SYNC.
23	37	SCKO	O	Transmit clock signal (256 kHz) for the PCM CODEC. Connect to the SCK pin and the PCM CODEC transmit/receive clock pin. Leave it open if using an external SCK.
24	38	$\overline{\text{RST}}$	I	Reset signal. "L": Reset mode "H": Normal operation mode Due to initialization, input signals are disabled for 100 μs after reset (after $\overline{\text{RST}}$ is returned from L to H). Input the basic clock during the reset. Output pins during the reset are in the following states : High impedance: SOUT, ROUT, PD0 to 15 "L": WDT "H": $\overline{\text{OF1}}$, $\overline{\text{OF2}}$ Not affected: X2, SYNCO, SCKO, $\overline{\text{IRLD}}$, MCKO
25	39	WDT	O	Test program end signal. This signal is output when the one cycle (8kHz) of processing is completed. Leave it open.
26	40	GC	I	Input signal by which the gain controller for the RIN input is controlled and the RIN input level is controlled and howling is prevented. The gain controller adjusts the RIN input level when it is –20 dBm0 or above. RIN input levels from –20 to –11.5 dBm0 will be suppressed to –20 dBm0 in the attenuation range from 0 to 8.5 dB. RIN input levels above –11.5 dBm0 will always be attenuated by 8.5 dB. • Single Chip or Master Chip in a Cascade Connection "H": Gain control ON "L": Gain control OFF "H" is recommended for echo cancellation. • Slave Chip in a Cascade Connection Fixed at "L" This pin is loaded in synchronization with the falling edge of the $\overline{\text{INT}}$ signal or the rising edge of $\overline{\text{RST}}$.

(5/5)

Pin		Symbol	Type	Description
28-pin SSOP	56-pin QFP			
28	46	MCKO	O	Basic clock (19.2 MHz).
—	47	$\overline{SF2}$	I	Parallel data transfer flag. • Single Chip Fixed at "H" • Master Chip in a Cascade Connection Fixed at "H" • Slave Chip in a Cascade Connection Connect $\overline{OF2}$ of the master chip to the 1st stage slave chip. Connect $\overline{OF1}$ of the previous stage slave chip to the 2nd and later stage slave chips. Refer to the control pin connection example.
—	48	$\overline{OF1}$	O	Parallel data transfer flag. • Single Chip Leave open. • Master Chip in a Cascade Connection Connect to the $\overline{SF1}$ of all slaves. • Slave chip in a Cascade Connection Connect to the $\overline{SF2}$ of the next stage slave chip. Connect the last stage slave chip to the $\overline{SF1}$ of the master chip. Refer to the control pin connection example.
—	52	$\overline{SF1}$	I	Parallel data transfer flag. • Single Chip Connect $\overline{OF2}$. • Master Chip in a Cascade Connection Connect $\overline{OF1}$ of the last stage slave chip. • Slave Chip in a Cascade Connection Connect $\overline{OF1}$ of master chip for all slave chips. Refer to the control pin connection example.
—	53	$\overline{OF2}$	O	Parallel data output flag. • Single Chip Connect to $\overline{SF1}$. • Master Chip in a Cascade Connection Connect to $\overline{SF2}$ of the 1st stage slave chip. • Slave Chip in a Cascade Connection Leave open. Refer to the control pin connection example.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D		1	W
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	3.3	3.6	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
High Level Input Voltage	V_{IH}	Pins other than X1	2.0	—	V_{DD}	V
		X1 pin	2.2	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.5	V
Operating Temperature	Ta	—	–40	+25	+85	°C

(V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.5	5	5.5	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
High Level Input Voltage	V_{IH}	Pins other than X1, SCK	2.4	—	V_{DD}	V
		X1, SCK pins	3.5	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.8	V
Operating Temperature	Ta	—	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH} = 40 µA		2.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA		0	—	0.4	V
High Level Input Current	I_{IH}	V_{IH} = V_{DD}		—	0.1	1	µA
		MS with pull-down		6	60	120	µA
Low Level Input Current	I_{IL}	V_{IL} = V_{SS}		–1	–0.1	—	µA
		$\overline{SF1}$, $\overline{SF2}$ with pull-up		–60	–33	–6	µA
High Level Output Leakage Current	I_{OZH}	V_{OH} = V_{DD}		—	0.1	1	µA
Low Level Output Leakage Current	I_{OZL}	V_{OL} = V_{SS}	PD15 to PD0 with pull-up	–60	–33	–6	µA
			Input other than the above	–1	–0.1	—	µA
Power Supply Current (Operating)	I_{DDO}	—		—	20	30	mA
Power Supply Current (Stand-by)	I_{DDS}	$\overline{PWDWN}$ = "L"		—	10	50	µA
Input Capacitance	C_I	—		—	—	15	pF
Output Load Capacitance	C_{LOAD}	—		—	—	20	pF

(V_{DD} = 4.5 V to 5.5 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH} = 40 µA		4.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA		0	—	0.4	V
High Level Input Current	I_{IH}	$V_{IH} = V_{DD}$		—	0.1	10	µA
		MS with pull-down		10	100	200	µA
Low Level Input Current	I_{IL}	$V_{IL} = V_{SS}$		–10	–0.1	—	µA
		$\overline{SF1}$, $\overline{SF2}$ with pull-up		–100	–50	–10	µA
High Level Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$		—	0.1	10	µA
Low Level Output Leakage Current	I_{OZL}	$V_{OL} = V_{SS}$	PD15 to PD0 with pull-up	–100	–50	–10	µA
			Input other than the above	–10	–0.1	—	µA
Power Supply Current (Operating)	I_{DDO}	—		—	30	45	mA
Input Capacitance	I_{DDS}	$\overline{PWDWN}$ = "L"		—	10	50	µA
Input Capacitance	C_I	—		—	—	15	pF
Output Load Capacitance	C_{LOAD}	—		—	—	20	pF

Echo Canceler Characteristics (Refer to Characteristics Diagram)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Attenuation	L_{RES}	R_{IN} = –10 dBm0 (5 kHz band white noise) E. R. L. (echo return loss) = 6 dB T_D = 20 ms ATT, GC, NLP: OFF	—	30	—	dB
Cancelable Echo Delay Time for a Single Chip or a Master Chip in a Cascade	T_D	R_{IN} = –10 dBm0 (5 kHz band white noise) E. R. L. = 6 dB ATT, GC, NLP: OFF	—	—	23	ms
Cancelable Echo Delay Time for a Slave Chip in a Cascade	T_{DS}		—	—	31	ms

AC Characteristics

(Ta = –40°C to +85°C)

Parameter	Symbol	V_{DD} = 2.7 V to 3.6 V			V_{DD} = 4.5 V to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_C	—	19.2	—	—	19.2	—	MHz
When Internal Sync Signal is not used		17.5	—	20	17.5	—	20	
Clock Cycle Time	t_{MCK}	—	52.08	—	—	52.08	—	ns
When Internal Sync Signal is not used		50	—	57.14	50	—	57.14	
Clock Duty Ratio	t_{DMC}	40	—	60	40	—	60	ns
Clock "H" Level Pulse Width fc = 19.2 MHz	t_{MCH}	20.8	—	31.3	20.8	—	31.3	ns
Clock "L" Level Pulse Width fc = 19.2 MHz	t_{MCL}	20.8	—	31.3	20.8	—	31.3	ns
Clock Rise Time	t_r	—	—	5	—	—	5	ns
Clock Fall Time	t_f	—	—	5	—	—	5	ns
Sync Clock Output Time	t_{DCM}	—	—	30	—	—	30	ns
Internal Sync Clock Frequency	f_{CO}	—	256	—	—	256	—	kHz
Internal Sync Clock Output Cycle Time	t_{CO}	—	3.9	—	—	3.9	—	µs
Internal Sync Clock Duty Ratio	t_{DCO}	—	50	—	—	50	—	%
Internal Sync Signal Output Delay Time	t_{DCC}	—	—	5	—	—	5	ns
Internal Sync Signal Period	t_{CYO}	—	125	—	—	125	—	µs
Internal Sync Signal Output Width	t_{WSO}	—	t_{CO}	—	—	t_{CO}	—	µs
Transmit/receive Operation Clock Frequency	f_{SCK}	64	—	2048	64	—	2048	kHz
Transmit/receive Sync Clock Cycle Time	t_{SCK}	0.488	—	15.6	0.488	—	15.6	µs
Transmit/receive Sync Clock Duty Ratio	t_{DSC}	40	50	60	40	50	60	%
Transmit/receive Sync Signal Period	t_{CYC}	123	125	—	123	125	—	µs
Sync Timing	t_{XS}	45	—	—	45	—	—	ns
	t_{SX}	45	—	t_{CYC}-t_{SCK}	45	—	t_{CYC}-t_{SCK}	ns
Sync Signal Width	t_{WSY}	t_{SCK}	—	—	t_{SCK}	—	—	µs
Receive Signal Setup Time	t_{DS}	45	—	—	45	—	—	ns
Receive Signal Hold Time	t_{DH}	45	—	—	45	—	—	ns
Receive Data Input Time	t_{ID}	—	7t_{SCK}	—	—	7t_{SCK}	—	µs
$\overline{IRLD}$ Signal Output Delay Time	t_{DIC}	—	—	138	—	—	138	ns
$\overline{IRLD}$ Signal Output Width	t_{WIR}	—	t_{SCK}	—	—	t_{SCK}	—	µs
Serial Output Delay Time	t_{SD}	—	—	90	—	—	90	ns
	t_{XD}	—	—	90	—	—	90	ns
Reset Signal Input Width	t_{WR}	1	—	—	1	—	—	µs
Reset Start Time	t_{DRS}	5	—	—	5	—	—	ns
Reset End Time	t_{DRE}	—	—	52	—	—	52	ns
Processing Operation Start Time	t_{DIT}	100	—	—	100	—	—	µs

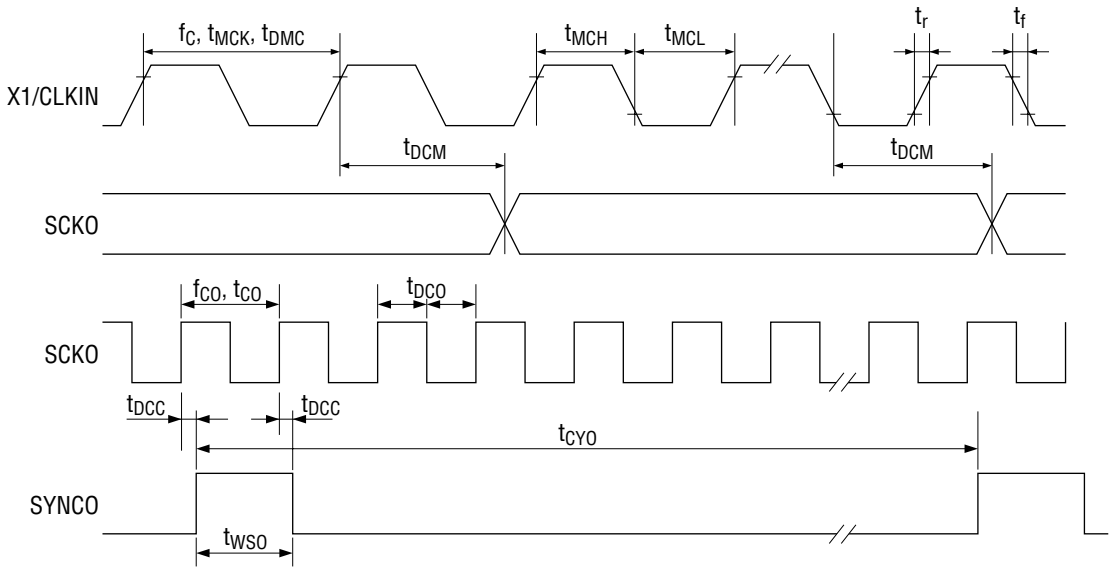
AC Characteristics (Continued)

(Ta = –40°C to +85°C)

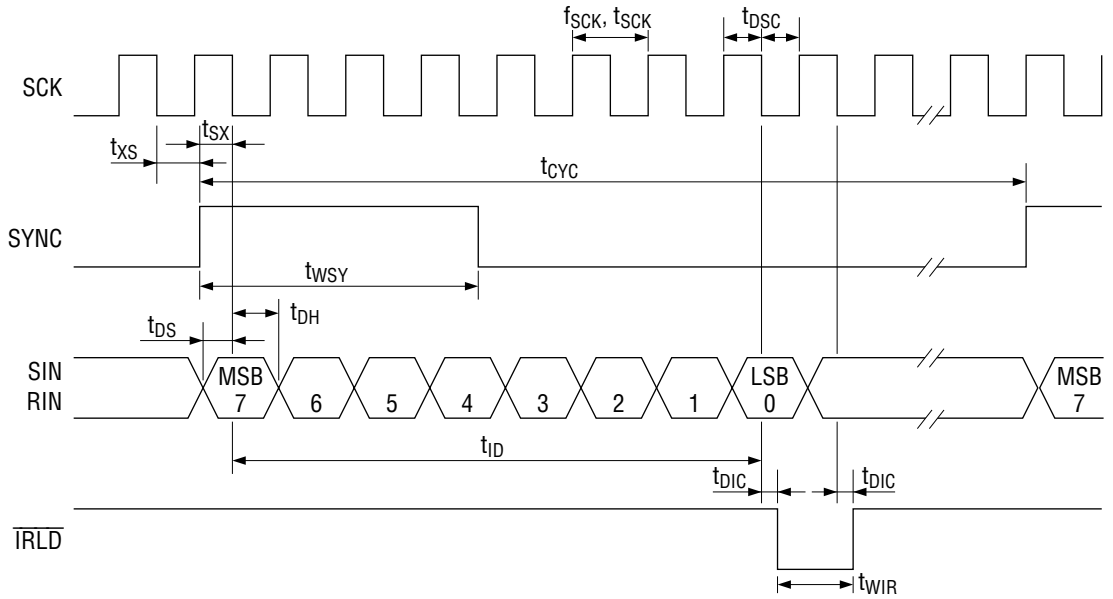
Parameter	Symbol	V_{DD} = 2.7 V to 3.6 V			V_{DD} = 4.5 V to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power Down Start Time	t_{DPS}	—	—	111	—	—	111	ns
Power Down End Time	t_{DPE}	—	—	15	—	—	15	ns
Control Pin Setup Time ($\overline{INT}$)	t_{DTS}	20	—	—	20	—	—	ns
Control Pin Hold Time ($\overline{INT}$)	t_{DTH}	120	—	—	120	—	—	ns
Control Pin Setup Time ($\overline{RST}$)	t_{DSR}	20	—	—	20	—	—	ns
Control Pin Hold Time ($\overline{RST}$)	t_{DHR}	10	—	—	10	—	—	ns
Parallel Data Output Signal Width	t_{WPD}	—	$2t_{MCK}$	—	—	$2t_{MCK}$	—	ns
Flag Signal Output Time	t_{DF}	—	t_{MCK}	—	—	t_{MCK}	—	ns
Flag Signal Output Width	t_{WFO}	—	$t_{MCK}/2$	—	—	$t_{MCK}/2$	—	ns
Flag Signal Input Width	t_{WFI}	—	t_{WFO}	—	—	t_{WFO}	—	ns
Data Read Setup Time	t_{FS}	—	20	—	—	20	—	ns
Data Read Hold Time	f_{FH}	—	10	—	—	10	—	ns

TIMING DIAGRAM

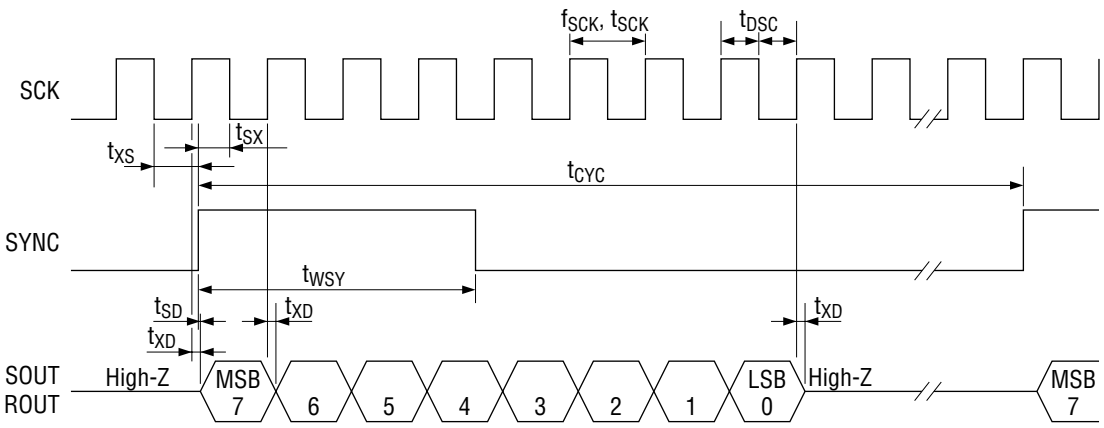
Clock Timing



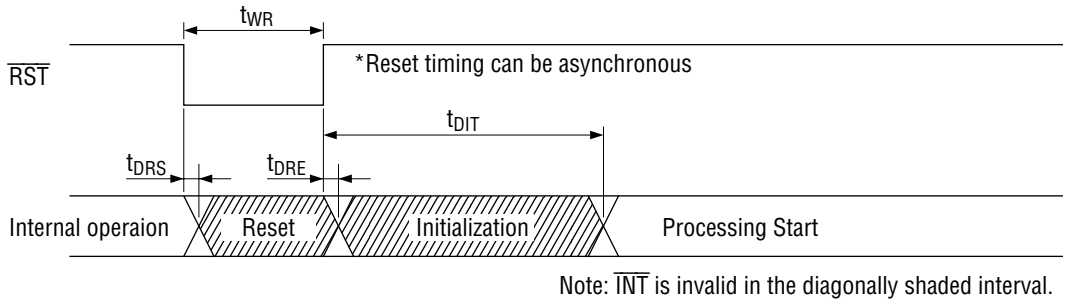
Serial Input Timing



Serial Output Timing

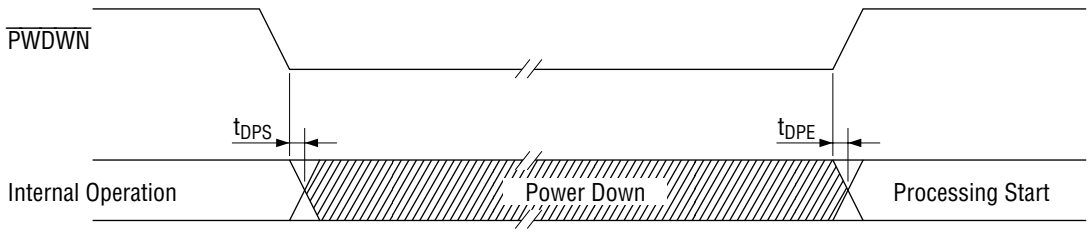


Operation Timing After Reset

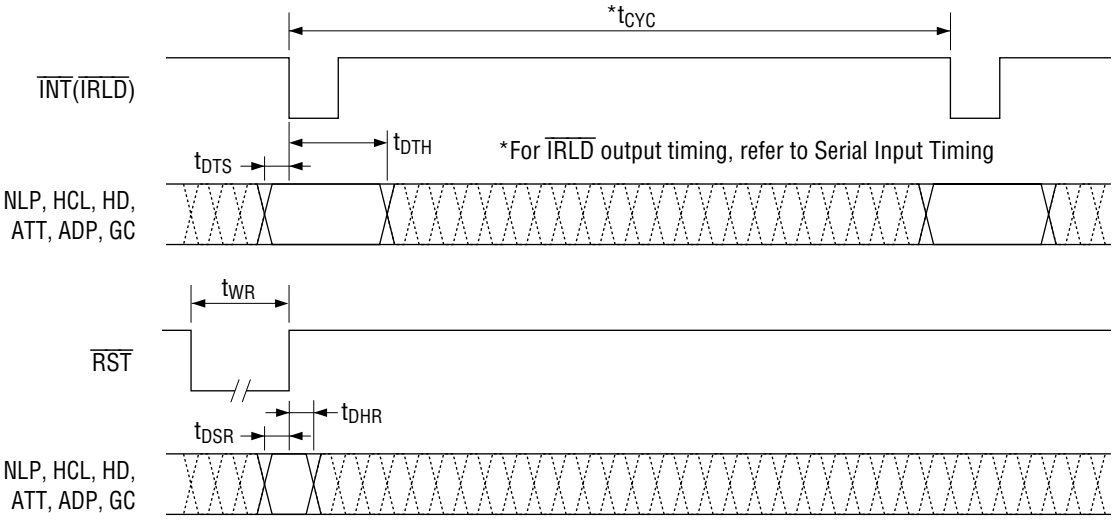


Note: $\overline{INT}$ is invalid in the diagonally shaded interval.

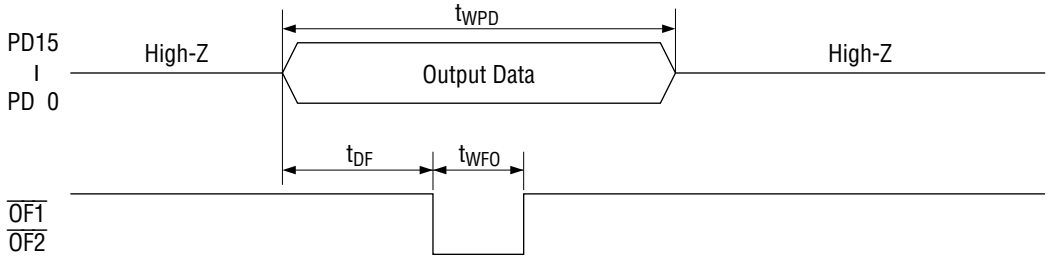
Power Down Timing



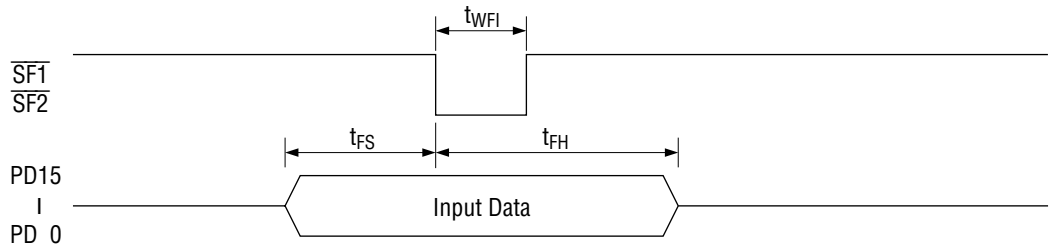
Control Pin Load-in Timing



Parallel Output Timing



Parallel Input Timing

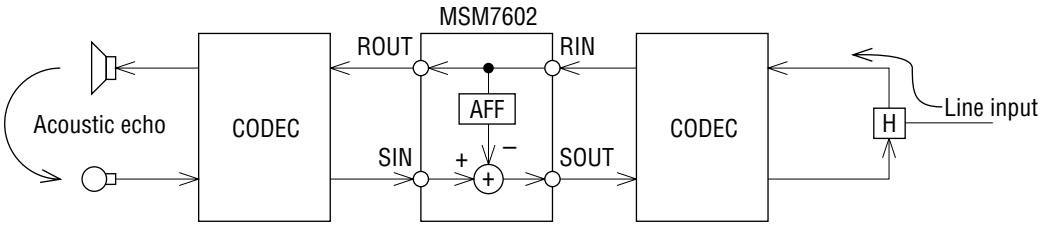


HOW TO USE THE MSM7602

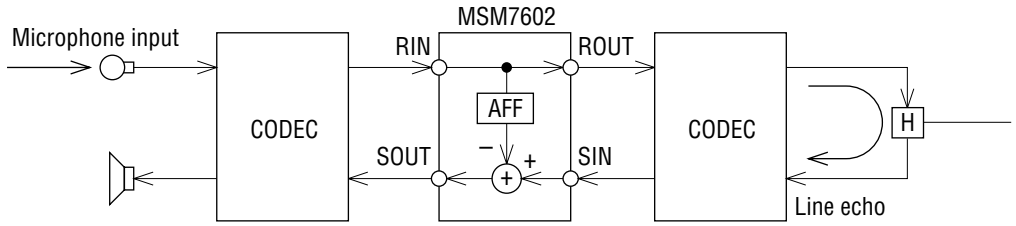
The MSM7602 cancels (based on the RIN signal) the echo which returns to SIN.
Connect the base signal to the R side and the echo generated signal to the S side.

Connection Methods According to Echos

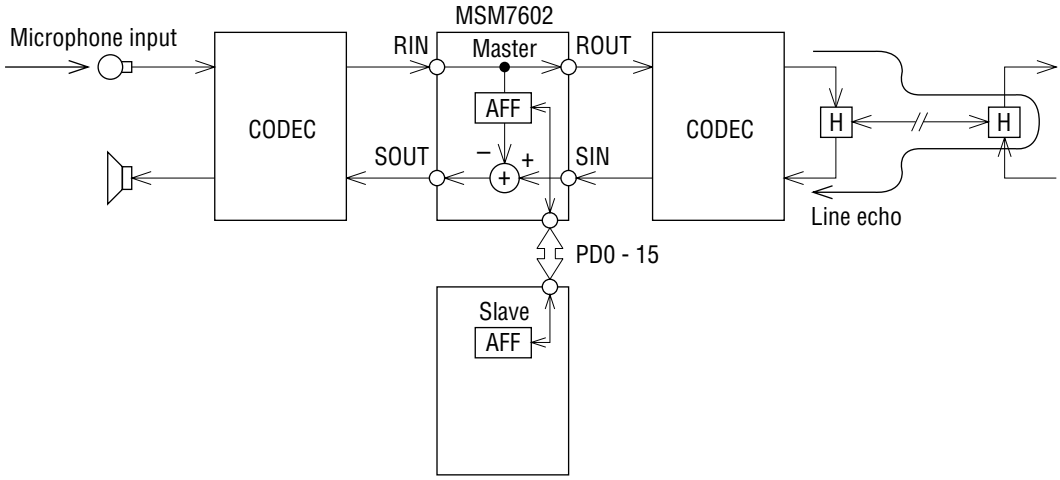
Example 1: Canceling acoustic echo (to handle acoustic echo from line input)



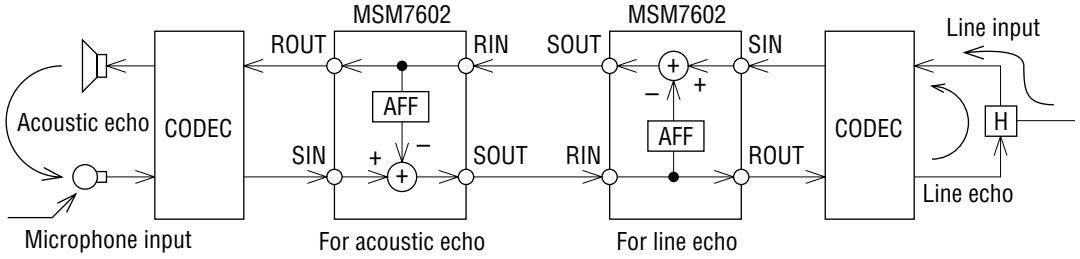
Example 2: Canceling line echo (to handle line echo from microphone input)



Example 3: Canceling line echo in a cascade connection
(to handle line echo from microphone input)

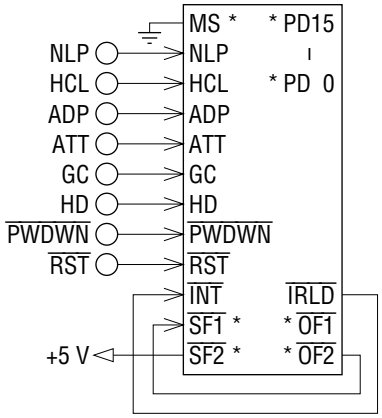


Example 4: Canceling of both acoustic echo and line echo
(to handle both acoustic echo from line input and line echo from microphone input)



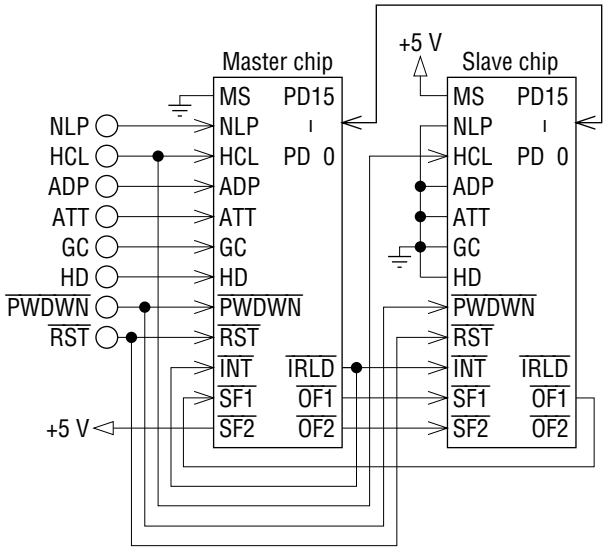
Control Pin Connection Example

Single chip connection

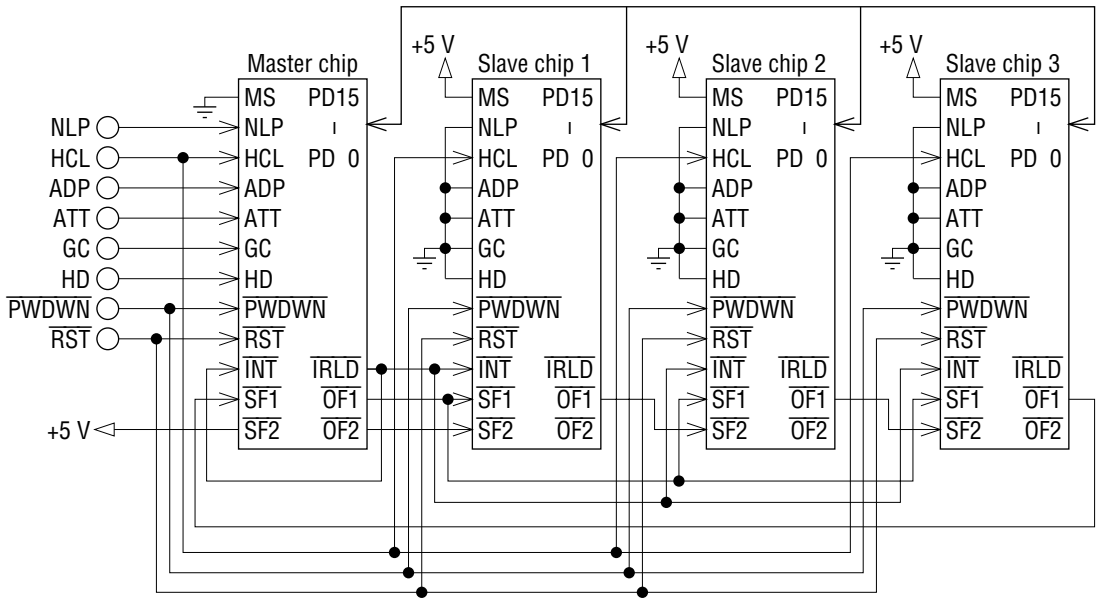


Asterisk (*) indicates a pin only for the MSM7602-011

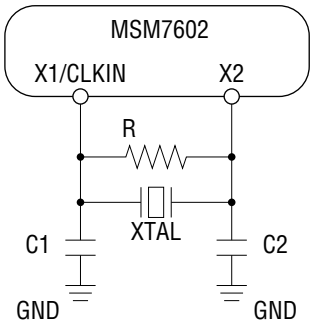
2-stage cascade connection
Master + (slave × 1)



4-stage cascade connection
Master + (slave × 3)

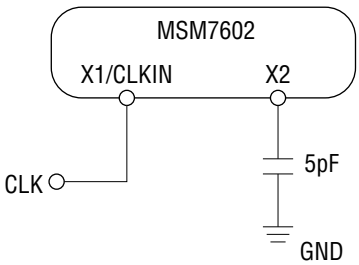


Internal Clock Generator Circuit Example



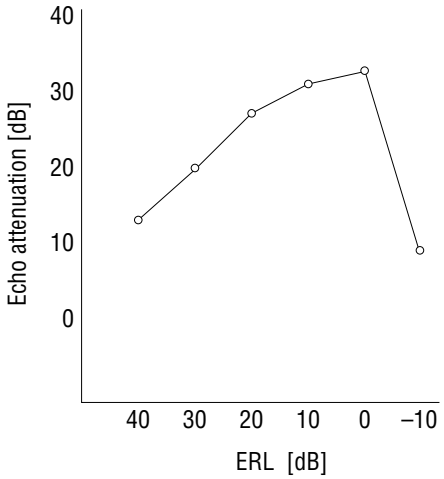
XTAL : 19.2 MHz
R : 1 MΩ
C1 : 27 pF
C2 : 27 pF

External Clock Input Circuit Example



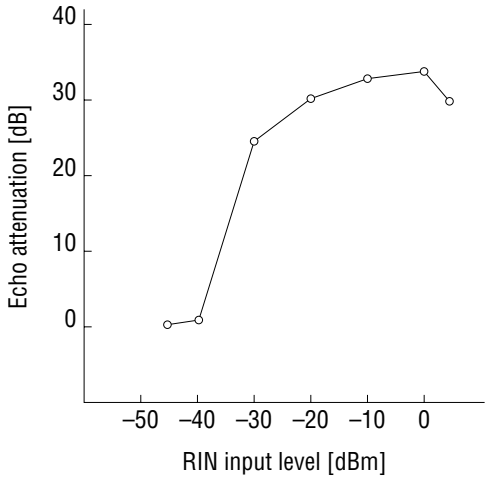
ECHO CANCELER CHARACTERISTICS DIAGRAM

ERL vs. echo attenuation



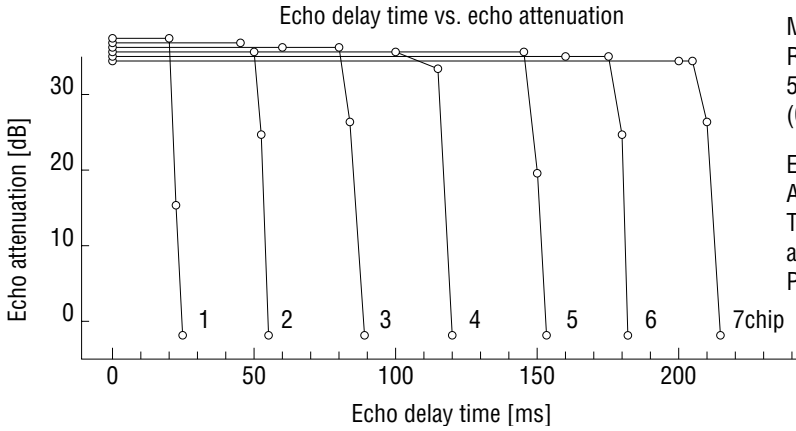
Measurement Conditions
RIN input = –10 dBm 5 kHz band white noise
(0 dBm = 2.2 dBm0)
Echo delay time T_D = 20 ms
ATT, GC, NLP = OFF
Power supply voltage 5 V

RIN input level vs. echo attenuation



Measurement Conditions
RIN input: 5 kHz band white noise
Echo delay time T_D = 20 ms
ERL = 6 dB
ATT, GC, NLP = OFF
Power supply voltage 5 V

Echo delay time vs. echo attenuation



Measurement Conditions
RIN input = –10 dBm
5 kHz band white noise
(0 dBm = 2.2 dBm0)

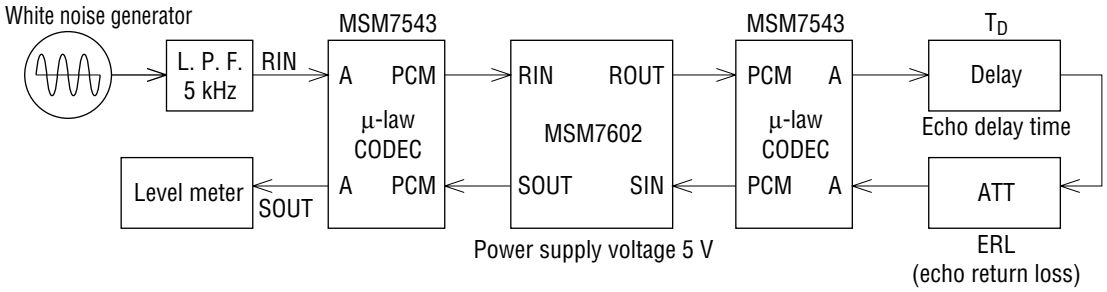
ERL = 6 dB
ATT, GC, NLP = OFF
The second through seventh chips are connected in a cascade.
Power supply voltage 5 V

Note: The characteristics above are for the MSM7543 (V_{DD} 5 V, μ-law interface). The MSM7566 (V_{DD} 3 V, μ-law interface) provides the same characleristics without input and output levels. Refer to are PCM CODEC data sheet.

MSM7543 (for both transmit and receive)
0 dBm0 = 0.6007 Vrms = –2.2 dBm (600 Ω)

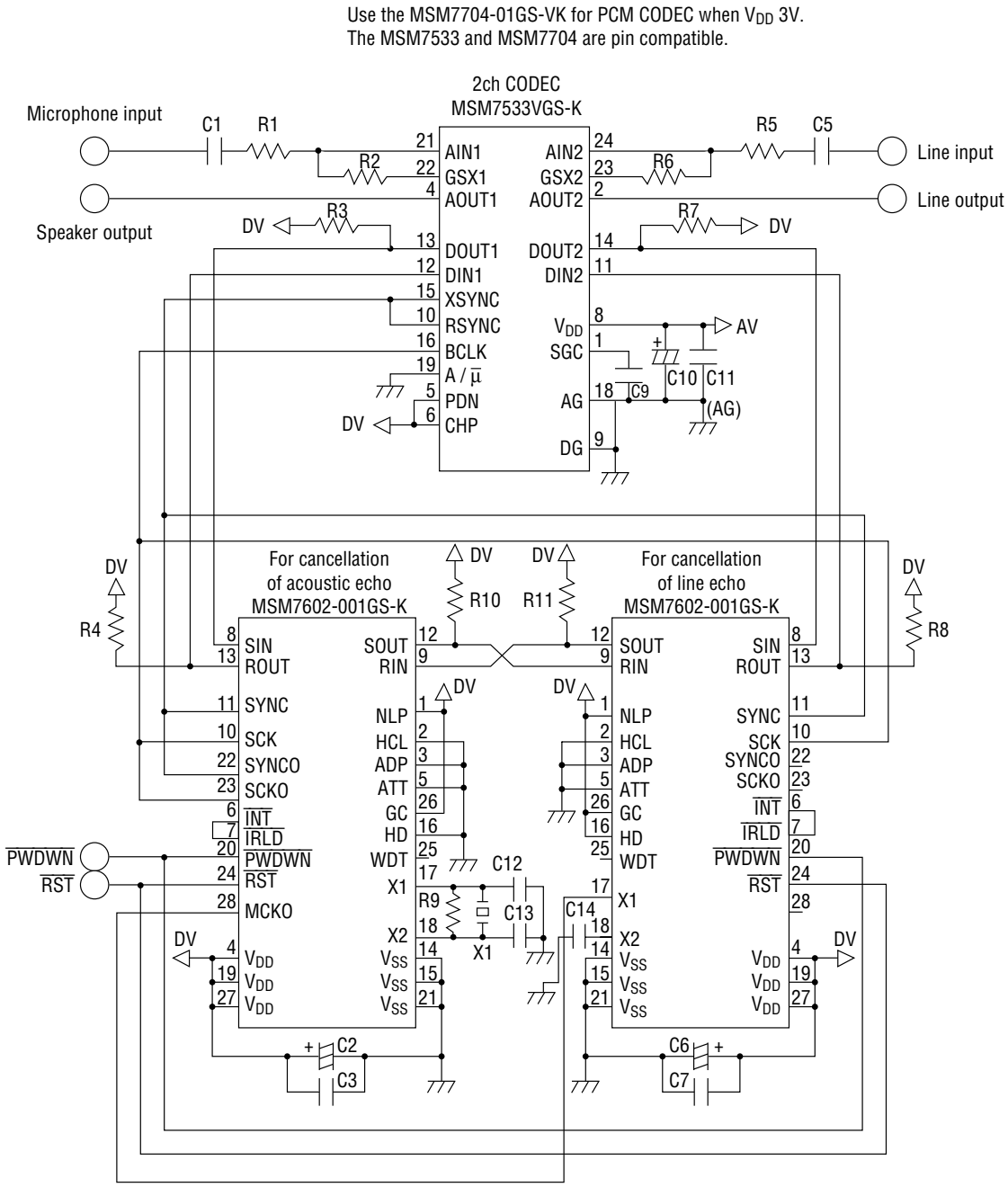
MSM7566 (for transmit side)
0 dBm0 = 0.35 Vrms = –6.9 dBm (600 Ω)
(for receive side)
0 dBm0 = 0.5 Vrms = –3.8 dBm (600 Ω)

Measurement System Block Diagram



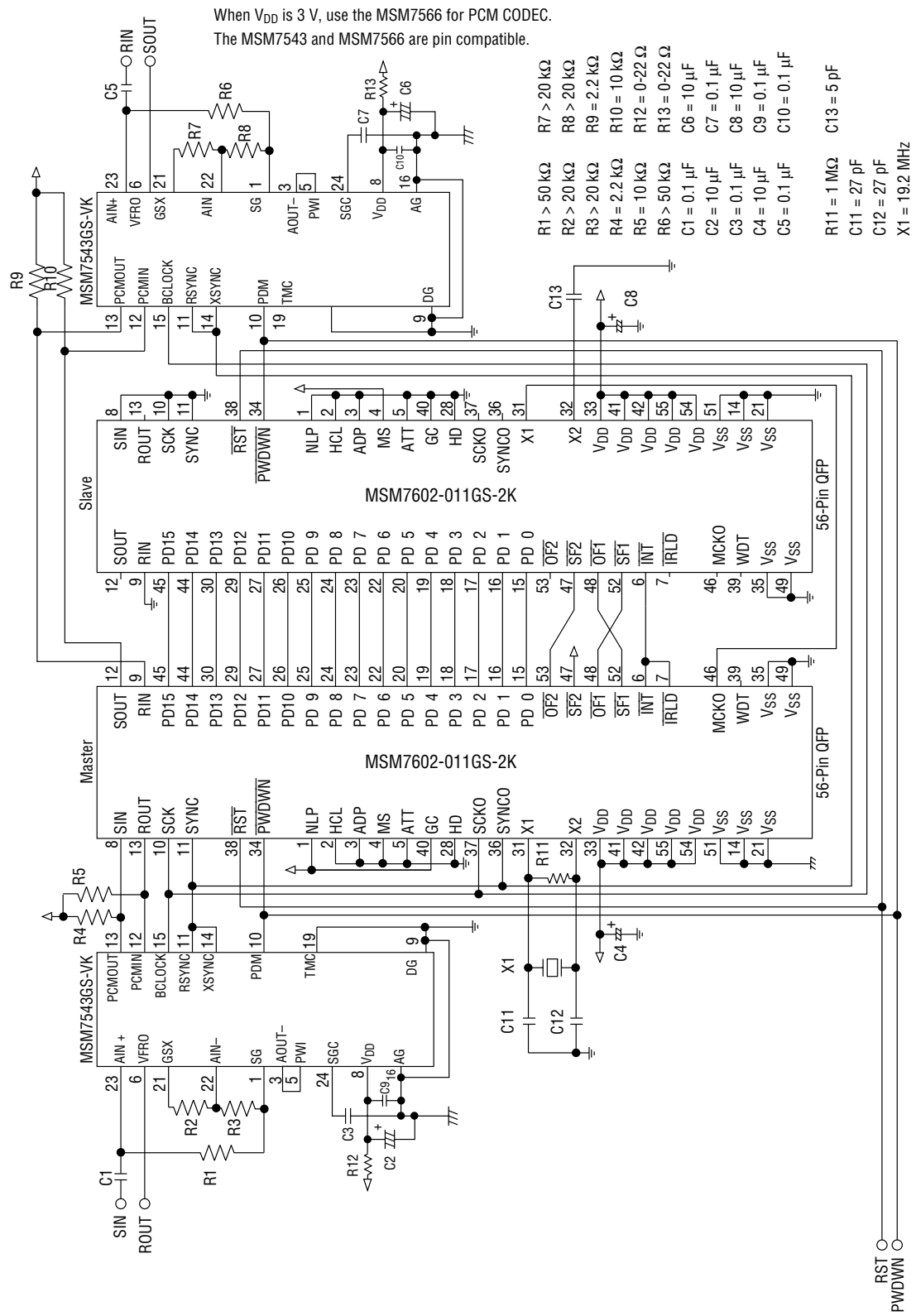
APPLICATION CIRCUIT

Bidirectional Connection Example



R1 = 20 kΩ	C1 = 1 μF	R5 = 20 kΩ	C5 = 1 μF	C9 = 0.1 μF	R9 = 1 MΩ
R2 = 20 kΩ	C2 = 10 μF	R6 = 20 kΩ	C6 = 10 μF	C10 = 10 μF	C12 = 27 pF
R3 = 2.2 kΩ	C3 = 0.1 μF	R7 = 2.2 kΩ	C7 = 0.1 μF	C11 = 0.1 μF	C13 = 27 pF
R4 = 10 kΩ	C4 = 0.1 μF	R8 = 10 kΩ	C8 = 0.1 μF		X1 = 19.2 MHz
R10 = 10 kΩ		R11 = 10 kΩ			C14 = 5 pF

Cascade Connection Example



NOTES ON USE

1. Set echo return loss (ERL) to be attenuated. If the echo return loss is set to be amplified, the echo can not be eliminated.
   Refer to the characteristics diagram for ERL vs. echo attenuation quantity.

2. Set the level of the analog input so that the PCM CODEC does not overflow.

3. The recommended input level is –10 to –20 dBm0. Refer to the characteristics diagram for the RIN input level vs. echo attenuation quantity.

4. Applying the tone signal to this echo canceler for long duration may decrease echo attenuation.
   When used with the HD pin "L" (howling detector ON), this echo canceler may operate faultily if, while a signal is input to the RIN pin, a tone signal with a higher level than the signal being input to RIN is input to the SIN pin.
   A signal should therefore be input either to the RIN pin or to the SIN pin. If, however, the tone signal is input to the SIN pin while a signal is input to the RIN pin, the ADP, HD, or HCL pin must be set to "H".

5. For changes in the echo path (retransmit, circuit switching during transmission, and so on), convergence may be difficult.
   Perform a reset, to make it converge.
   If the state of the echo path changes after a reset, convergence may again be difficult.
   In cases such as a change in the echo path, perform a reset each time.

6. When turning the power ON, set the $\overline{\text{PWDWN}}$ pin to "1" and input the basic clock simultaneously with power ON.
   If powering down immediately after power ON, be sure fast input 10 or more clocks of the basic clock.

7. After powering ON, be sure to reset.

8. After the power down mode is released (when the $\overline{\text{PWDWN}}$ pin is changed to "H" from "L"), be sure to reset the device.

9. If this canceler is used to cancel acoustic echoes, an echo attenuation may be less than 30 dB.

EXPLANATION OF TERMS

Attenuating Function :	This function prevents howling and controls the noise level with the attenuator for the RIN input and SOUT output. Refer to the explanation of pins (ATT pin).
Echo Attenuation :	If there is talking (input only to RIN) in the path of a rising echo arises, the echo attenuation refers to the difference in the echo return loss (canceled amount) when the echo canceler is not used and when it is used. Echo attenuation = (SOUT level during through mode operation) – (SOUT level during echo canceler operation) [dB]
Echo Delay Time :	This is the time from when the signal is output from ROUT until it returns to SIN as an echo.
Acoustic Echo :	When using a hands free phone, and so on, the signal output from the speaker echoes and is input again to the microphone. The return signal is referred to as acoustic echo.
Telephone Line Echo :	This is a signal which is delayed midway in a telephone line and returns as an echo, due to reasons such as a hybrid impedance mismatch.
Gain Control Function :	This function prevents howling and controls the sound level with a gain controller for the RIN input. Refer to the explanation of pins (GC pin).
Center Clipping Function :	This function forces the SOUT output to a minimum value when the signal is below –57 dBm0. Refer to the explanation of pins (NLP pin).
Double Talk Detection :	Double talk refers to a state in which the SIN and RIN signals are input simultaneously. In a double talk state, a signal outside the echo signal which is to be canceled can be input to the SIN input, resulting in misoperation. The double talk detector prevents such misoperation of the canceler.
Howling Detection :	This is the oscillating state caused by the acoustic coupling between the loud speaker and the microphone during hands free talking. Howling not only interferes with talking, but can also cause in misoperation of the echo canceler. The howling detector prevents such misoperation and prevents howling.
Echo Return Loss (ERL) :	When the signal output from ROUT returns to SIN as an echo, ERL refers to how much loss there is in the signal level during ROUT. ERL = (ROUT level) – (SIN level of the ROUT signal which returns as an echo) [dB] If ERL is positive (ROUT > SIN), the system is an attenuator system. If ERL is negative (ROUT < SIN), the system is an amplifier system.
PHS :	Personal Handy Phone System.

APPENDIX Differences Between the MSM7602 and the MSM7520/7620

Introduction

The MSM7602 is the improved version of the MSM7520 with improved usage. Thus, there are no differences in echo canceling characteristics.

Enhancements

- A new clock frequency of 19.2 MHz.
  The basic clock frequency of the MSM7520/7620 was 18 or 38 MHz, while the basic clock frequency of MSM7602 is 19.2 MHz. (MSM7602 can be applied at a frequency of 18 MHz. However, external SYNC and SCK are required because the periods of SYNCO and SCKO are varied.)

- Adoption of full-fledged 8-bit data through-mode
  In the through-mode for the MSM7520 (HCL pin: "H"), an internally processed PCM signal was used. Therefore, only the negative minimum value ($7F_{HEX}$) was converted into the corresponding positive minimum value (FF_{HEX}).
  Analog to analog conversion causes no problem since both values are the minimum ones, but data transfer in the through-mode encounters problems. Hence, in the MSM7620/7602, the complete data trough-mode has been implemented.

- Control of input timing to control pins (NLP, HCL, ADP, ATT and GC)
  In MSM7520, asynchronous changes in a control pin may result in malfunctioning. This problem stems from the fact that information on control pins is checked several times during the execution of a program over one cycle and the state of a control pin is changed between the first and second half periods.
  The MSM7620/7602 provides an internal circuit for using an INT signal to hold control pin information for one cycle. Thus, external timing control is not needed.
  The howling detector control pin (HD) is added.
  The MSM7602 can prevent the false detection of the howling detecter cause by tone signals by providing the howling detecter control pins.

- Introduction of 256 kHz internal clock output (SCKO) for PCM transmission
  Internal sync signals (SYNCO and SCKO) in MSM7520/7620 are rated at 8 kHz and 200 kHz, respectively. At a frequency of 8 kHz, PCM multiplexing can be applied to no more than three channels.
  In the MSM7602, SCKO is rated at 256 kHz, while SYNCO at 8 kHz. Thus, PCM multiplexing can be applied with up to four channels.

- Addition of basic clock output
  The use of a crystal oscillator for a clock in the MSM7520/7620 requires an oscillating circuit installed in each of two or more cascade-connected IC chips.
  Since the MSM7602 supports basic clock output, only one IC chip requires an oscillating circuit. (The MSM7602-001TS-K does not provide the basic clock output.)

- Small-sized package

MSM7602		Package code	Package size (mm)
MSM7602-001GS-K	:28-pin SSOP	:SSOP28-P-485-0.65-K	:9.5 × 10.5 × 1.85
MSM7602-011GS-2K	:56-pin QFP	:QFP56-P-910-0.65-2K	:9.5 × 10.5 × 1.85

MSM7520 : 14.0 × 14.0 × 3.75 mm
MSM7620 : 14.0 × 14.0 × 2.1 mm

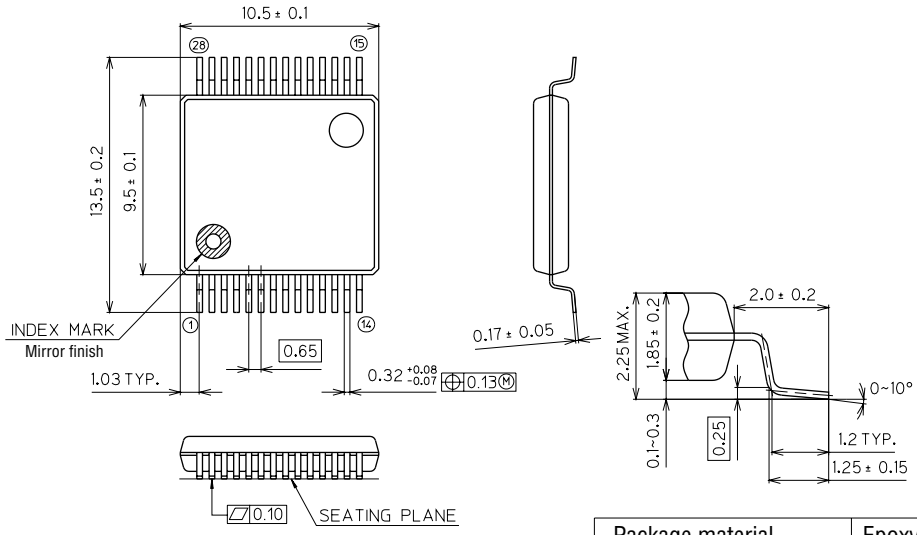
- Supply voltage rated at 3 volts

MSM7520/7620	4.5 V to 5.5 V	5 V typ.
MSM7602	2.7 V to 5.5 V	3.3 V or 5 V typ.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP28-P-485-0.65-K



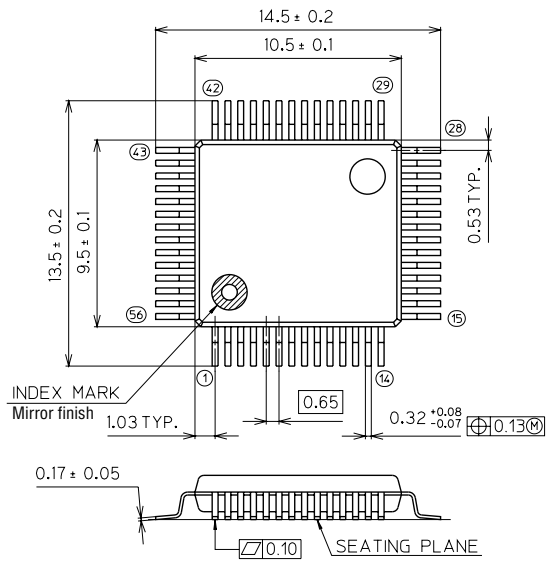
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.39 TYP.

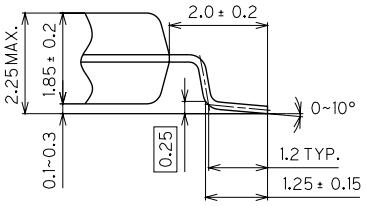
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP56-P-910-0.65-2K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).