1. GENERAL

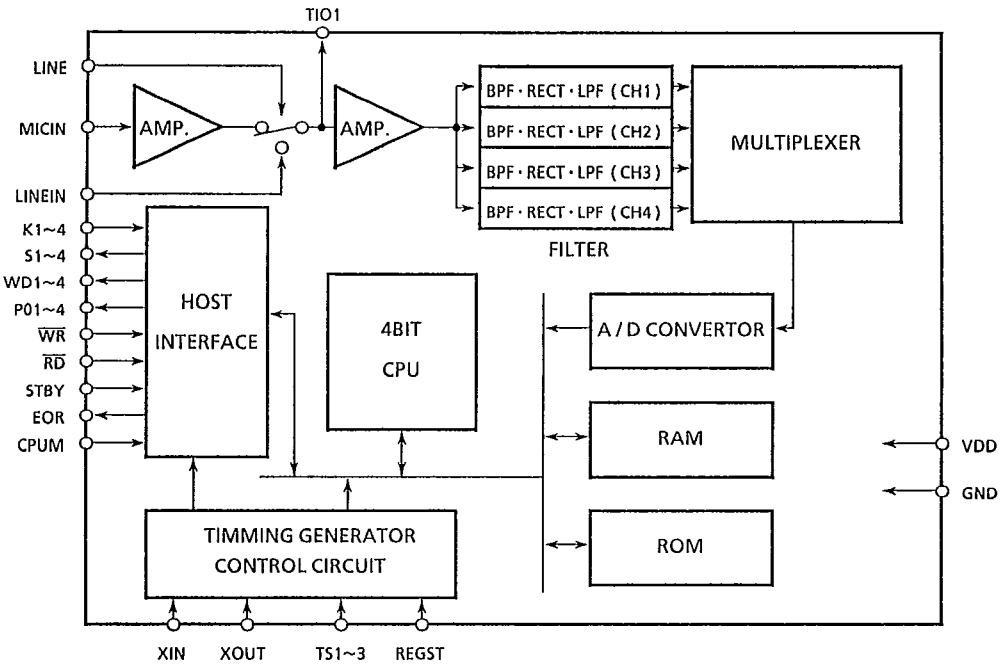
The TC8860F is a single chip LSI with on chip circuits and functions required for voice recognition including analog circuit, registration RAM, and pattern matching function. It is possible to construct a voice recognition system only by externally connecting a microphone and keyboard to this LSI.

2. FEATURES

- ☐ A single chip voice recognition LSI.
- ☐ Speaker dependent word recognition system.
- ☐ Linear matching system.
- ☐ Number of words that can be registered : Max. 10 words.
- ☐ Response time is Max. 0.60 sec, average 0.35 sec.
- ☐ Input voice time length allowed : 0.16~0.96 sec.
- ☐ Built - in 4Kbit RAM for registration.
- ☐ A microphone for voice inputting is directly connectable.
- ☐ Either the manual mode by key operation or CPU Mode using host CPU is selectable.
- ☐ Mutual data transmission between host CPU and on chip registration RAM is possible.
- ☐ Built - in 800KHz ceramic oscillation circuit.
- ☐ 5V single power supply.
- ☐ 44 pin mini flat package.

3. BLOCK DIAGRAM AND SYSTEM CONFIGRATION

3.1 TC8860F Block Diagram



3.2 Block Diagram Description

(1) Amplifer

The amplifer consists of two blocks and is selectable microphone input or line input.

(2) Filter

The filter extracts a portion of signals lying in passband of four frequency bands.

(3) RAM

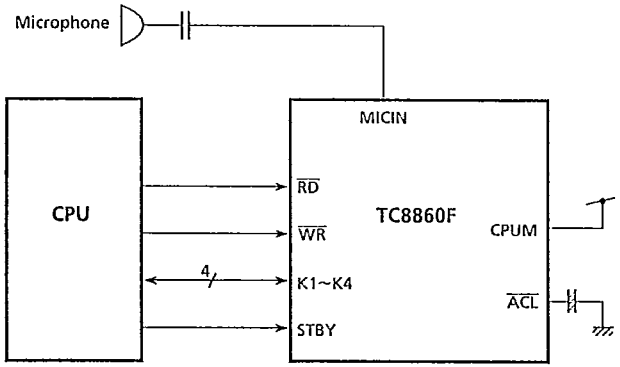
The RAM contains registration data.

(4) Host interface

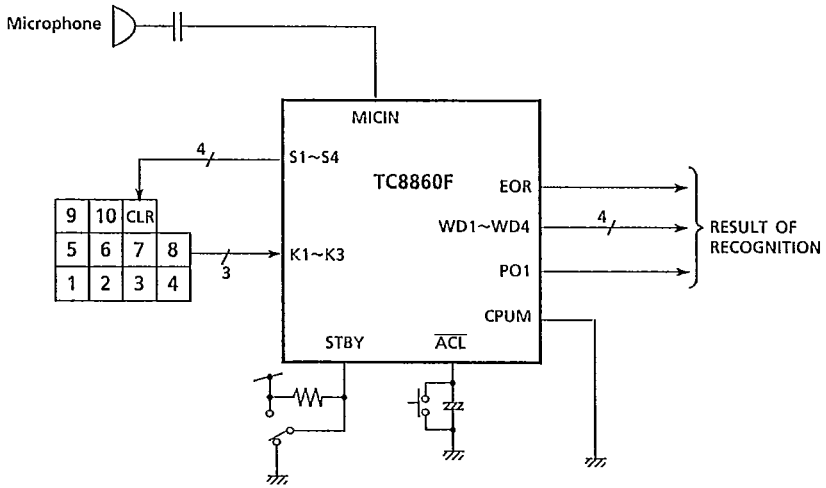
The host interface consists of external CPU interface circuit for CPU Control Mode and Key Scan Circuit for Manual Control Mode.

3.3 Example of Voice Recognition System

3.3.1 CPU Control Mode

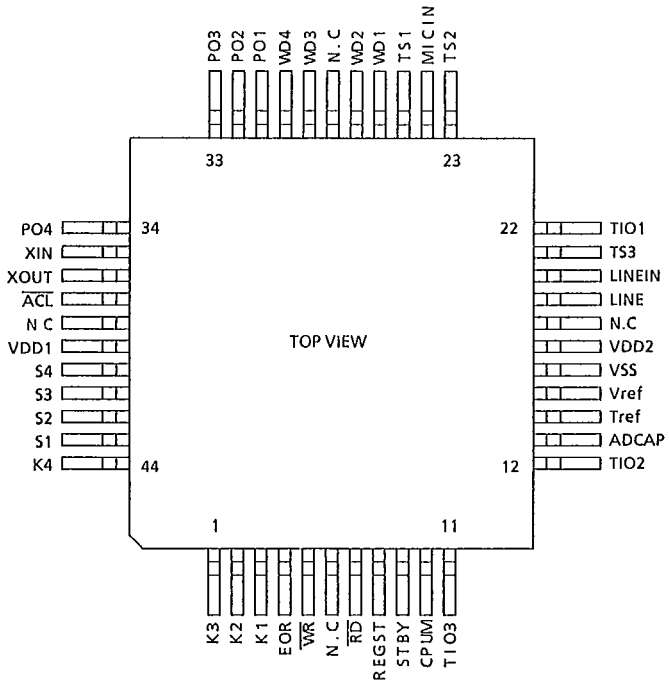


3.3.2 Manual Control Mode



4. PIN DESCRIPTION

4.1 Pin Assignment



4.2 Pin Description

PIN	PIN NO.	STRUCTURE				DESCRIPTION
		MANUAL CONTROL		CPU CONTROL		
		IN / OUT	PULL UP PULL DOWN	IN / OUT	PULL UP PULL DOWN	
TS3 TS2 TS1	21 22 23	IN	PULL DOWN	IN	PULL DOWN	Test input pins. These pins should be set at L level when used by user.
MICIN	24	IN	NO	IN	NO	Microphone connecting pin. A microphone should be connected via a coupling capacitor. This pin is selected when the LINE pin is at L level.
WD1 WD2 WD3 WD4	26 27 29 30	OUT	–	OUT	–	Recognition result pins. At time of the recognition, word No. of the registered words that have been judged to be most close to input voice is transmitted. At time of the registration, the stored word No.is transmitted. After reset, these pin is L level.
K4 K3 K2 K1	44 1 2 3	IN	PULL DOWN	IN / OUT	NO	4 bit bidirectional data bus. 1. CPU CONTROL (1) Command input and status output. (2) When the $\overline{RD}$ pin is H level, these pins serve for input with a latch a command at the leading edge of the $\overline{WR}$ signal. (3) When the $\overline{RD}$ pin is L level, these pins are put in the output mode. * After reset, these pins are in the state to output of the status register. * CHANGE command, the same data as values transmitted at the WD1~4 are transmitted to these pins, which will return to the state to read out the status when the $\overline{RD}$ pin is again set at L level after last rise. 2. MANUAL MODE key input pin.
EOR	4	OUT	–	OUT	–	End of Recognition pin. This pin becomes L level at time of voice input and returns to H level after end of registration / recognition processing.
$\overline{WR}$	5	IN	NO	IN	NO	Signal rising from L to H level is given to this pin in the CPU mode, a command given through the K1~K4 pins is latched. Both the $\overline{RD}$ and $\overline{WR}$ pins should not be set simultaneously at L level.

PIN	PIN NO.	STRUCTURE				DESCRIPTION
		MANUAL CONTROL		CPU CONTROL		
		IN / OUT	PULL UP PULL DOWN	IN / OUT	PULL UP PULL DOWN	
$\overline{RD}$	7	IN	NO	IN	NO	When an L level signal is given to this pin, the K1~K4 pins are placed in the output mode and it becomes possible to read the contents of the status register or those transmitted to the WD1~4 pins. At the rise of this signal from L to H level, this pin is internally switched over to the status output. Both the $\overline{RD}$ and $\overline{WR}$ pins should not be simultaneously set at L level.
REGST	8	IN	PULL DOWN	IN	NO	Input pin used to change over the reject level at time of voice recognition. At time of the manual mode, the on chip pull down resistor is connected to this pin but it is separated at time of the standby state.
STBY	9	IN	NO	IN	NO	Standby control pin. When this pin is set at H level, TC8860F is placed in the standby mode. When this pin is returned to L level, after reset operation, the TC8860F resumes the normal operation.
CPUM	10	IN	NO	IN	NO	CPU / manual mode selector pin. Manual mode results when this pin is at L level, when this pin is set at H level, CPU mode results.
TIO3 TIO2 TIO1	11 12 22	OUT	–	OUT	–	Test I/O pins. Nothing should be connected to these pins when used by user.
ADCAP	13	OUT	–	OUT	–	reference voltage pin for on chip A / D conversion circuit. Time constant capacitor connect to this pin.
Tref	14	OUT	–	OUT	–	The reference voltage pin for on chip voice trigger circuit of TC8860F. A decoupling capacitor is connected to this pin.
Vfef	15	OUT	–	OUT	–	The reference voltage pin for on chip analog circuit of TC8860F. A decoupling capacitor is connected to this pin.
VSS	16	POWER SUPPLY	–	POWER SUPPLY	–	This pin is connected to the negative side
VDD2 VDD1	17 39	POWER SUPPLY	–	POWER SUPPLY	–	This pins are connected to the positive side.

PIN	PIN NO.	STRUCTURE				DESCRIPTION
		MANUAL CONTROL		CPU CONTROL		
		IN / OUT	PULL UP PULL DOWN	IN / OUT	PULL UP PULL DOWN	
LINE	19	IN	NO	IN	NO	The MICIN pin is selected when this pin is at L level and the LINEIN pin is selected when this pin is at H level.
LINEIN	20	IN	NO	IN	NO	Line input pin. Voice signal should be input via a coupling capacitor. This pin is selected when the LINE pin is at H level.
PO1 PO2 PO3 PO4	31 32 33 34	OUT	–	OUT	–	4 bit output pins. PO1 transmits H level at time of registering voice waiting and returns to L level after completion of registration. During the standby state and after reset, PO1 becomes L level. Other PO2~PO4 pins always transmit L level.
XIN XOUT	35 36	IN OUT	– –	IN OUT	– –	Ceramic oscillator connecting pins. An ceramic oscillator and capacitors are connected.
$\overline{ACL}$	37	IN / OUT	NO	IN / OUT	NO	Reset pin. When set at L level, the TC8860F is reset. This pin is kept at L level during the standby state.
S4 S3 S2 S1	40 41 42 43	OUT	–	OUT	–	Key scan signal output pins. During the standby state, L level signals are transmitted.

5. SPECIFICATION

5.1. Voice Recognition

SYSTEM	Speaker dependent word recognition.
VOICE ANALYSIS	4 channel Band pass filter
RECOGNITION WORDS	Max. 10 words.
INPUT VOICE TIME LENGTH	0.16~0.96 sec
RESPONSE TIME	Max. : 0.60 sec, Ave. : 0.35 sec.

5.2. Others

Recognition Results	4 Bit
Command input	Manual control : 4x3 Key matrix CPU control : 4 bit data bus
Registration RAM	Built - in 4Kbit RAM
Oscilation Frequency	800kHz

5.3 Operations and Functions

5.3.1 Configration of Key Matrix

- Numeric keys

  These keys are used to specify word No. for registering and clearing voice. Depressing of 1~10 key puts the TC8860F in the registering voice waiting state. When voice is input at this stage, it is registered under word No. corresponding to the depress key No. When another numeric key is depressed before inputting voice, that new number is specified.

- CLR key

  This key is used to clear a registered word. Direct depress of this key clear all words of 1~10. If this key is depressed in the voice input waiting state after depressing the numeric key, the specified word No. only is cleared.

5.3.2 Registration

[CLR] Clear all stored words (always depress immediately after power is ON).

[1] Specifies word 1. Voice input

Registers under word 1. Word No. is transmitted to WD1~WD4.

[2] Specifies word 2. Voice input

Registers under word 2. Word No. is transmitted to WD1~WD4.

⌇

[10] Erroneously specifies word 10.

[8] Specifies word 8 (correct word No., must be before inputting voice). Voice input

Registers under word 8. Word No. is transmitted to WD1~WD4.

5.3.3 Recognition

Voice input

Recognition result output Word No. is transmitted to WD1~WD4.

⌇

5.3.4 Registered Word Clearing

[3] Specifies word 3.

[CLR] Clears word 3.

[5] Specifies word 5.(erroneous word No.)

[4] Specifies word 4.

[CLR] Clears word 4.

⌇

5.4 CPU control

5.4.1 Commands of TC8860F

(1) NOP (1 nibble) K4 | 0 | 0 | 0 | 0 | K1

No operation. No processing is carried out. This command may be used to interrupt ENTn command before inputting voice.

(2) ENTn (1 nibble) K4 | 0 | 0 | 0 | 1 | K1 ~ K4 | 1 | 0 | 1 | 0 | K1

Specifies word No. to perform registration / clearance. When this command is given, thee TC8860F is placed in the registering voice waiting state. If voice is input at this stage, it is registered under the specified word No. It another command is given before inputting voice, the previous specification is canceled and the processing of the new command starts.

(3) CLEAR (1 nibble) K4 | 1 | 0 | 1 | 1 | K1

When this command is given directly, all registered word Numbers are cleared. It is desirable to execute this command immediately after power is ON. When this command is input in the voice waiting state after giving ENTn command, the specified word only is cleared.

(4) CHANGE (1 nibble) K4 | 1 | 1 | 0 | 0 | K1

This command changes the data output to K1~K4 from the status register to the result of registration / recognition. Normally, output data to K1~K4 is the content of the status register and therefore, to read the registration / recognition result, this command should be given. A waiting time of more than 700μs is required to read output data at K1~K4 from issue of the CHANGE command. Returns to the status register output at the rise of $\overline{RD}$ signal

(5) LOAD (641 nibble) K4 | 1 | 1 | 0 | 1 | K1

Write into the dictionary. This command writes registered data given to K1~K4 into the dictionary area of the on chip 4 K SRAM in order of word 1~Word 10. Refer to the memory map for sequence of data. Host CPU should not give next command until transfer of all data of 10 words is completed. (Next command will not be accepted as a command.)

(6) SAVE (1 nibble) K4 | 1 | 1 | 1 | 0 | K1

Readout from the dictionary. This command transmits data registered in the dictionary area of the on chip 4 K SRAM to WD1~WD4 (K1~K4). Refer to the memory map for sequence of data. Host CPU should not give next command until readout of all data of 11 words including the input buffer area is completed.

(7) TEST (1 nibble) K4 | 1 | 1 | 1 | 1 | K1

Test command. When this command is executed, a test pattern is written into word 4 from word 1 after clearing the dictionary. Therefore, this command can be used for checking the function of TC8860F. For instance, if word 1 is transmitted as the result of recognition when 400 Hz sine wave is input in a time length 0.16~0.96 sec to MICIN pin, the TC8860F functions properly.

Test pattern

Word No.	Frequency	Input Level
1	400 Hz	about 3mV
2	1000	2
3	2000	1.5
4	4000	1.5

(1) BUSY

Becomes 1 during the commands / registration / recognition processing and at time of reset / standby.

(2) EOR

The same as an output value at the EOR pin. Becomes 1 during the voice input and registration / recognition processing.

PIN NAME	K4	K3	K2	K1
STATUS REGISTOR	BUSY	EOR	0	0

5.4.2 Readout Function

When the $\overline{RD}$ pin of TC8860F is set at L level, the K1~K4 pins are replaced in in the output mode and it becomes possible to read out to the status or result of recognition. The details are described here.

(1) What is transmitted to K1~K4 pins when the RD pin is set at L level is the content of the status register or result of registration / recognition.

(2) Immediately after reset or after applying a rising signal from low to high level to the $\overline{RD}$ pin, the content of the status register is transmitted when the $\overline{RD}$ pin is at L level.

(3) When the CHANGE command is executed, the TC8860F is placed in the recognition result output state and the same value as that at the WD1~WD4 pin is transmitted when the $\overline{RD}$ pin is at L level.

(4) If data readout once ends even when the CHANGE command is executed; that is, when the $\overline{RD}$ pin changes from L level to H level, the TC8860F returns again to the status output state.

PIN NAME	K4	K3	K2	K1
RECOGNITION RESULT	WD4	WD3	WD2	WD1

5.4.3 Register / Recognition Monitor Pin

(1) EOR

Normally, H level signal is transmitted. When voice is input, this pin becomes L level. After the registration or recognition processing ended and the result was transmitted to the WD1~WD4 pins, this pin returns to H level. During the standby state, L level signal is transmitted.

(2) WD1~4

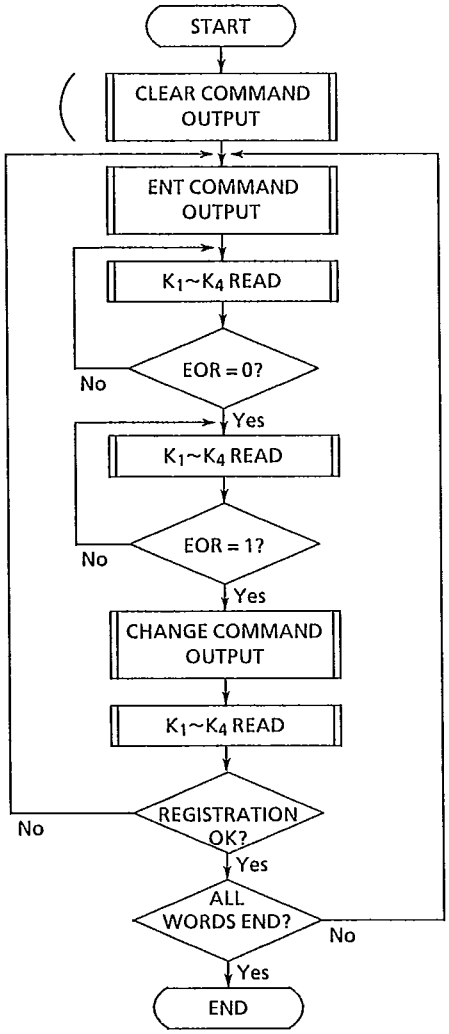
Registration / recognition result is transmitted in 4 bit binary code. These pins become L level immediately after reset and during the standby.

(3) PO1

Normally, L level signal is transmitted. When the numeric keys are depressed in the manual mode or the ENTn command is given in the CPU Mode and the TC8860F is placed in the registering voice waiting state, this pin becomes H level. After ending the registration processing, this pin return to L level. Further, if another key is depressed or another command is given when waiting voice input, this pin also returns to L level. During the standby state, L level signal is transmitted to this pin.

5.4.4 Control Flow From CPU to TC8860F

(1) Registration



The dictionary is cleared completely.

1 word is registered

Voice input waiting
(Status read)

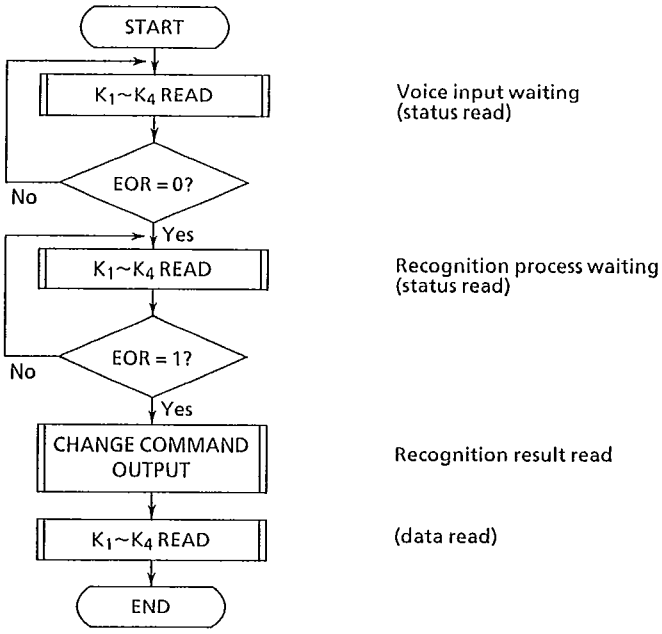
Registering process waiting
(status read)

Registration result readout
(data read)

Note 1. A waiting time of more than 700μs is required from the CHANGE command output to the K1~K4 read.
To read out the result of registration from the WD1~4 pins, the CHANGE command and a waiting time of 700μs and not required.

Note 2 If no result is read from the K1~K4 or WD1~4 pins within 15ms from the rise of the EOR signal, the value may possible be changed by next voice input.

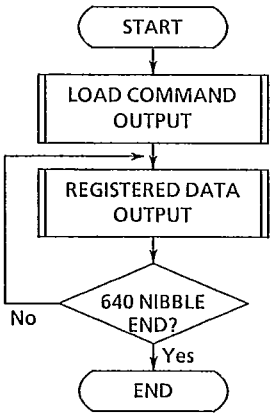
(2) Recognition



Note 1. A waiting time of more than 700μs is required from the CHANGE command output to the K1~4 read. To read out the result of recognition from the WD1~4 pins, the CHANGE command and a waiting time of 700μs are not required.

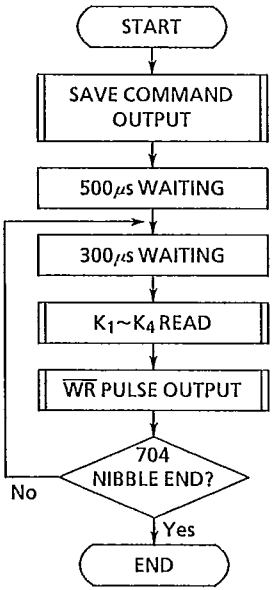
Note 2. If no data read from the K1~4 or WD1~4 pins within 15 ms from the rise of the EOR signal, the value may possibly be changed by next voice input.

(3) LOAD Command



The same flow as that of the command output

(4) SAVE Command



Stored data read

Note: When data to be stored is read through the WD1~WD4 pins, read strobe pulse should also be given to the $\overline{RD}$ pin.
To transmit $\overline{WD}$ pulse, K1~K4 data is optional and it is not necessary to check BSY flag.

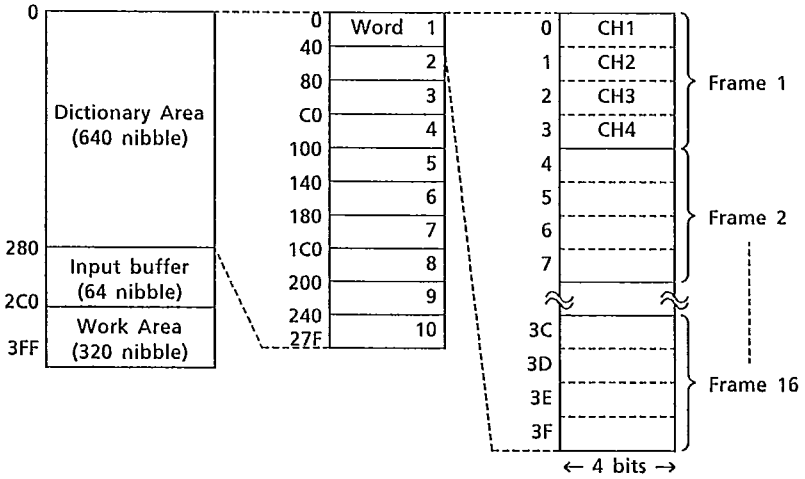
5.5 Output Codes for Registration / Recognition

K4 WD_4	K3 WD_3	K2 WD_2	K1 WD_1	At time of registration	At time of recognition
0	0	0	0	Transmitted only immediately after reset and during standby.	
0	0	0	1	Registered in word 1.	Recognized as word 1.
0	0	1	0	Registered in word 2.	Recognized as word 2.
0	0	1	1	Registered in word 3.	Recognized as word 3.
0	1	0	0	Registered in word 4.	Recognized as word 4.
0	1	0	1	Registered in word 5.	Recognized as word 5.
0	1	1	0	Registered in word 6.	Recognized as word 6.
0	1	1	1	Registered in word 7.	Recognized as word 7.
1	0	0	0	Registered in word 8.	Recognized as word 8.
1	0	0	1	Registered in word 9.	Recognized as word 9.
1	0	1	0	Registered in word 10.	Recognized as word 10.
1	0	1	1	–	–
1	1	0	0	–	–
1	1	0	1	–	Can't be recognized (Rejected)
1	1	1	0	Input voice is too short as it lasts for less than 0.16 sec.	
1	1	1	1	Input voice is too long as it lasts for more than 0.96 sec.	

Note:
1. The content of RAM (Dictionary) remains unchanged even when input voice becomes too short or too long at time of registration.
2. The TC8860F transmits registration / recognition result and dose not accept next voice input for 15ms after the EOR signal returned to H level.
   This is a waiting time for the host side to read registration / recognition result certainly. However, input of command is accepted.

5.6 Registration RAM Memory Map

RAM address (HEX)



Note : ① When the CLEAR command is executed, 0 is written into top 4 words (Frame 1) of each word No.

② The LOAD command transfers data of 640 nibble from the top of the dictionary area.

③ The SAVE command transfers data of 704 nibble including the input buffer to the dictionary area.

5.7 Reject Level Selecting

At time of the voice recognition, a distance (degree of non similarity) is calculated between unknown voice and registered data and the least one within the reject level is transmitted as the result to voice recognition. This reject level can be changed to two stages by the REGST pin on the TC8860F. If the reject level is made large, accurence of rejection may decrease but the possibility for erroneous recognition as other registered words may increase.

REGST Pin	Reject Level	Easiness of Recognition
L	Large	Easy
H	Small	Difficult

5.8 Reset Operation

Though the $\overline{ACL}$ pin of TC8860F is an I / O pin, it is possible to reset the TC8860F by giving L level signal externally by force.

① When the $\overline{ACL}$ pin becomes L level, the TC8860F interrupts all the processing. Further, BSY bit of the status register becomes 1.

② Even when the TC8860F has been reset, the content of the registration RAM remains unchanged.

③ As long as the $\overline{ACL}$ pin is at L level, all output pins are kept at the state immediately before the $\overline{ACL}$ pin was placed at L level. When the $\overline{ACL}$ pin becomes H level, the EOR pin becomes H level, and the WD1~WD4 pins as well as the PO1 pin become L level.

5.9 Standby Mode

When the STBY pin is placed at H level, the TC8860F is put in the standby mode. This pin is placed at H level at an optional timing but it is actually placed in the standby state after end of commands or registration / recognition processing.

① When the TC8860F has been put in the standby mode, the oscillation stops. L level signal is transmitted at the $\overline{ACL}$ pin and BSY bit of the status register becomes 1.

② On chip pull down resistors, which are kept connected to the K1~K4 pins and REGST pin in the manual mode, will be disconnected when the TC8860F is placed in the standby mode. It is not necessary to fix the K1~K4 and REGST pins at either H or L level at this time. (The pins may be kept open.)

③ If the TC8860F is placed in the standby mode under CPU mode, it is also not necessary to fix the K1~K4 and REGST pins at either H or L level.

④ The content of the on chip registration RAM remains unchanged even when the TC8860F is placed in the standby mode.

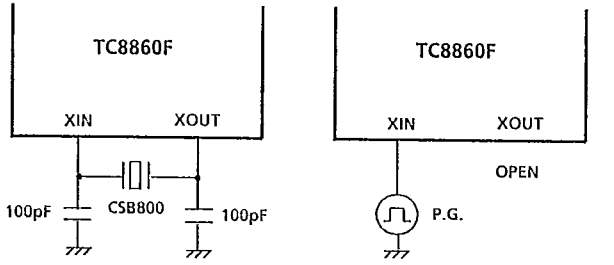
⑤ All output pins become L level.

⑥ When the STBY pin is pulsed at L level, the TC8860F is released from the standby state and returns to the normal operation.

5.10 Clock Generator

TC8860F has clock generator, ceramic resonator and capacitor are connected between XIN and XOUT pins.

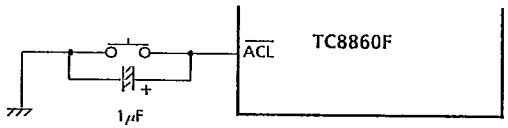
If using external clock, it should be connect to XIN pin directly. (XOUT should be left open.)



(a) Using internal oscillator (b) Using external oscillator

5.11 $\overline{\text{ACL}}$ Pin

Power on reset circuit is constructed by attaching a capacitor to the $\overline{\text{ACL}}$ pin, makes the system initialization is possible immediately after on.

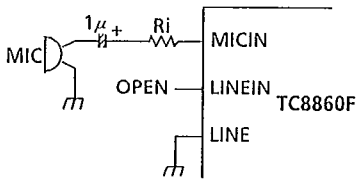


However, the power on reset is effective only for a rapid step power rise and when power rise is gentle or power on / off is repeated in short cycle, no system initialization is performed.

5.12 Voice Input Pin

5.12.1 Microphone Input

The dynamic range of MICIN (max. allowable input to prevent generation of distortion) is 3.5 mVrms. It is possible to decrease gain of the on chip microphone amplifier of the TC8860F and expand the max. input level by connecting a register to the MICIN pin in series.

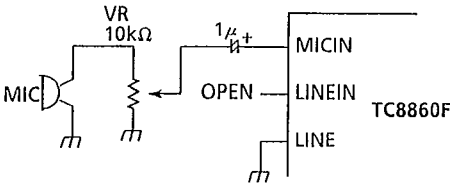


Maximum input level

$DR = (1 + \frac{Ri[k\Omega]}{10}) \times 3.5$ [mVrms]

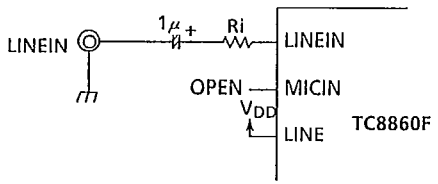
$Ri = 0 \sim 50$ [kΩ]

To further lower the microphone input level as noise is readily picked up if a valve of Ri becomes too large, use a VR as shown below. (This is so with the LINEIN input)



5.12.2 Line Input

The dynamic range of the LINEIN pin is 550 mVrms. It is possible to expand the max. input level by connecting a register to the LINEIN pin in series.



Maximum input level

$DR = (1 + \frac{Ri[k\Omega]}{65}) \times 550$ [mVrms]

$Ri = 0 \sim 100$ [kΩ]

5.12.3 Adjustment of Input Level

To adjust input levels of the MICIN and LINEIN pins, it is a good method to observe output signal level at the TIO1 pin of the TC8860F. Connect a sine wave of 1kHz at about the same level as that obtained when speaked to the microphone in a normal voice for the microphone, etc. Observe the signal at the TIO1 pin at this time through an oscilloscope, etc. and adjust to 250 to 300 mVpp with a VR, etc.

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$-0.3 \sim +6.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V
Storage Temperature	T_{stg}	$-55 \sim +125$	°C

6.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{DD}$	V
Output Voltage	V_{OUT}	$0 \sim V_{DD}$	V
Oscillation Frequency	f_{CLK}	$760 \sim 840$	kHz
Operating Temperature	T_{opr}	$-10 \sim 70$	°C

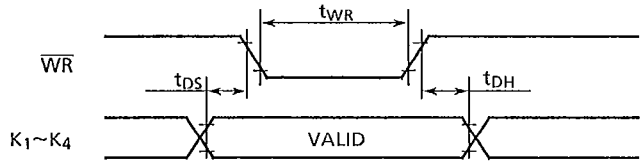
6.3 DC Electrical Characteristic (V_{DD} = + 5.0 V ± 10 %, Ta = 25 °C)

CHARACTERISTIC		SYMBOL	CONDITION	VALUE			UNIT
				MIN.	TYP.	MAX.	
Low Level Input Voltage		V_{IL}		–	–	0.8	V
High level Input Voltage	K1~K4	V_{IH}		2.2	–	–	V
	Except above			V_{DD} – 0.8	–	–	
Low Level Input Current		I_{IL}	V_{IN} = 0 V	–	–	– 5	μA
High level Input Current	K1~K4 REGST	I_{IH}	V_{IN} = V_{DD}, CPUM = V_{IL}	–	100	250	μA
	Except above		V_{IN} = V_{DD}	–	–	5	
Low Level Output Current	S1~S4	I_{OL}	V_{OUT} = 0.4 V	50	–	–	μA
	Except above		V_{OUT} = 0.4 V	0.44	–	–	mA
High level Output Current	S1~S4	I_{OH}	V_{OUT} = V_{DD} – 2.0 V	–	– 2.4	–	mA
	Except above		V_{OUT} = V_{DD} – 0.4 V	– 0.22	–	–	
Supply Current (1)		I_{DD}	At voice input	–	4.5	9.0	mA
Supply Current (2)		I_{STBY}	At standby		–	3	μA

6.4 AC Electrical Characteristics (V_{DD} = 5 V ± 10 %, f_{CLK} = 800 kHz, Ta = 25 °C, C_L = 20 pF)

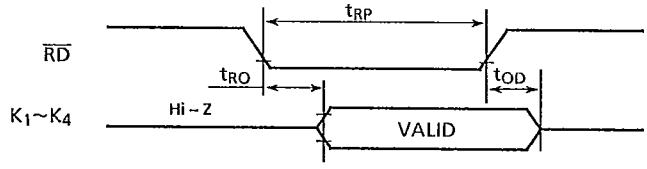
6.4.1 K1~K4 Write Cycle

CHARACTERISTIC	SYMBOL	CONDITION	VALUE			UNIT
			MIN.	TYP.	MAX.	
$\overline{WR}$ Pulse Width	t_{WR}		2	–	–	μs
Data Set Up Time	t_{DS}		1	–	–	
Data Hold Time	t_{DH}		1	–	–	



6.4.2 K1~K4 Read Cycle

CHARACTERISTIC	SYMBOL	CONDITION	VALUE			UNIT
			MIN.	TYP.	MAX.	
$\overline{RD}$ Pulse Width	t_{RP}		2	–	–	μs
Output Delay Time	t_{RO}		–	–	500	ns
Output Disable Time	t_{OD}		–	–	500	

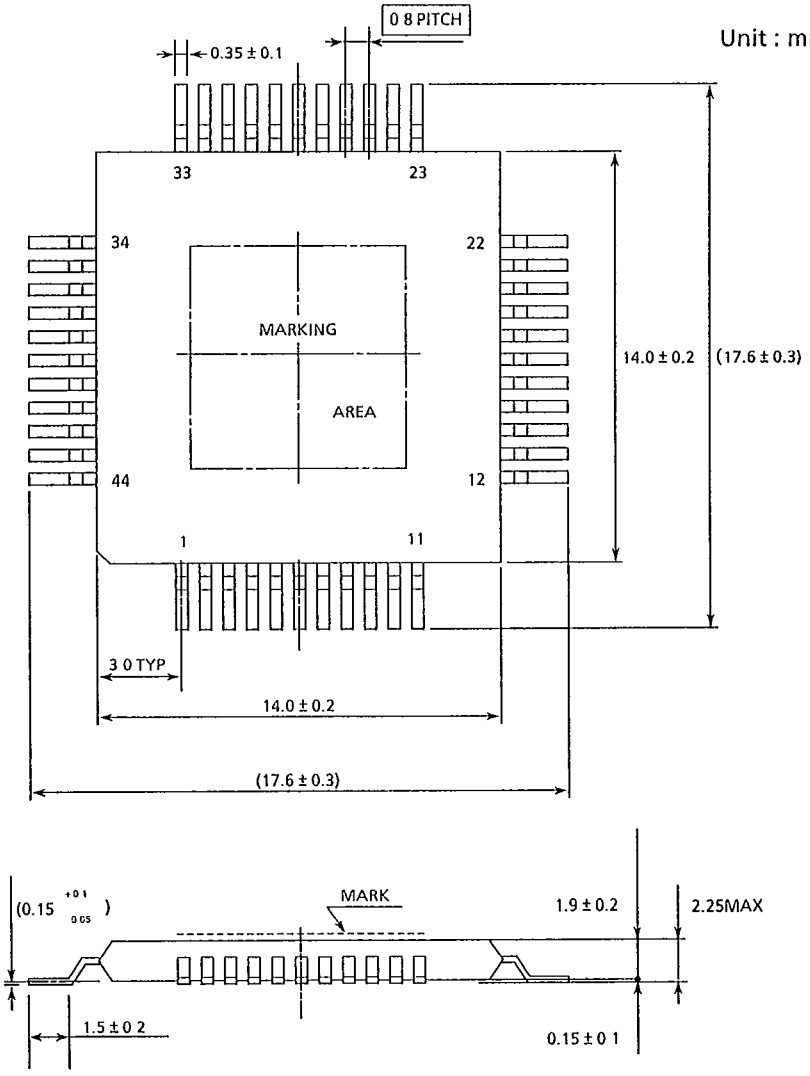


6.5 Analog Input Pin (V_{DD} = + 5.0 V ± 10 %, Ta = 25 °C)

CHARACTERISTIC		SYMBOL	CONDITION	VALUE			UNIT
				MIN.	TYP.	MAX.	
Maximum Input Level	MICIN	U_{in}		–	–	3.5	mVrms
	LINEIN			–	–	550	
Input Resistance	MICIN	R_{in}	f = 1 kHz	–	10	–	kΩ
	LINEIN			–	65	–	

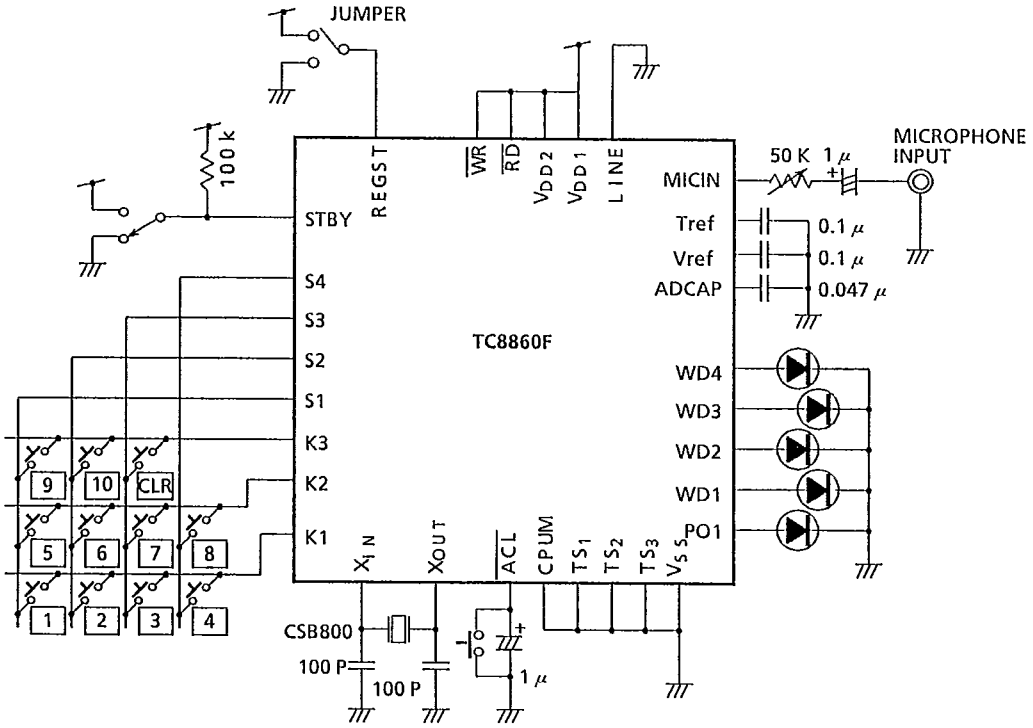
7. PACKAGE OUTLINE

44 Pin Mini flat Package
(QFP44-P-1414A)



8. APPLICATION CIRCUITS

Manual Mode



Note: External capacitors and resistors should be arranged as near TC8860F as possible.