Precision, Dual-Channel Instrumentation Amplifier

Preliminary Technical Data

AD8222

FEATURES

Available in space-saving LFCSP package
Gain set with 1 external resistor (gain range 1 to 1000)
Wide power supply range: ±2.3 V to ±18 V
Temperature range for specified performance: –40°C to +85°C

EXCELLENT AC SPECIFICATIONS

80 dB minimum CMRR to 10 kHz (G = 1)
825 kHz, –3 dB bandwidth (G = 1)
2 V/µs slew rate

LOW NOISE

8 nV/√Hz, @ 1 kHz, maximum input voltage noise
0.25 µV p-p input noise (0.1 Hz to 10 Hz)

HIGH ACCURACY DC PERFORMANCE

80 dB minimum CMRR (G = 1)
120 dB minimum CMRR (G = 100)
70 µV maximum input offset voltage
0.9 µV/°C maximum input offset drift
2 nA maximum input bias current

APPLICATIONS

Industrial process controls
Precision data acquisition systems
Medical instrumentation
Driving differential input ADCs
Bridge amplifiers
Weigh scales
Strain gages
Transducer interfaces

FUNCTIONAL BLOCK DIAGRAM

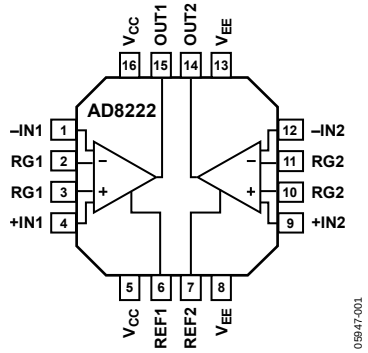

Figure 1. AD8222 Dual Instrumentation Amplifier

GENERAL DESCRIPTION

The AD8222 is a dual-channel, gain programmable, high performance instrumentation amplifier that delivers the industry's highest CMRR over frequency. The CMRR of most instrumentation amplifiers falls off at 200 Hz.

In contrast, the AD8222 maintains a minimum CMRR of 80 dB to 10 kHz for all grades at G = 1. High CMRR over frequency allows the AD8222 to reject wideband interference and line harmonics, greatly simplifying filter requirements. Possible applications include precision data acquisition, biomedical analysis, and industrial process controls.

The AD8222 is available in a 16-lead 4 mm × 4 mm LFCSP_VQ package, 75% less board space than a 16-lead SOIC. This small size makes AD8222 ideal for multichannel or space-constrained applications. The AD8222 is specified for single-ended and differential output operation over the entire industrial temperature range of –40°C to +85°C. It operates on both single and dual supplies.

Rev. PrA

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REVISION HISTORY

3/06—Revision PrA: Preliminary Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

Table 1.

		Single-Ended Output (Both Amplifiers)			Differential Output			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V							
G = 1		80			80			dB
G = 10		100			100			dB
G = 100		120			120			dB
G = 1000		130			130			dB
NOISE	*RTI Noise* = $\sqrt{e_{NI}^2 + (e_{NO}/G)^2}$							
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			8			8	nV/√Hz
Output Voltage Noise, e_{NO}				75			75	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.25			0.25		μV p-p
Current Noise	f = 1 kHz		40			40		fA/√Hz
	f = 0.1 Hz to 10 Hz		6			6		pA p-p
VOLTAGE OFFSET[1]								
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V			70			70	μV
Overtemperature	T = −40°C to +85°C			135			135	μV
Average TC				0.9			0.9	μV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V			600			600	μV
Overtemperature	T = −40°C to +85°C			1			1	mV
Average TC				9			9	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.3 V to ±18 V							
G = 1		90	100		90	100		dB
G = 10		110	120		110	120		dB
G = 100		124	130		124	130		dB
G = 1000		130	140		130	140		dB
INPUT CURRENT								
Input Bias Current			0.5	2		0.5	2	nA
Overtemperature	T = −40°C to +85°C			3			3	nA
Average TC			3			3		pA/°C
Input Offset Current			0.3	1		0.3	1	nA
Overtemperature	T = −40°C to +85°C			1.5			1.5	nA
Average TC			3			3		pA/°C
REFERENCE INPUT								
R_{IN}			20					kΩ
I_{IN}			50	60				μA
Voltage Range		$-V_S$		$+V_S$				V
Gain to Output		1 ± 0.0001						pA/°C
POWER SUPPLY								
Operating Range	V_S = ±2.3 V to ±18 V	±2.3		±18	±2.3		±18	V
Quiescent Current (per Amplifier)			0.75	0.9		1.5	1.8	mA
Overtemperature	T = −40°C to +85°C		1	1.2		2	2.4	mA

Parameter	Conditions	Single-Ended Output (Both Amplifiers) Min	Typ	Max	Differential Output Min	Typ	Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			825			825		kHz
G = 10			562			562		kHz
G = 100			100			100		kHz
G =1000			14.7			14.7		kHz
Settling Time 0.01%	10 V step							
G = 1 to 100			10					µs
G = 1000			80					µs
Settling Time 0.001%	10 V step							
G = 1 to 100			13					µs
G = 1000			110					µs
Slew Rate	G = 1	1.5	2		1.5	2		V/µs
	G = 5 to 1000	2	2.5		3	4		V/µs
GAIN	G = 1 + (49.4 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ± 10 V							
G = 1				0.1			0.1	%
G = 10				0.3			0.3	%
G = 100				0.3			0.3	%
G = 1000				0.3			0.3	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1	R_L = 10 kΩ		3	10		3	10	ppm
G = 100	R_L = 10 kΩ		5	15		5	15	ppm
G = 1000	R_L = 10 kΩ		10	40		10	40	ppm
G = 1 to 100	R_L = 2 kΩ		10	95		10	95	ppm
Gain vs. Temperature								
G = 1			3	10		3	10	ppm/°C
G > 1[2]				−50			−50	ppm/°C
INPUT								
Input Impedance								
Differential			100||2			100||2		GΩ||pF
Common Mode			100||2			100||2		GΩ||pF
Input Operating Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.1	$-V_S$ + 1.9		$+V_S$ − 1.1	V
Overtemperature	T = −40°C to +85°C	$-V_S$ + 2.0		$+V_S$ − 1.2	$-V_S$ + 2.0		$+V_S$ − 1.2	V
Input Operating Voltage Range	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
Overtemperature	T = −40°C to +85°C	$-V_S$ + 2.0		$+V_S$ − 1.2	$-V_S$ + 2.0		$+V_S$ −1.2	V
OUTPUT	R_L = 10 kΩ							
Output Swing	V_S = ±2.3V to ±5V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
Overtemperature	T = −40°C to +85°C	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	V
Output Swing	V_S = ±5V to ±18V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
Overtemperature	T = −40°C to +85°C	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	V
Short-Circuit Current			18			18		mA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C

[1] Total RTI V_{OS} = (V_{OSI}) + (V_{OSO}/G).
[2] Does not include the effects of external resistor R_G.
[3] One input grounded. G = 1.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	TBD mW
Output Short-Circuit Current	Indefinite
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Operational Temperature Range	−40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Specification is for device in free air:

16-Lead LFCSP: θ_{JA} (4-layer JEDEC board) = 48.5°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

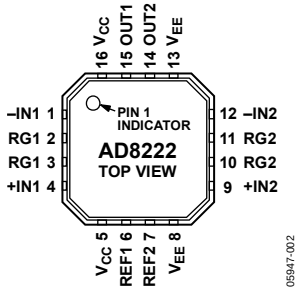

Figure 2. Pin Configuration

Table 3. Pin Function Description

Pin No	Mnemonic	Description
1	–IN1	Negative Input In-Amp 1
2	RG1	Gain Resistor In-Amp 1
3	RG1	Gain Resistor In-Amp 1
4	+IN1	Positive Input In-Amp 1
5	V_{CC}	Positive Supply
6	REF1	Reference Adjust In-Amp 1
7	REF2	Reference Adjust In-Amp 2
8	V_{EE}	Negative Supply
9	+IN2	Positive Input In-Amp 2
10	RG2	Gain Resistor In-Amp 2
11	RG2	Gain Resistor In-Amp 2
12	–IN2	Negative Input In-Amp 2
13	V_{EE}	Negative Supply
14	OUT2	Output In-Amp 2
15	OUT1	Output In-Amp 1
16	V_{CC}	Positive Supply

THEORY OF OPERATION

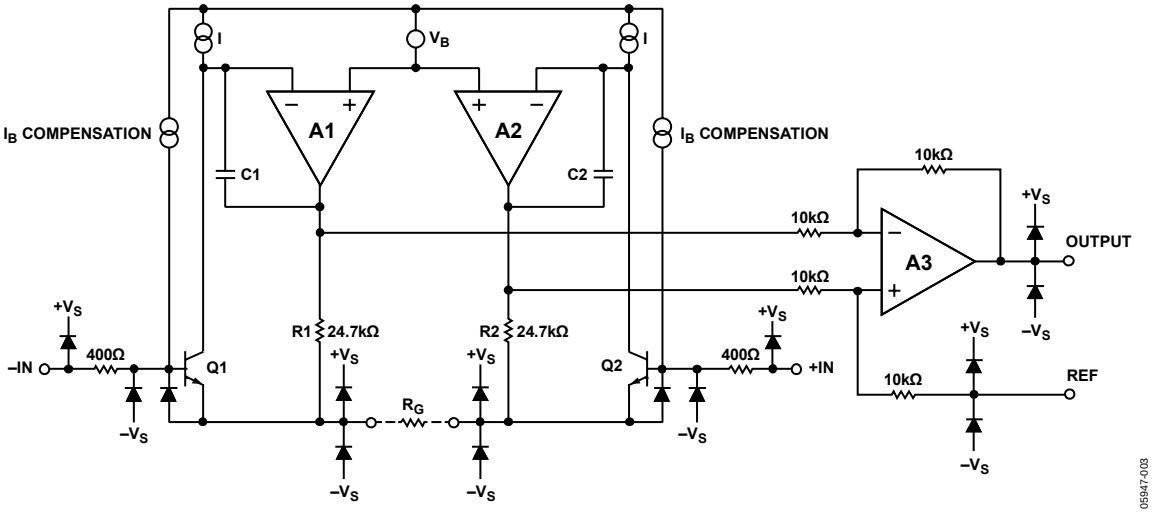

Figure 3. Simplified Schematic

The two instrumentation amplifiers of the AD8222 are based on the classic three op amp topology. Figure 3 shows a simplified schematic of one of the amplifiers. Input Transistor Q1 and Transistor Q2 are biased at a fixed current; therefore, any differential input signal forces the output voltages of A1 and A2 to change accordingly. A signal applied to the input creates a current through R_G, R1, and R2 such that the outputs of A1 and A2 deliver the correct voltage. Topologically, Q1, A1, and R1 and Q2, A2, and R2 can be viewed as precision current feedback amplifiers. The amplified differential and common-mode signals are applied to a difference amplifier that rejects the common-mode voltage but amplifies the differential voltage. The difference amplifier employs innovations that result in low output offset voltage as well as low output offset voltage drift. Laser-trimmed resistors allow for a highly accurate in-amp with gain error typically less than 20 ppm and CMRR that exceeds 90 dB (G = 1).

Using superbeta input transistors and an I_B compensation scheme, the AD8222 offers extremely high input impedance, low I_B, low I_B drift, low I_{OS}, low input bias current noise, and extremely low voltage noise of 8 nV/√Hz.

The transfer function of the AD8222 is

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

Users can easily and accurately set the gain per amplifier using a single standard resistor.

Because the input amplifiers employ a current feedback architecture, the gain-bandwidth product of the AD8222 increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

To maintain precision even at low input levels, special attention was given to the design and layout of the AD8222, resulting in an in-amp whose performance satisfies the most demanding applications.

A unique pinout enables the AD8222 to meet a CMRR specification of 80 dB at 10 kHz (G = 1) and 110 dB at 1 kHz (G = 1000). The balanced pinout, shown in Figure 4, reduces the parasitics that had, in the past, adversely affected CMRR performance. In addition, the new pinout simplifies board layout because associated traces are grouped together. For example, the gain setting resistor pins are adjacent to the inputs.

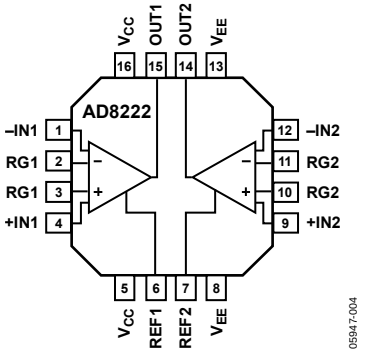

Figure 4. Pinout Diagram

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8222, which can be calculated by referring to Table 4 or by using the following gain equation.

$$R_G = \frac{49.4\ \text{k}\Omega}{G-1}$$

Table 4. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8222 defaults to G = 1 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of R_G. The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

LAYOUT

Careful board layout maximizes system performance. Traces from the gain setting resistor to the R_G pins should be kept as short as possible to minimize parasitic inductance. To ensure the most accurate output, the trace from the REF pins should either be connected to its local ground or connected to a voltage that is referenced to its local ground.

Common-Mode Rejection

One benefit of the high CMRR over frequency of the AD8222 is that it has greater immunity to disturbances, such as line noise and its associated harmonics, than do typical in-amps. Typical instrumentation amplifiers have a CMRR that falls off at 200 Hz; common mode filters are often used to compensate for this shortcoming. The AD8222 is able to reject CMRR over a greater frequency range, reducing the need for filtering.

A well-implemented layout helps to maintain its high CMRR over frequency. Input source impedance and capacitance should be closely matched. In addition, source resistance and capacitance should be placed as close to the inputs as possible.

Grounding

The output voltage of the AD8222 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

In mixed-signal environments, low level analog signals need to be isolated from the noisy digital environment. Many ADCs have separate analog and digital ground pins. Although it is convenient to tie both grounds to a single ground plane, the current traveling through the ground wires and PC board can cause hundreds of millivolts of error. Therefore, separate analog and digital ground returns should be used to minimize the current flow from sensitive points to the system ground.

REFERENCE TERMINAL

As shown in Figure 3, the reference terminal, REF, is at one end of a 10 kΩ resistor. The output of the instrumentation amplifier is referenced to the voltage on this REF terminal; this is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8222 can interface with an ADC. The allowable reference voltage range is a function of the gain, input, and supply voltage. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, source impedance to the REF terminal should be kept low. Additional impedance at the REF terminal results in amplification of the signal connected to the positive input. The amplification can be computed by

$$\frac{2\left(10\ \text{k}\Omega + R_{REF}\right)}{20\ \text{k}\Omega + R_{REF}}$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the amplifier's CMRR.

POWER SUPPLY REGULATION AND BYPASSING

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

A 0.1 μF capacitor should be placed close to each supply pin. As shown in Figure 5, a 10 μF tantalum capacitor can be used further away from the part. In most cases, it can be shared by other precision integrated circuits.

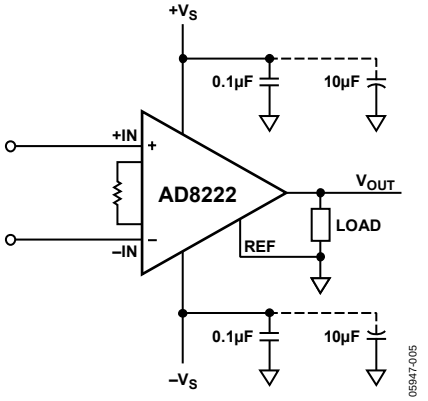

Figure 5. Supply Decoupling—REF and Output Referred to Local Ground

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8222 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 6.

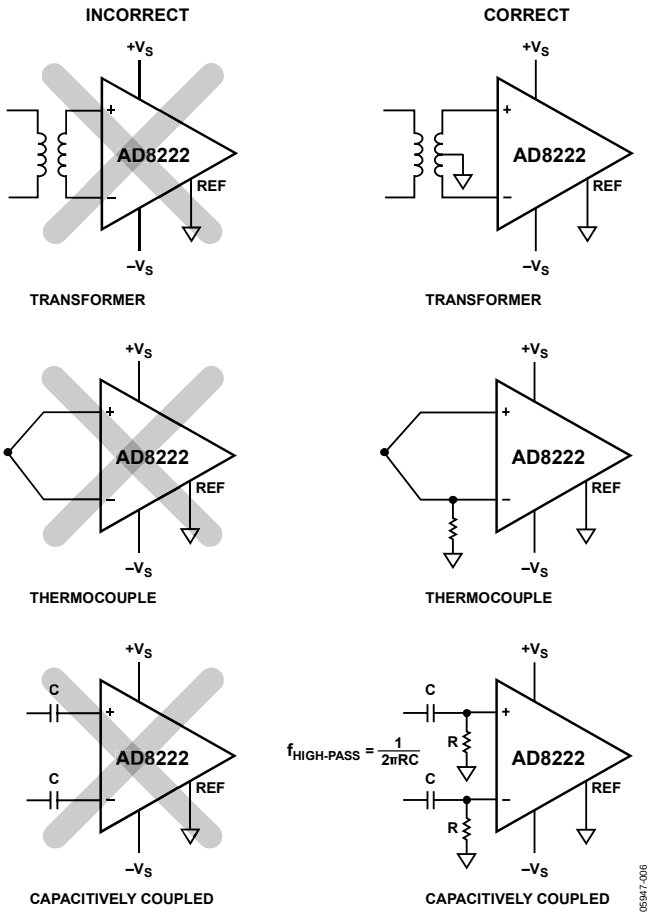

Figure 6. Creating an I_{BIAS} Path

INPUT PROTECTION

All terminals of the AD8221 are protected against ESD (1 kV—human body model). In addition, the input structure allows for dc overload conditions below the negative supply, $-V_S$. The internal 400 Ω resistors limit current in the event of a negative fault condition. However, in the case of a dc overload voltage above the positive supply, $+V_S$, a large current would flow directly through the ESD diode to the positive rail. Therefore, an external resistor should be used in series with the input to limit current for voltages above $+V_S$. In either scenario, the AD8221 can safely handle a continuous 6 mA current, $I = V_{IN}/R_{EXT}$ for positive overvoltage and $I = V_{IN}/(400\ \Omega + R_{EXT})$ for negative overvoltage.

For applications where the AD8221 encounters extreme overload voltages, such as cardiac defibrillators, external series resistors and low leakage diode clamps, such as the BAV199L, the FJH1100s or the SP720, should be used.

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, R-C network placed at the input of the instrumentation amplifier, as shown in Figure 7. The filter limits the input signal bandwidth according to the following relationship.

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

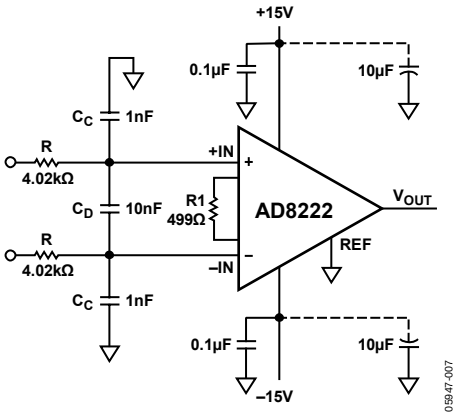

Figure 7. RFI Suppression

C_D affects the difference signal and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at negative input degrades CMRR of the AD8222. By using a value of C_D one magnitude larger than C_C, the effect of the mismatch is reduced, and therefore, performance is improved.

PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8222 make it an excellent candidate for both ac and dc bridge measurements. As shown in Figure 8, the bridge can be directly connected to the inputs of the amplifier.

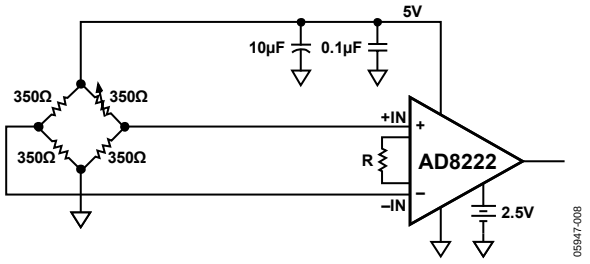

Figure 8. Precision Strain Gage

DIFFERENTIAL OUT

A differential circuit configuration is shown in Figure 9. Amplifier 1 sets the differential voltage by maintaining the following equation:

$$V_{DIFF\_OUT} = +OUT - -OUT = (+IN - -IN) \times G$$

Amplifier 2 sets the output common-mode voltage by maintaining the following equation:

$$V_{CM\_OUT} = (+OUT + -OUT)/2 = (REF\_A + REF\_B)/2$$

Because the differential voltage is set solely by Amplifier 1, all of the precision specifications (offset voltage, offset drift, and 1/f noise) are the same as if Amplifier 1 was operating in single-ended mode.

The output common-mode voltage is set by the average of REF_A and REF_B (that is, +IN2 and REF2 of Amplifier 2). Because REF_A and REF_B have different properties, the reference voltage is easy to set for a wide variety of applications REF_A has high impedance but cannot swing to the supply rails of the part, and REF_B must be driven with a low impedance but can go 500 mV beyond the supply rails. A very common application sets the common-mode output voltage to the midscale of a differential ADC. In this case, the ADC reference voltage would be sent to the REF_A terminal, and ground would be connected to the REF_B terminal. This would produce a common-mode output voltage of half the ADC reference voltage.

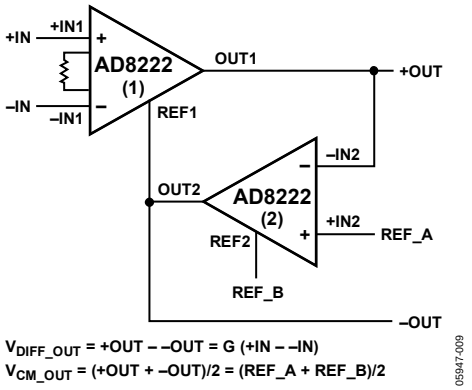

Figure 9. Differential Circuit

OUTLINE DIMENSIONS

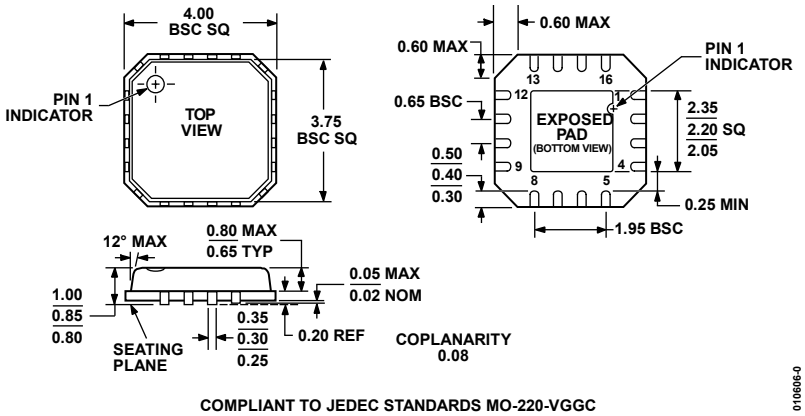

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-9)
Dimensions are shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Product Description	Package Option
AD8222ACPZ-R7[1]	–40°C to +85°C	16-Lead LFCSP_VQ	CP-16-9
AD8222ACPZ-RL[1]	–40°C to +85°C	16-Lead LFCSP_VQ	CP-16-9
AD8222ACPZ-WP[1]	–40°C to +85°C	16-Lead LFCSP_VQ	CP-16-9
AD8222-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

PR05947-0-3/06(PrA)