LH168K

324-output TFT-LCD Source Driver IC

DESCRIPTION

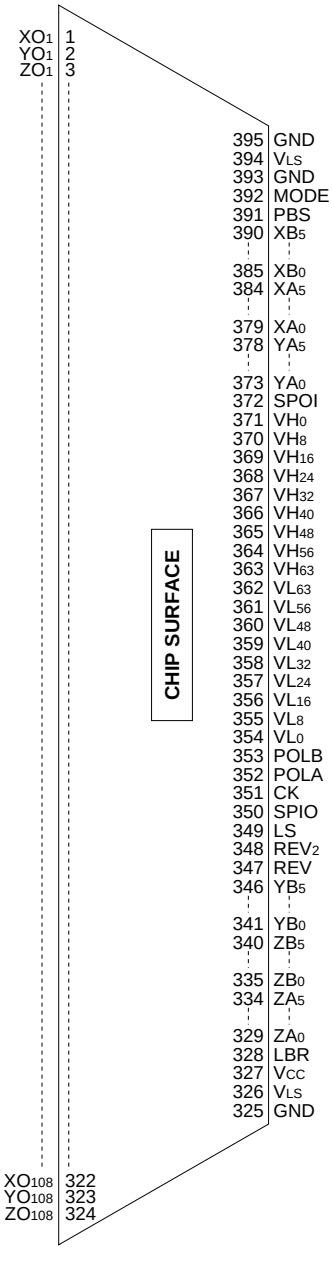
The LH168K is a 324-output TFT-LCD source driver IC which can simultaneously display 262 144 colors in 64 gray scales.

FEATURES

- Selectable number of LCD drive outputs : 324/321/312/309
- Built-in 6-bit digital input DAC
- Dot-inversion drive : Outputs the inverted gray scale voltages between LCD drive pins next to each other
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time at 324-output and 312-output modes. 1-port input for each circuit of data inputs R, G and B at 321-output and 309-output modes.
- Possible to display 262 144 colors in 64 gray scales with reference voltage input of 18 gray scales : This reference voltage input corresponds to γ correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :
  Output shift direction can be selected
  XO_1, YO_1, $ZO_1 \rightarrow XO_{108}$, YO_{108}, ZO_{108} or
  ZO_{108}, YO_{108}, $XO_{108} \rightarrow ZO_1$, YO_1, XO_1
- Shift clock frequency : 55 MHz (MAX.)
- Supply voltages
  – V_{CC} (for logic system) : +2.7 to +3.6 V
  – V_{LS} (for LCD drive system) : +12 V (MAX.)
- Package : 395-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

395-PIN TCP TOP VIEW

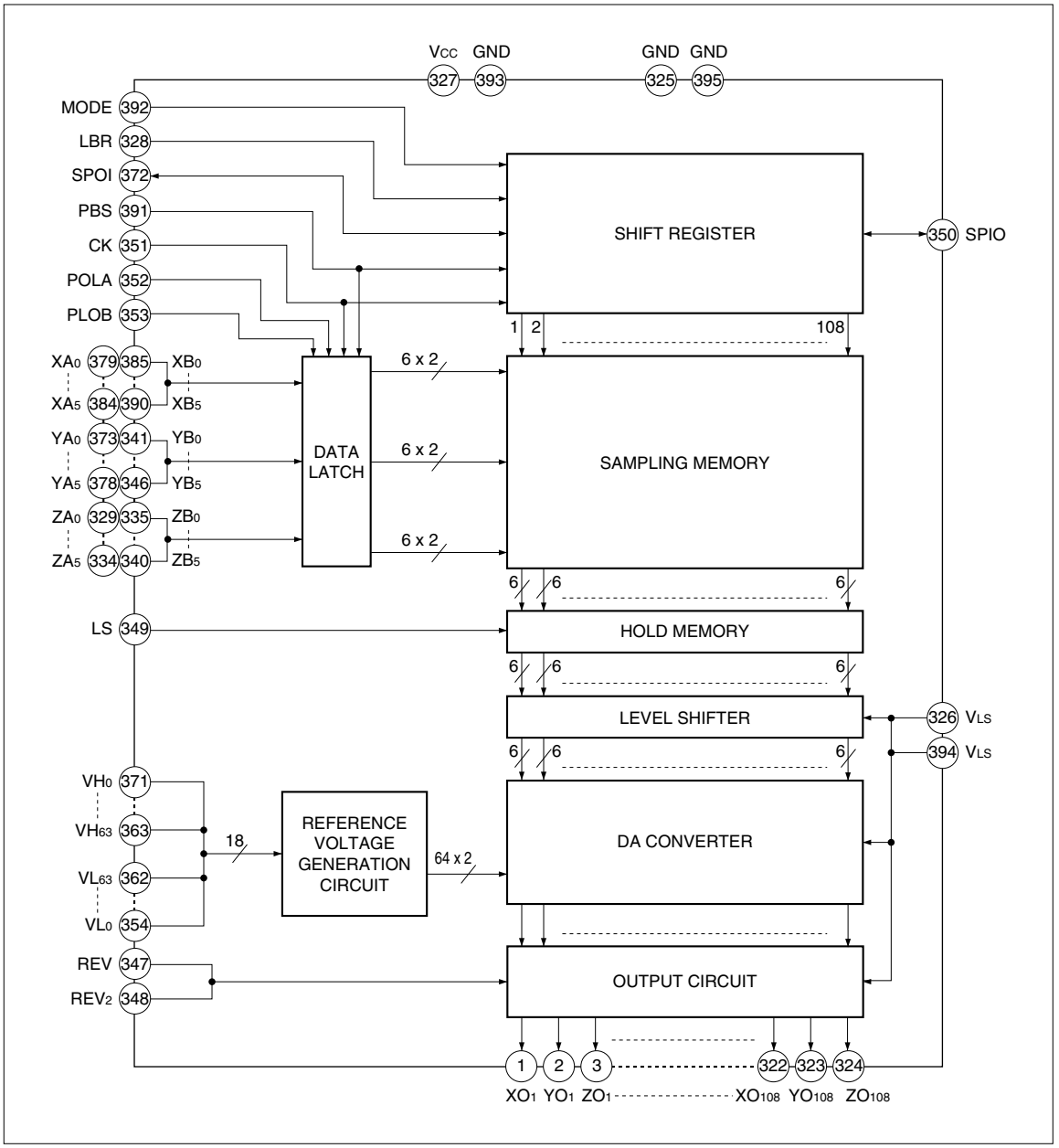


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 324	XO_1-ZO_{108}	O	LCD drive output pins
325, 393, 395	GND	–	Ground pins
326, 394	V_{LS}	–	Power supply pins for analog circuit
327	V_{CC}	–	Power supply pin for digital circuit
328	LBR	I	Shift direction selection input pin
329 to 334	ZA_0-ZA_5	I	Data input pins
335 to 340	ZB_0-ZB_5	I	Data input pins
341 to 346	YB_0-YB_5	I	Data input pins
347, 348	REV, REV_2	I	LCD drive output polarity exchange input pins
349	LS	I	Latch input pin
350	SPIO	I/O	Start pulse input/cascade output pin
351	CK	I	Shift clock input pin
352, 353	POLA, POLB	I	Input data polarity exchange input pins
354 to 362	VL_0-VL_{63}	I	Reference voltage input pins
363 to 371	VH_{63}-VH_0	I	Reference voltage input pins
372	SPOI	I/O	Start pulse input/cascade output pin
373 to 378	YA_0-YA_5	I	Data input pins
379 to 384	XA_0-XA_5	I	Data input pins
385 to 390	XB_0-XB_5	I	Data input pins
391	PBS	I	2-port/1-port selection input pin
392	MODE	I	Input pin for selecting the number of LCD drive outputs

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 64 x 2-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 64 x 2 gray scales to LCD drive output pin.

INPUT/OUTPUT CIRCUITS

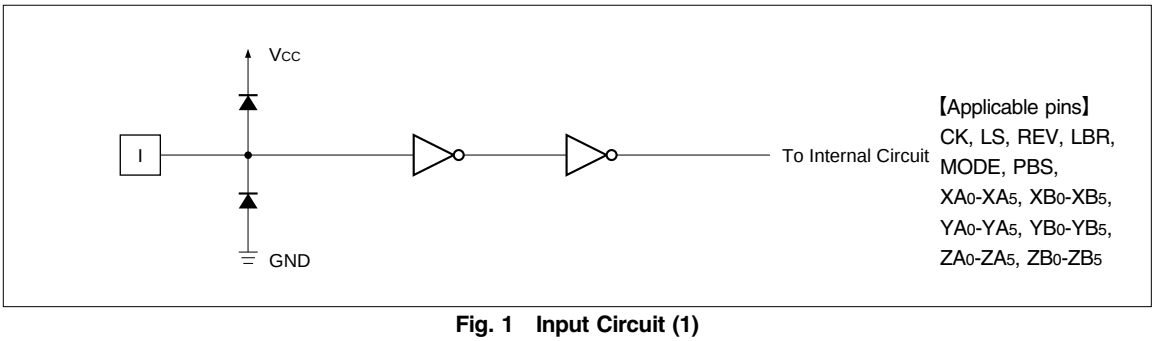


Fig. 1 Input Circuit (1)

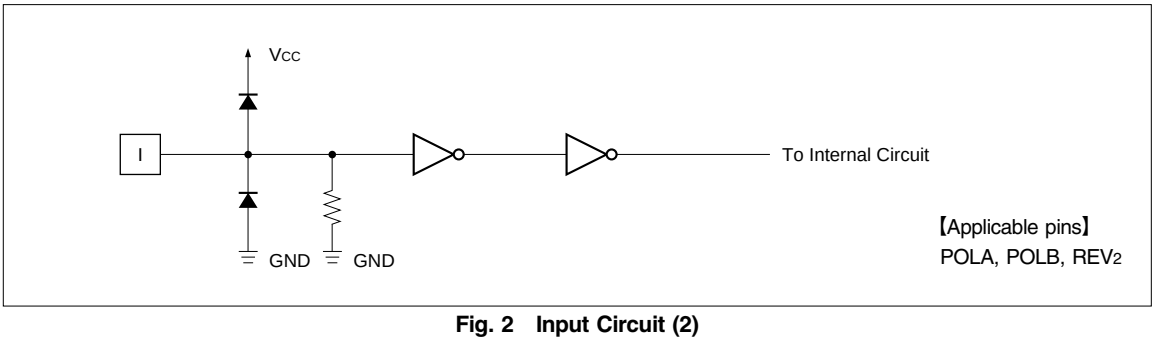


Fig. 2 Input Circuit (2)

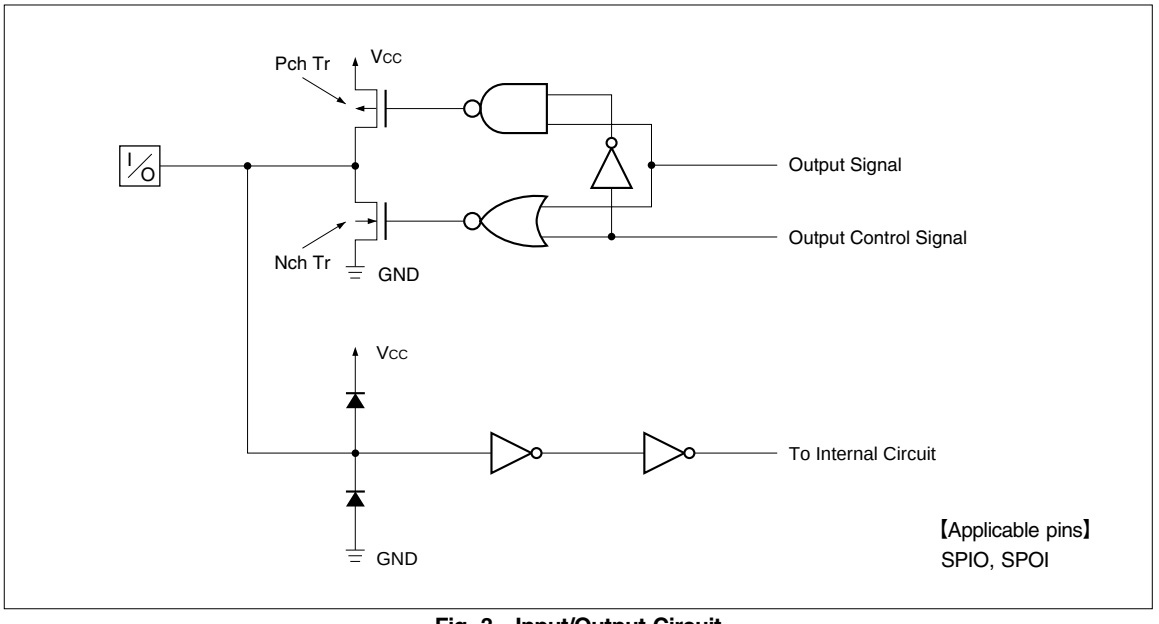


Fig. 3 Input/Output Circuit

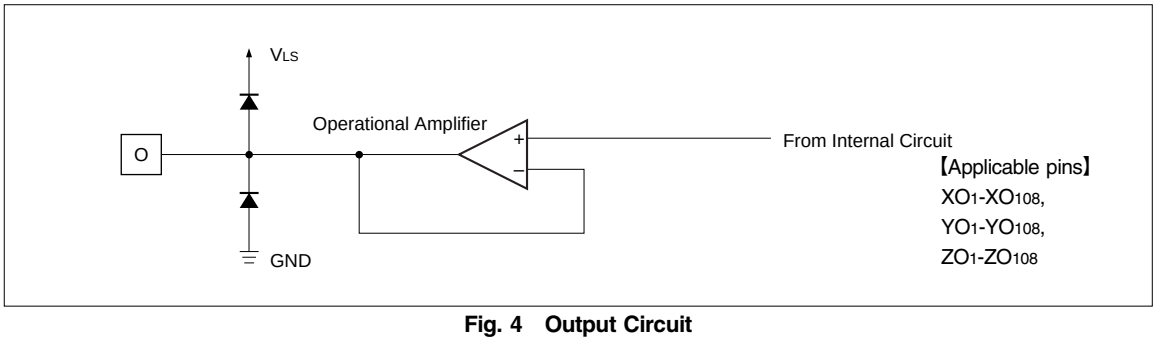


Fig. 4 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
V_{CC}	Used as power supply pin for digital circuit, connected to +2.7 to +3.6 V.
V_{LS}	Used as power supply pin for analog circuit, connected to +8.0 to +12.0 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting, refer to **"Functional Operations"**.
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to **"Functional Operations"**.
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
VH_0-VH_{63} VL_0-VL_{63}	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. For internal gamma correction, refer to **"Gamma Correction Value"**. Observe the following relation for input voltage. $V_{LS} > VH_0 \geq VH_8 \geq \cdots \geq VH_{63} \geq VL_{63} \geq VL_{56} \geq \cdots \geq VL_0 >$ GND.
XA_0-XA_5 YA_0-YA_5 ZA_0-ZA_5 XB_0-XB_5 YB_0-YB_5 ZB_0-ZB_5	Used as data input pins of R, G, and B colors. 6-bit data are input from data pins at the rising edge of CK. When PBS is "L", 2-pixel data are input from XA_0 to XA_5, YA_0 to YA_5, ZA_0 to ZA_5 and XB_0 to XB_5, YB_0 to YB_5, ZB_0 to ZB_5 at the same time. When PBS is "H", 1-pixel data is input from XA_0 to XA_5, YA_0 to YA_5 and ZA_0 to ZA_5, and fixed XB_0 to XB_5, YB_0 to YB_5 and ZB_0 to ZB_5 to "L" or "H". For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**. Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
MODE	Used as input pin for selecting the number of LCD drive outputs, which sets up operation mode with PBS pin. When "L" is entered, it becomes 324-output/2-port input mode at PBS pin "L" or 321-output/1-port input mode at PBS pin "H". When "H" is entered, it becomes 312-output/2-port input mode at PBS pin "L" or 309-output/1-port mode at PBS pin "H". For selecting the number of LCD drive outputs, refer to **"Output Characteristics"**.
PBS	Used as 2-port/1-port exchange input pin to take in data. When "L" is entered, it becomes 2-port input mode and 2-pixel data are input at the same time. When "H" is entered, it becomes 1-port input mode.

SYMBOL	FUNCTIONS
XO_1-XO_{108} YO_1-YO_{108} ZO_1-ZO_{108}	Used as LCD drive output pins which output the voltage corresponding to the input of data input pins. When 321-output mode, 3 outputs (XO_{54} to ZO_{54}) are invalid. When 312-output mode, 12 outputs (XO_{55} to XO_{58}, YO_{55} to YO_{58}, ZO_{55} to ZO_{58}) are invalid. When 309-outputs mode, 15 outputs (XO_{54} to XO_{58}, YO_{54} to YO_{58}, ZO_{54} to ZO_{58}) are invalid. Invalid output pins must be opened. Data of XO_1 to XO_{108} correspond to XA_0 to XA_5 and XB_0 to XB_5. Data of YO_1 to YO_{108} correspond to YA_0 to YA_5 and YB_0 to YB_5, and data of ZO_0 to ZO_{108} correspond to ZA_0 to ZA_5 and ZB_0 to ZB_5. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**.
POLA POLB	Used as input pins for input data polarity exchange, POLA corresponds to XA_0 to XA_5, YA_0 to YA_5 and ZA_0 to ZA_5, and POLB corresponds to XB_0 to XB_5, YB_0 to YB_5 and ZB_0 to ZB_5. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. These pins are pulled down at the inside.
REV REV_2	Used as polarity exchange pins of LCD drive output. Data is taken at the term when LS is "H" and the output polarity of the LCD drive output pin is determined. Function of REV is the same as function of REV_2. Input polarity exchange signal to REV, and REV_2 is fixed to "L" or opened in general. When 321-output/309-output mode, it is possible to exchange output polarity between LCD driver next to each other by fixing REV_2 to "L" or "H" according to position on panel. For exchanging, refer to **"Output Characteristics"**. REV_2 pin is pulled down at the inside.

Functional Operations

The following describes the relation between data input pin and output direction.

(1) PBS = "L"

Data input pin	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5	·····	XB_0-XB_5	YB_0-YB_5	ZB_0-ZB_5
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	·····	XO_{108}	YO_{108}	ZO_{108}

(2) PBS = "H"

Data input pin	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5	·····	XA_0-XA_5	YA_0-YA_5	ZA_0-ZA_5
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	·····	XO_{108}	YO_{108}	ZO_{108}

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO_1, YO_1, ZO_1→XO_{108}, YO_{108}, ZO_{108})	LEFT SHIFT (ZO_{108}, YO_{108}, XO_{108}→ZO_1, YO_1, XO_1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

Output Characteristics

The following describes the relation between operation mode, REV pin, REV_2 pin and output polarity of LCD drive pin.

	WHEN REV = "L", REV_2 = "L" or REV = "H", REV_2 = "H"				WHEN REV = "H", REV_2 = "L" or REV = "L", REV_2 = "H"			
MODE	L	L	H	H	L	L	H	H
PBS	L	H	L	H	L	H	L	H
Operation	324-output mode	321-output mode	312-output mode	309-output mode	324-output mode	321-output mode	312-output mode	309-output mode
XO_1	–	–	–	–	+	+	+	+
YO_1	+	+	+	+	–	–	–	–
ZO_1	–	–	–	–	+	+	+	+
XO_2	+	+	+	+	–	–	–	–
YO_2	–	–	–	–	+	+	+	+
ZO_2	+	+	+	+	–	–	–	–

XO_{53}	–	–	–	–	+	+	+	+
YO_{53}	+	+	+	+	–	–	–	–
ZO_{53}	–	–	–	–	+	+	+	+
XO_{54}	+	NA	+	NA	–	NA	–	NA
YO_{54}	–	NA	–	NA	+	NA	+	NA
ZO_{54}	+	NA	+	NA	–	NA	–	NA
XO_{55}	–	+	NA	NA	+	–	NA	NA
YO_{55}	+	–	NA	NA	–	+	NA	NA
ZO_{55}	–	+	NA	NA	+	–	NA	NA
XO_{56}	+	–	NA	NA	–	+	NA	NA
YO_{56}	–	+	NA	NA	+	–	NA	NA
ZO_{56}	+	–	NA	NA	–	+	NA	NA
XO_{57}	–	+	NA	NA	+	–	NA	NA
YO_{57}	+	–	NA	NA	–	+	NA	NA
ZO_{57}	–	+	NA	NA	+	–	NA	NA
XO_{58}	+	–	NA	NA	–	+	NA	NA
YO_{58}	–	+	NA	NA	+	–	NA	NA
ZO_{58}	+	–	NA	NA	–	+	NA	NA
XO_{59}	–	+	–	+	+	–	+	–
YO_{59}	+	–	+	–	–	+	–	+
ZO_{59}	–	+	–	+	+	–	+	–

XO_{107}	–	+	–	+	+	–	+	–
YO_{107}	+	–	+	–	–	+	–	+
ZO_{107}	–	+	–	+	+	–	+	–
XO_{108}	+	–	+	–	–	+	–	+
YO_{108}	–	+	–	+	+	–	+	–
ZO_{108}	+	–	+	–	–	+	–	+

NOTES :

+ : The gray scale voltages corresponding to reference voltage VH_0 to VH_{63} are output.

– : The gray scale voltages corresponding to reference voltage VL_0 to VL_{63} are output.

NA : Non active. Must be opened.

Output Voltage Value

Two voltages are selected from all of the reference voltages (V_0-V_{63}) by the upper 3-bit data (D_5, D_4 and D_3) of the 6-bit input data (D_5, D_4, D_3, D_2, D_1 and D_0) taken by time sharing, and intermediate value is determined by the lower 3-bit data (D_2, D_1 and D_0).

The V_i is a reference voltage (VH_i or VL_i) that is determined by the polarity exchange input (REV and REV_2).

Relation between input data and output voltage values is shown below.

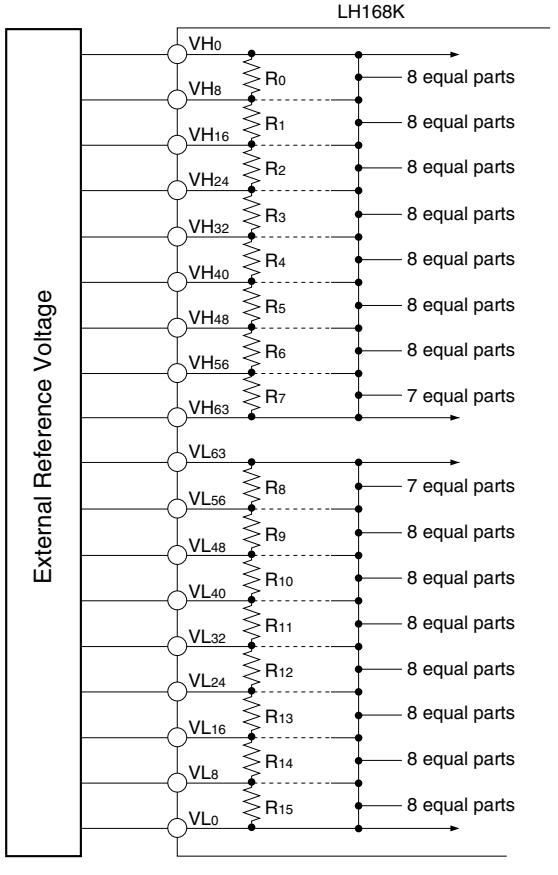
(i = 0, 8, 16, 24, 32, 40, 48, 56, 63)

INPUT DATA	OUTPUT VOLTAGE		INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"		POLA (POLB) = "L"	POLA (POLB) = "H"
0	V_0	V_{63}	20	V_{32}	$V_{32} + (V_{24} - V_{32}) \times 1/8$
1	$V_8 + (V_0 - V_8) \times 7/8$	$V_{63} + (V_{56} - V_{63}) \times 1/7$	21	$V_{40} + (V_{32} - V_{40}) \times 7/8$	$V_{32} + (V_{24} - V_{32}) \times 2/8$
2	$V_8 + (V_0 - V_8) \times 6/8$	$V_{63} + (V_{56} - V_{63}) \times 2/7$	22	$V_{40} + (V_{32} - V_{40}) \times 6/8$	$V_{32} + (V_{24} - V_{32}) \times 3/8$
3	$V_8 + (V_0 - V_8) \times 5/8$	$V_{63} + (V_{56} - V_{63}) \times 3/7$	23	$V_{40} + (V_{32} - V_{40}) \times 5/8$	$V_{32} + (V_{24} - V_{32}) \times 4/8$
4	$V_8 + (V_0 - V_8) \times 4/8$	$V_{63} + (V_{56} - V_{63}) \times 4/7$	24	$V_{40} + (V_{32} - V_{40}) \times 4/8$	$V_{32} + (V_{24} - V_{32}) \times 5/8$
5	$V_8 + (V_0 - V_8) \times 3/8$	$V_{63} + (V_{56} - V_{63}) \times 5/7$	25	$V_{40} + (V_{32} - V_{40}) \times 3/8$	$V_{32} + (V_{24} - V_{32}) \times 6/8$
6	$V_8 + (V_0 - V_8) \times 2/8$	$V_{63} + (V_{56} - V_{63}) \times 6/7$	26	$V_{40} + (V_{32} - V_{40}) \times 2/8$	$V_{32} + (V_{24} - V_{32}) \times 7/8$
7	$V_8 + (V_0 - V_8) \times 1/8$	V_{56}	27	$V_{40} + (V_{32} - V_{40}) \times 1/8$	V_{24}
8	V_8	$V_{56} + (V_{48} - V_{56}) \times 1/8$	28	V_{40}	$V_{24} + (V_{16} - V_{24}) \times 1/8$
9	$V_{16} + (V_8 - V_{16}) \times 7/8$	$V_{56} + (V_{48} - V_{56}) \times 2/8$	29	$V_{48} + (V_{40} - V_{48}) \times 7/8$	$V_{24} + (V_{16} - V_{24}) \times 2/8$
A	$V_{16} + (V_8 - V_{16}) \times 6/8$	$V_{56} + (V_{48} - V_{56}) \times 3/8$	2A	$V_{48} + (V_{40} - V_{48}) \times 6/8$	$V_{24} + (V_{16} - V_{24}) \times 3/8$
B	$V_{16} + (V_8 - V_{16}) \times 5/8$	$V_{56} + (V_{48} - V_{56}) \times 4/8$	2B	$V_{48} + (V_{40} - V_{48}) \times 5/8$	$V_{24} + (V_{16} - V_{24}) \times 4/8$
C	$V_{16} + (V_8 - V_{16}) \times 4/8$	$V_{56} + (V_{48} - V_{56}) \times 5/8$	2C	$V_{48} + (V_{40} - V_{48}) \times 4/8$	$V_{24} + (V_{16} - V_{24}) \times 5/8$
D	$V_{16} + (V_8 - V_{16}) \times 3/8$	$V_{56} + (V_{48} - V_{56}) \times 6/8$	2D	$V_{48} + (V_{40} - V_{48}) \times 3/8$	$V_{24} + (V_{16} - V_{24}) \times 6/8$
E	$V_{16} + (V_8 - V_{16}) \times 2/8$	$V_{56} + (V_{48} - V_{56}) \times 7/8$	2E	$V_{48} + (V_{40} - V_{48}) \times 2/8$	$V_{24} + (V_{16} - V_{24}) \times 7/8$
F	$V_{16} + (V_8 - V_{16}) \times 1/8$	V_{48}	2F	$V_{48} + (V_{40} - V_{48}) \times 1/8$	V_{16}
10	V_{16}	$V_{48} + (V_{40} - V_{48}) \times 1/8$	30	V_{48}	$V_{16} + (V_8 - V_{16}) \times 1/8$
11	$V_{24} + (V_{16} - V_{24}) \times 7/8$	$V_{48} + (V_{40} - V_{48}) \times 2/8$	31	$V_{56} + (V_{48} - V_{56}) \times 7/8$	$V_{16} + (V_8 - V_{16}) \times 2/8$
12	$V_{24} + (V_{16} - V_{24}) \times 6/8$	$V_{48} + (V_{40} - V_{48}) \times 3/8$	32	$V_{56} + (V_{48} - V_{56}) \times 6/8$	$V_{16} + (V_8 - V_{16}) \times 3/8$
13	$V_{24} + (V_{16} - V_{24}) \times 5/8$	$V_{48} + (V_{40} - V_{48}) \times 4/8$	33	$V_{56} + (V_{48} - V_{56}) \times 5/8$	$V_{16} + (V_8 - V_{16}) \times 4/8$
14	$V_{24} + (V_{16} - V_{24}) \times 4/8$	$V_{48} + (V_{40} - V_{48}) \times 5/8$	34	$V_{56} + (V_{48} - V_{56}) \times 4/8$	$V_{16} + (V_8 - V_{16}) \times 5/8$
15	$V_{24} + (V_{16} - V_{24}) \times 3/8$	$V_{48} + (V_{40} - V_{48}) \times 6/8$	35	$V_{56} + (V_{48} - V_{56}) \times 3/8$	$V_{16} + (V_8 - V_{16}) \times 6/8$
16	$V_{24} + (V_{16} - V_{24}) \times 2/8$	$V_{48} + (V_{40} - V_{48}) \times 7/8$	36	$V_{56} + (V_{48} - V_{56}) \times 2/8$	$V_{16} + (V_8 - V_{16}) \times 7/8$
17	$V_{24} + (V_{16} - V_{24}) \times 1/8$	V_{40}	37	$V_{56} + (V_{48} - V_{56}) \times 1/8$	V_8
18	V_{24}	$V_{40} + (V_{32} - V_{40}) \times 1/8$	38	V_{56}	$V_8 + (V_0 - V_8) \times 1/8$
19	$V_{32} + (V_{24} - V_{32}) \times 7/8$	$V_{40} + (V_{32} - V_{40}) \times 2/8$	39	$V_{63} + (V_{56} - V_{63}) \times 6/7$	$V_8 + (V_0 - V_8) \times 2/8$
1A	$V_{32} + (V_{24} - V_{32}) \times 6/8$	$V_{40} + (V_{32} - V_{40}) \times 3/8$	3A	$V_{63} + (V_{56} - V_{63}) \times 5/7$	$V_8 + (V_0 - V_8) \times 3/8$
1B	$V_{32} + (V_{24} - V_{32}) \times 5/8$	$V_{40} + (V_{32} - V_{40}) \times 4/8$	3B	$V_{63} + (V_{56} - V_{63}) \times 4/7$	$V_8 + (V_0 - V_8) \times 4/8$
1C	$V_{32} + (V_{24} - V_{32}) \times 4/8$	$V_{40} + (V_{32} - V_{40}) \times 5/8$	3C	$V_{63} + (V_{56} - V_{63}) \times 3/7$	$V_8 + (V_0 - V_8) \times 5/8$
1D	$V_{32} + (V_{24} - V_{32}) \times 3/8$	$V_{40} + (V_{32} - V_{40}) \times 6/8$	3D	$V_{63} + (V_{56} - V_{63}) \times 2/7$	$V_8 + (V_0 - V_8) \times 6/8$
1E	$V_{32} + (V_{24} - V_{32}) \times 2/8$	$V_{40} + (V_{32} - V_{40}) \times 7/8$	3E	$V_{63} + (V_{56} - V_{63}) \times 1/7$	$V_8 + (V_0 - V_8) \times 7/8$
1F	$V_{32} + (V_{24} - V_{32}) \times 1/8$	V_{32}	3F	V_{63}	V_0

γ (Gamma) Correction Value

Between reference voltage input pins VH_0 and VH_{63}, 63 resistors are connected in series. And between reference voltage input pins VL_0 and VL_{63}, 63 resistors are connected in series. No resistor is connected between reference voltage input pins VH_{63} and VL_{63}.

The γ correction curve is a broken line connected between intermediate voltage inputs (VH_8, VH_{16}, VH_{24}, VH_{32}, VH_{40}, VH_{48}, VH_{56}, VL_8, VL_{16}, VL_{24}, VL_{32}, VL_{40}, VL_{48} and VL_{56}). Each γ correction value between the intermediate voltage inputs is divided into 7 or 8 parts by the same resistor.



The following shows the ratio of γ correction resistance, when R_0 equals 1.

R_0	1.00
R_1	0.20
R_2	0.10
R_3	0.10
R_4	0.10
R_5	0.10
R_6	0.10
R_7	0.20

R_8	0.20
R_9	0.10
R_{10}	0.10
R_{11}	0.10
R_{12}	0.10
R_{13}	0.10
R_{14}	0.20
R_{15}	1.00

PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

V_{CC} → logic input → V_{LS}, VH_0-VH_{63}, VL_0-VL_{63}

When disconnecting the power supply, follow the reverse sequence.

Reference voltage input

The relation of the reference voltage input is shown here.

$V_{LS} > VH_0 \geq VH_8 \geq \cdots \geq VH_{56} \geq VH_{63} \geq 0.5V_{LS} \geq VL_{63} \geq VL_{56} \geq \cdots \geq VL_8 \geq VL_0 >$ GND

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

Target output load

This IC is designed for a 150 pF output load capacity. When using this IC for other than 150 pF panels, confirm the device is having no problem before using it.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{CC}	V_{CC}	−0.3 to +6.0	V	1, 2
	V_{LS}	V_{LS}	−0.3 to +13.0	V	
Input voltage	V_I	VH_0-VL_0	−0.3 to V_{LS} + 0.3	V	
	V_I	SPIO, SPOI, CK, LS, REV, REV_2, LBR, POLA, POLB, MODE, PBS, XA_0-XA_5, XB_0-XB_5, YA_0-YA_5, YB_0-YB_5, ZA_0-ZA_5, ZB_0-ZB_5	−0.3 to V_{CC} + 0.3	V	
Output voltage	V_O	SPIO, SPOI	−0.3 to V_{CC} + 0.3	V	
	V_O	XO_1-ZO_{108}	−0.3 to V_{LS} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to GND (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	+2.7		+3.6	V	1
	V_{LS}	+8.0		+12.0	V	
Reference voltage input	VH_0-VH_{63}	0.5V_{LS}		V_{LS} − 0.1	V	
	VL_0-VL_{63}	+0.1		0.5V_{LS}	V	
Clock frequency	f_{CK}			55	MHz	
LCD drive output load capacity	C_L			150	pF	
Operating temperature	T_{OPR}	−20		+75	°C	

NOTE :

1. The applicable voltage on any pin with respect to GND (0 V).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = +2.7 to +3.6 V, V_{LS} = +8.0 to +12.0 V, T_{OPR} = −20 to +75 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, REV_2, POLA, POLB, MODE, PBS	GND		0.3V_{CC}	V	
Input "High" voltage	V_{IH}			0.7V_{CC}		V_{CC}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.3 mA		V_{CC} − 0.4		V_{CC}	V	
Input "Low" current	I_{ILL1}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, REV_2, POLA, POLB, MODE, PBS			10	µA	
Input "High" current	I_{ILH1}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, SPIO, SPOI, CK, LS, LBR, REV, MODE, PBS			10	µA	
	I_{ILH2}		POLA, POLB, REV_2			400	µA	
Supply current (In operation mode)	I_{CC1}	f_{CK} = 55 MHz f_{LS} = 50 kHz (Data sampling state)	V_{CC}-GND			12	mA	
Supply current (In standby mode)	I_{CC2}	f_{CK} = 55 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)				1.5	mA	
Supply current (In operation mode)	I_{LS1}	f_{CK} = 55 MHz f_{LS} = 50 kHz (Data sampling state)	V_{LS}-GND			4.5	mA	
Supply current (In standby mode)	I_{LS2}	f_{CK} = 55 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)				3.5	mA	
Output voltage range	V_{OUT}		XO_1-ZO_{108}	GND + 0.2		V_{LS} − 0.2	V	1
Deviations between output voltage pins	V_{OD}			−20		+20	mV	
Output current	I_{O1}-I_{O4}				200		µA	2
Resistance between reference voltage input pins	R_{GMAH}		VH_0-VH_{63}		20		kΩ	
	R_{GMAL}		VL_0-VL_{63}		20		kΩ	

NOTES :

1. Criterion of evaluating voltage deviations.
   (a) Between output voltage pins
   Measuring values : Output voltage value at the time after 10 µs at the rising edge of LS. (Average of several times)
   (Conditions) Output load capacity is 150 pF.
   In a state when the reference voltage is fixed.
   Expecting values : Calculated following these specifications.
   (Conditions) In a state when the reference voltage is fixed.
   (b) Between LCD drivers
   Measuring values : Applicable to (a).
   (Conditions) Applicable to (a).
   Expecting values : Applicable to (a).
   (Conditions) Applicable to (a).
   Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.

2. I_{O1} : Applied voltage = 8.0 V for output pins XO_1 to ZO_{108}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{108}.
   V_{LS} = 10.0 V
   I_{O2} : Applied voltage = 7.0 V for output pins XO_1 to ZO_{108}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{108}.
   V_{LS} = 10.0 V
   I_{O3} : Applied voltage = 3.0 V for output pins XO_1 to ZO_{108}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{108}.
   V_{LS} = 10.0 V
   I_{O4} : Applied voltage = 2.0 V for output pins XO_1 to ZO_{108}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{108}.
   V_{LS} = 10.0 V

AC Characteristics (V_{CC} = +2.7 to +3.6 V, V_{LS} = +8.0 to +12.0 V, T_{OPR} = –20 to +75 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CK}		CK			55	MHz
"H" level pulse width	t_{CWH}			4			ns
"L" level pulse width	t_{CWL}			4			ns
Input rise time	t_{CR}					10	ns
Input fall time	t_{CF}					10	ns
Data setup time	t_{SUD}		XA_0-XA_5, YA_0-YA_5, ZA_0-ZA_5, XB_0-XB_5, YB_0-YB_5, ZB_0-ZB_5, POLA, POLB	4			ns
Data hold time	t_{HD}			0			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	4			ns
Start pulse hold time	t_{HSP}			0			ns
Start pulse width	t_{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 15 pF				12	ns
LCD drive output delay time 1	t_{DO1}	C_L = 150 pF	XO_1-ZO_{108}			3	µs
LCD drive output delay time 2	t_{DO2}	C_L = 150 pF				10	µs
LS signal-SPI signal setup time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t_{HLS}			7			ns
LS signal "H" level width	t_{WLS}			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t_{SURV}		REV, REV_2	14			ns
REV signal-LS signal hold time	t_{HRV}			10			ns

Timing Chart