



Features

- Up to 33 dBm Output Power in CW Mode
- High Power Added Efficiency (PAE)
- Single Supply Operation at 2.4 V (1 W) or 3.2 V (2 W)
- Current Consumption in Power-down Mode $\leq 10 \mu\text{A}$
- No External Power Supply Switch Required
- Power Ramp Control
- Simple Input and Output Matching for Maximum Flexibility
- SMD Package (PSSOP16 with Heat Slug)

Electrostatic sensitive device.
Observe precautions for handling.

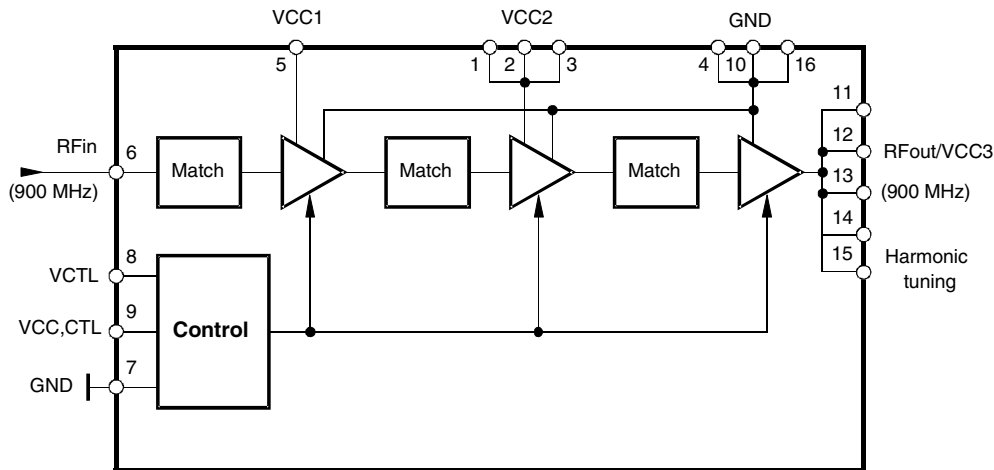


Description

The T0930 is a monolithic integrated power amplifier IC. The device is manufactured with Atmel's Silicon-Germanium (SiGe) technology and has been designed for use in 900-MHz two-way pagers, PDAs, meter readers and ISM phones.

With a single supply voltage of 2.4 V to 3.4 V and a neglectable leakage current in power-down mode, the pager amplifier only needs few external components and thus helps to reduce system costs. It is suited for operation in CW mode.

Figure 1. Block Diagram



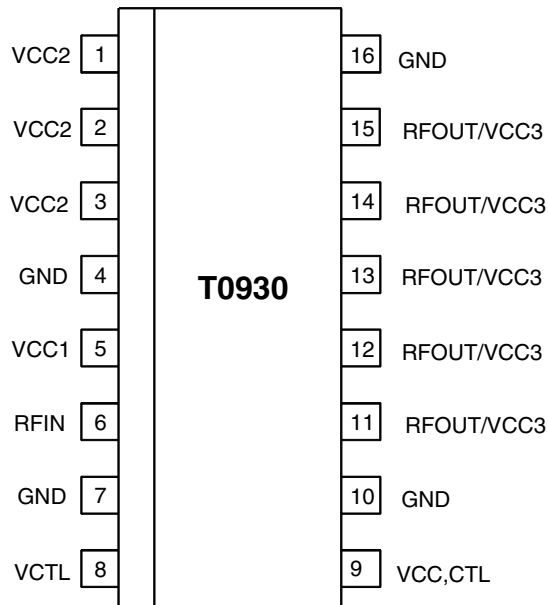
SiGe Power Amplifier for CW Applications

T0930



Pin Configuration

Figure 2. Pinning PSSOP16



Pin Description

Pin	Symbol	Function
1	VCC2	Supply voltage 2
2	VCC2	Supply voltage 2
3	VCC2	Supply voltage 2
4	GND	Ground
5	VCC1	Supply voltage 1
6	RFIN	RF input
7	GND	Ground (control)
8	VCTL	Control input
9	VCC,CTL	Supply voltage for control
10	GND	Ground (optional)
11	RFOUT/VCC3	RF output/supply voltage 3
12	RFOUT/VCC3	RF output/supply voltage 3
13	RFOUT/VCC3	RF output/supply voltage 3
14	RFOUT/VCC3	RF output/supply voltage 3
15	RFOUT/VCC3	RF output/harmonic tuning
16	GND	Ground

Absolute Maximum Ratings

All voltages refer to GND

Parameters	Symbol	Min.	Max.	Unit
Supply voltage V_{CC} at $V_{CTL} = 1.7$ V, Pin 5 Pin 1, 2, 3 Pins 11, 12, 13, 14 and 15 Pin 9	V_{CC1} V_{CC2} V_{CC3} $V_{CC, CTL}$		4 4 4 4	V
Input power, Pin 6	P_{in}		12	dBm
Gain control voltage ⁽¹⁾ , Pin 8	V_{CTL}	0	2	V
Duty cycle for operation			100	%
Junction temperature	T_j		+150	°C
Storage temperature	T_{stg}	-40	+150	°C

Note: 1. The gain control voltage should always be 0.2 V below the supply voltage. RF should be applied before ramp-up.

Operating Range

All voltages referred to GND

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage $V_{CC}^{(1)}$ 1 W application	$V_{CC1}, V_{CC2}, V_{CC3},$ $V_{CC, CTL}$	1.8	2.4	3	V
Supply voltage $V_{CC}^{(1)}$ 2 W application	$V_{CC1}, V_{CC2}, V_{CC3},$ $V_{CC, CTL}$	2.6	3.2	3.6	V
Ambient temperature	T_{amb}	-25		+85	°C
Input frequency	f_{in}		900		MHz

Note: 1. The gain control voltage should be always 0.2 V below the supply voltage. RF should be applied before ramp-up.

Electrical Characteristics for 1 W Application

$V_{CC} = V_{CC1}, \dots, V_{CC3}, V_{CC, CTL} = +2.4 \text{ V}, V_{CTL} = 1.7 \text{ V}, T_{amb} = +25^\circ\text{C}$, 50- Ω input and 50- Ω external output match

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Power Supply								
1.1	Supply voltage			V_{CC}	1.8	2.4	3.0	V	A
1.2	Current consumption in active mode	$P_{out} = 30 \text{ dBm}$ $PAE = 47\%$		I		0.9		A	A
1.3	Current consumption (leakage current) in power-down mode	$V_{CTL} \leq 0.2 \text{ V}$		I			10	μA	A
2	RF Input								
2.1	Frequency range			f_{in}	880	900	935	MHz	A
2.2	Input impedance ⁽¹⁾			Z_i		50		Ω	C
2.3	Input power			P_{in}		5	12	dBm	C
2.4	Input VSWR ⁽¹⁾	$P_{in} = 0 \text{ to } 12 \text{ dBm}$ $P_{out} = 30 \text{ dBm}$					2:1		C
3	RF Output								
3.1	Output impedance ⁽¹⁾			Z_o		50		Ω	C
3.2	Output power in normal conditions	$P_{in} = 5 \text{ dBm}$ $R_L = R_G = 50 \Omega$ $V_{CC} = 2.4 \text{ V}, T_{amb} = +25^\circ\text{C}$ $V_{CC} = 1.8 \text{ V}, T_{amb} = +25^\circ\text{C}$		P_{out} P_{out}		30 27		dBm dBm	A
3.3	Minimum output power	$V_{CTL} = 0.3 \text{ V}$				-20		dBm	A
3.4	Power-added efficiency	$V_{CC} = 2.4 \text{ V}, P_{out} = 27 \text{ dBm}$ $V_{CC} = 2.4 \text{ V}, P_{out} = 30 \text{ dBm}$		PAE PAE		40 47		% %	A
3.5	Stability	Temp = -25 to +85°C no spurious $\geq -60 \text{ dBc}$		VSWR			10:1		C
3.6	Load mismatch (stable, no damage)	$P_{out} = 30 \text{ dBm}$, all phases		VSWR			10:1		C
3.7	Second harmonic distortion			2fo			-35	dBc	A
3.8	Third harmonic distortion			3fo			-35	dBc	A
3.9	Noise power $f = 925 \text{ to } 935 \text{ MHz}$ $f \geq 935 \text{ MHz}$	$P_{out} = 30 \text{ dBm}$ RBW = 100 kHz				-73 -85	-70 -82	dBm dBm	C
3.10	Rise and fall time						0.5	ms	A
3.11	Isolation between input and output	$P_{in} = 0 \text{ to } 10 \text{ dBm}$ $V_{CTL} \leq 0.2 \text{ V}$ (power down)			50			dB	C
4	Power Control								
4.1	Control curve	$P_{out} \geq 25 \text{ dBm}$					150	dB/V	C
4.2	Power control range	$V_{CTL} = 0.3 \text{ to } 2.0 \text{ V}$			50			dB	C
4.3	Control voltage range			V_{CTL}	0.3		2.0	V	A
4.4	Control current	$P_{in} = 0 \text{ to } 10 \text{ dBm}, V_{CTL} = 0 \text{ to } 2.0 \text{ V}$		I_{CTL}			200	μA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. With external matching (see "Application Circuit").

Electrical Characteristics for 2 W Application

$V_{CC} = V_{CC1}, \dots, V_{CC3}, V_{CC, CTL} = +3.2 \text{ V}, V_{CTL} = 1.9 \text{ V}, T_{amb} = +25^\circ\text{C}$, 50- Ω input and 50- Ω external output match

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	Power Supply								
5.1	Supply voltage			V_{CC}	2.6	3.2	3.6	V	A
5.2	Current consumption in active mode	$P_{out} = 33 \text{ dBm}$ $PAE = 47\%$		I		1.33		A	A
5.3	Current consumption (leakage current) in power-down mode	$V_{CTL} \leq 0.2 \text{ V}$		I			10	μA	A
6	RF Input								
6.1	Frequency range			f_{in}	880	900	935	MHz	A
6.2	Input impedance ⁽¹⁾			Z_i		50		Ω	C
6.3	Input power			P_{in}		5	12	dBm	C
6.4	Input VSWR ⁽¹⁾	$P_{in} = 0 \text{ to } 12 \text{ dBm}$ $P_{out} = 30 \text{ dBm}$					2:1		C
7	RF Output								
7.1	Output impedance ⁽¹⁾			Z_o		50		Ω	C
7.2	Output power in normal conditions	$P_{in} = 5 \text{ dBm}, R_L = R_G = 50 \Omega$ $V_{CC} = 3.2 \text{ V}, T_{amb} = +25^\circ\text{C}$ $V_{CC} = 2.2 \text{ V}, T_{amb} = +25^\circ\text{C}$		P_{out} P_{out}		33 30		dBm dBm	A
7.3	Minimum output power	$V_{CTL} = 0.3 \text{ V}$				-20		dBm	A
7.4	Power-added efficiency	$V_{CC} = 3.2 \text{ V}, P_{out} = 27 \text{ dBm}$		PAE		47		%	A
7.5	Stability	Temp = -25 to +85°C no spurious $\geq -60 \text{ dBc}$		VSWR			10:1		C
7.6	Load mismatch (stable, no damage)	$P_{out} = 33 \text{ dBm}$, all phases		VSWR			10:1		C
7.7	Second harmonic distortion			2fo			-35	dBc	A
7.8	Third harmonic distortion			3fo			-35	dBc	A
7.9	Noise power $f = 925 \text{ to } 935 \text{ MHz}$ $f \geq 935 \text{ MHz}$	$P_{out} = 33 \text{ dBm}$ RBW = 100 kHz				-73 -85	-70 -82	dBm dBm	C
7.10	Rise and fall time						0.5	μs	A
7.11	Isolation between input and output	$P_{in} = 0 \text{ to } 10 \text{ dBm}$ $V_{CTL} \leq 0.2 \text{ V}$ (power down)			50			dB	C
8	Power Control								
8.1	Control curve	$P_{out} \geq 25 \text{ dBm}$					150	dB/V	C
8.2	Power control range	$V_{CTL} = 0.3 \text{ to } 2.0 \text{ V}$			50			dB	C
8.3	Control voltage range			V_{CTL}	0.3		2.0	V	A
8.4	Control current	$P_{in} = 0 \text{ to } 10 \text{ dBm}, V_{CTL} = 0 \text{ to } 2.0 \text{ V}$		I_{CTL}			200	μA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. With external matching (see "Application Circuit").

Figure 3. P_{out} and PAE versus V_{CC} (1 W Application)

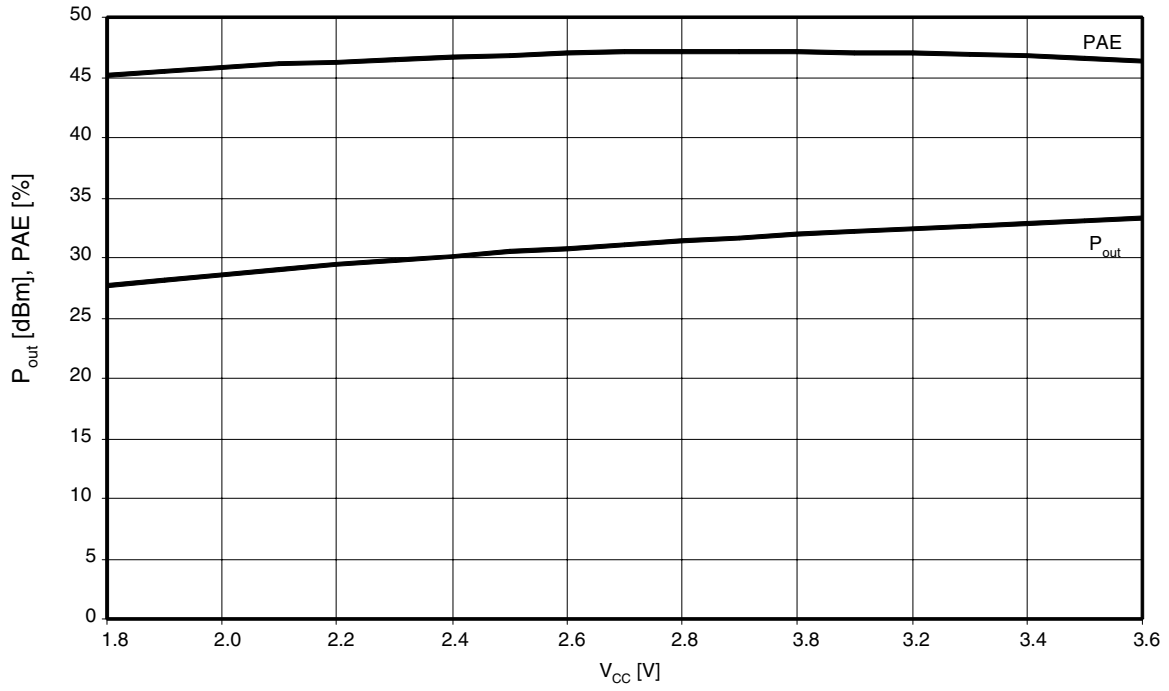


Figure 4. P_{out} and PAE versus V_{ramp} (1 W Application)

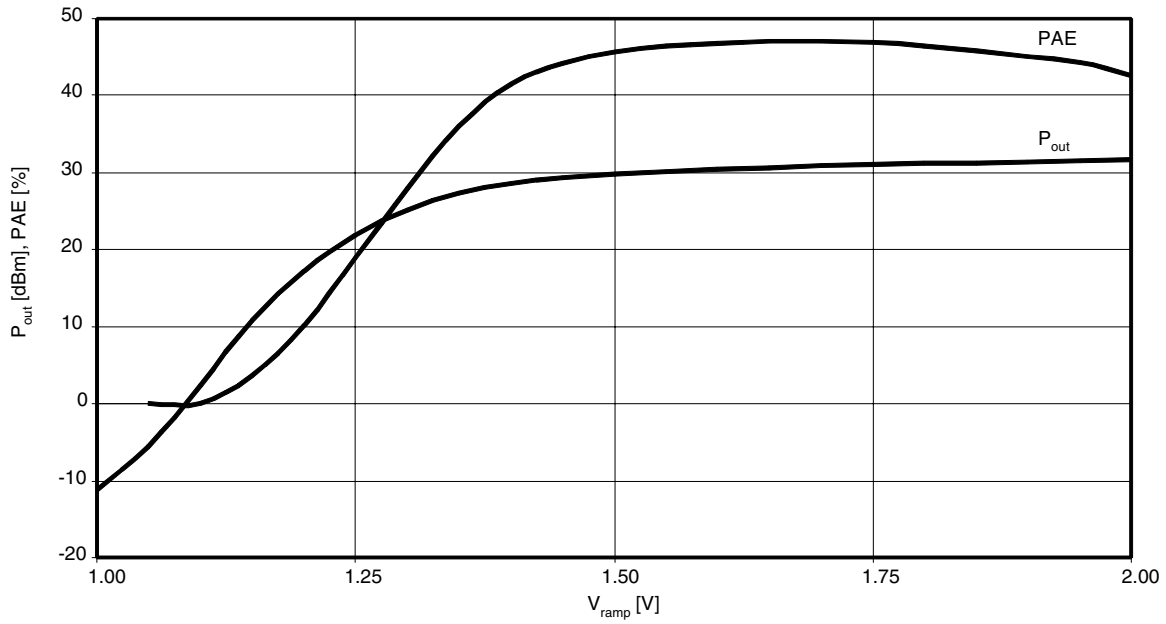


Figure 5. P_{out} and PAE versus V_{CC} (2 W Application)

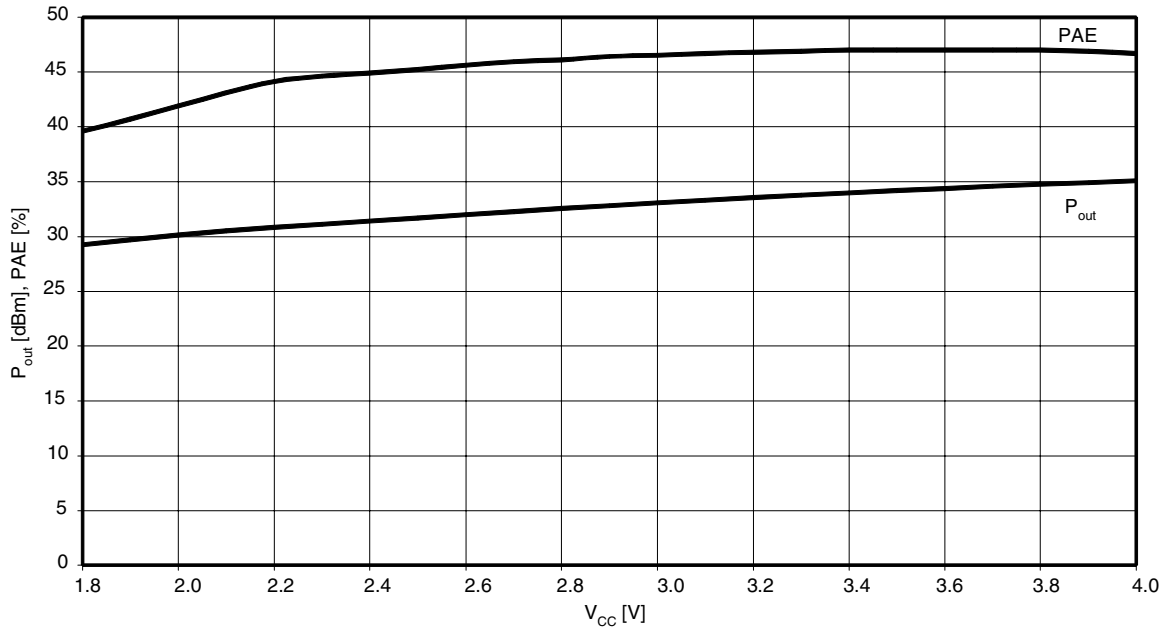
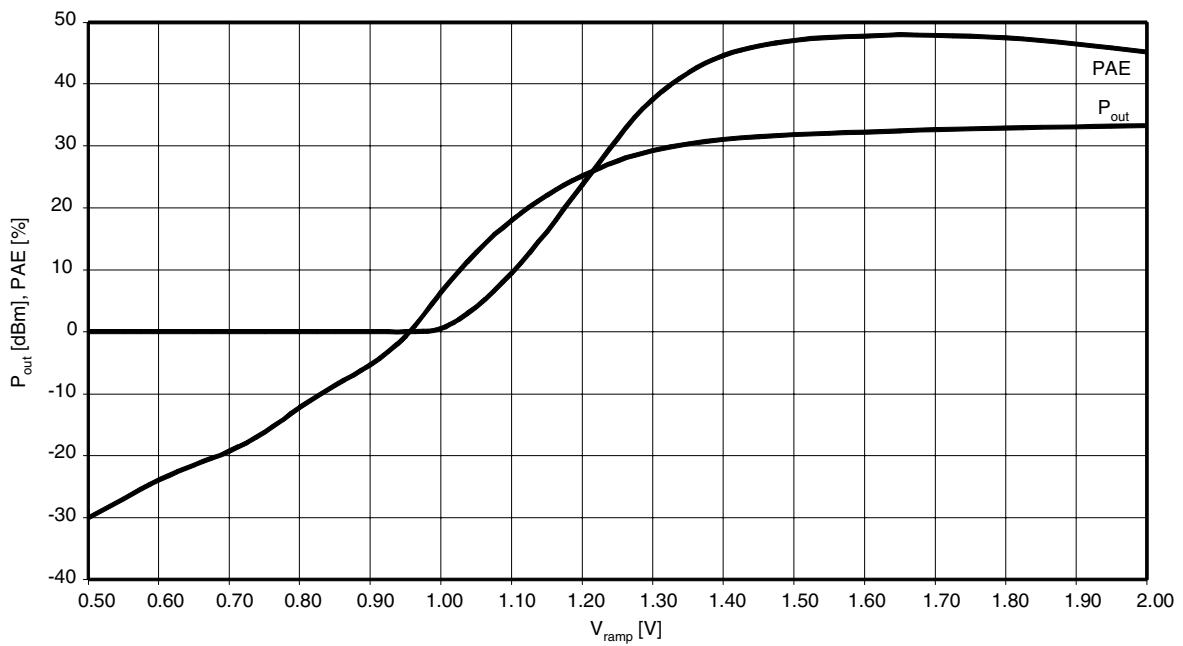
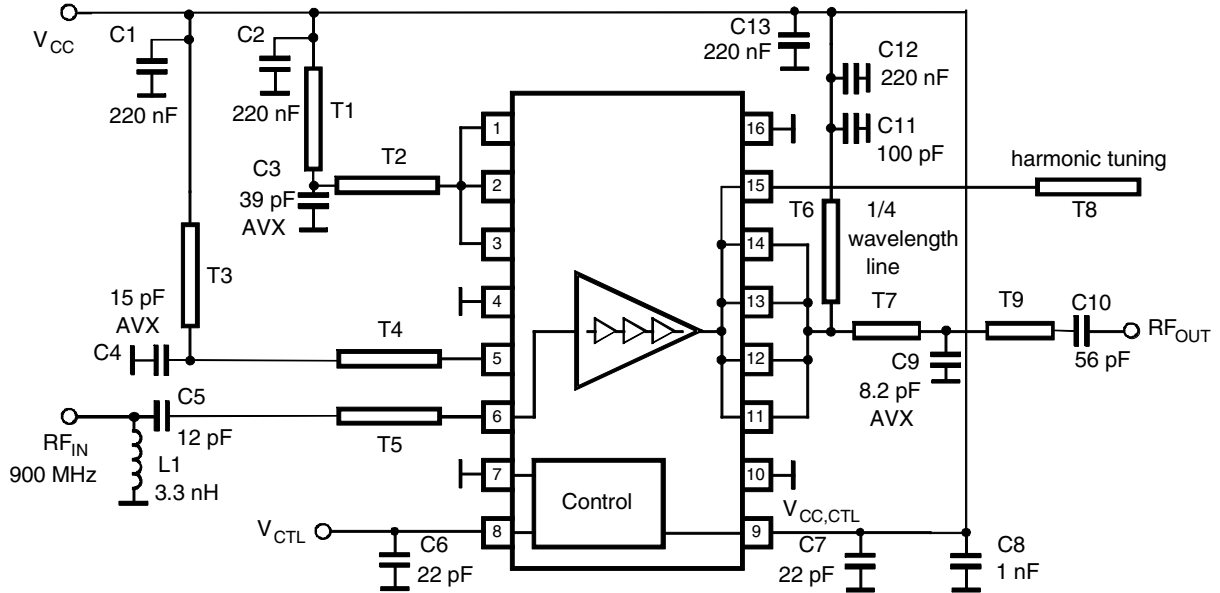


Figure 6. P_{out} and PAE versus V_{ramp} (2 W Application)



Application Circuit

Figure 7. Application Circuit GSM Pager (900 MHz)



Microstrip line : FR4 ; Epsilon(r) : 4.3 ; metal Cu : 35 μ m
 distance 1. layer -rf ground : 0.5 mm

	l/mm	x	w/mm		l/mm	x	w/mm
T1	20.5	x	1.0	T6	43.1	x	0.5
T2	1.3	x	1.0	T7	6.0	x	1.25
T3	14.8	x	0.5	T8	10.0	x	0.5
T4	14.2	x	0.5	T9	4.0	x	1.25
T5	2.5	x	1.0				

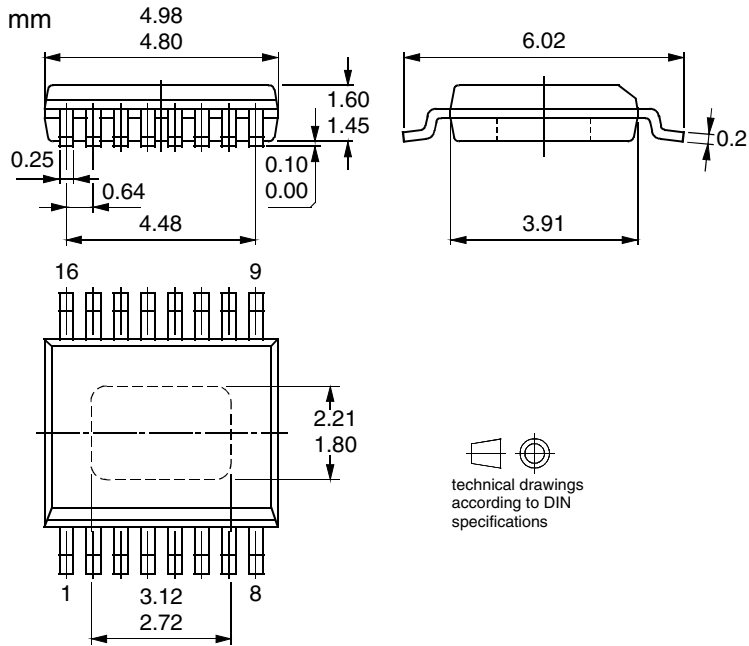
Ordering Information

Extended Type Number	Package	Remarks
T0930-TJT	PSSOP16	Tube
T0930-TJQ	PSSOP16	Taped and reeled

Package Information

Package PSSOP16

Dimensions in mm





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