



P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

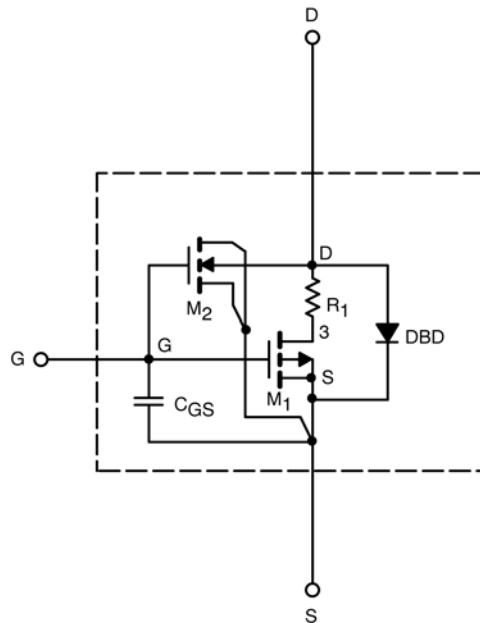
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	0.80		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} = -4.5V	191		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5V, I _D = -1 A	0.0184	0.0174	Ω
		V _{GS} = -2.5V, I _D = -1 A	0.0211	0.0214	
		V _{GS} = -1.8V, I _D = -1 A	0.0252	0.0270	
Forward Transconductance ^a	g _{fs}	V _{DS} = -4V, I _D = -1 A	20	8.3	S
Diode Forward Voltage ^a	V _{SD}	I _S = -1A, V _{GS} = 0 V	-0.78	-0.80	V
Dynamic^b					
Input Capacitance	C _{iss}	V _{DS} = -6 V, V _{GS} = 0 V, f = 1 MHz	3228	2220	pF
Output Capacitance	C _{oss}		913	865	
Reverse Transfer Capacitance	C _{rss}		542	555	
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -5 V, I _D = -1 A	25	38	nC
		V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -1 A	23	35	
Q _{gs}	7.3		7.3		
Gate-Drain Charge	Q _{gd}		5.9	5.9	

Notes

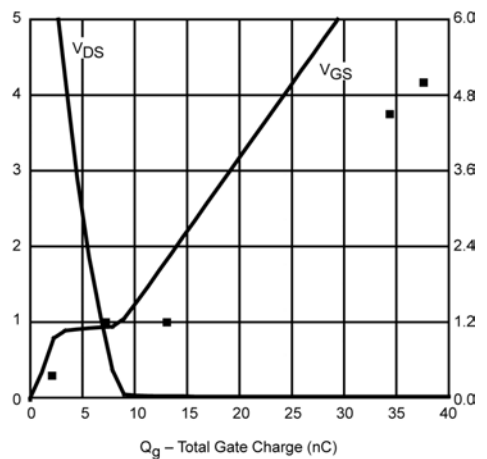
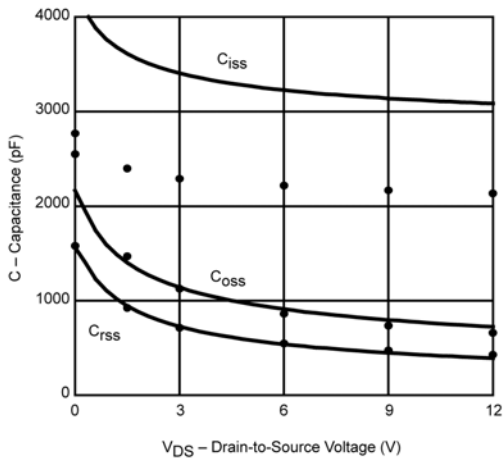
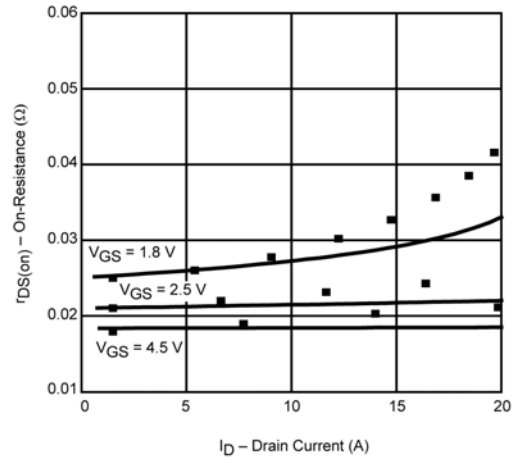
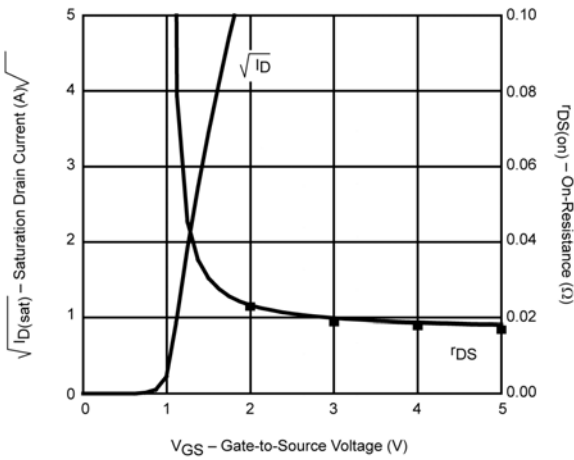
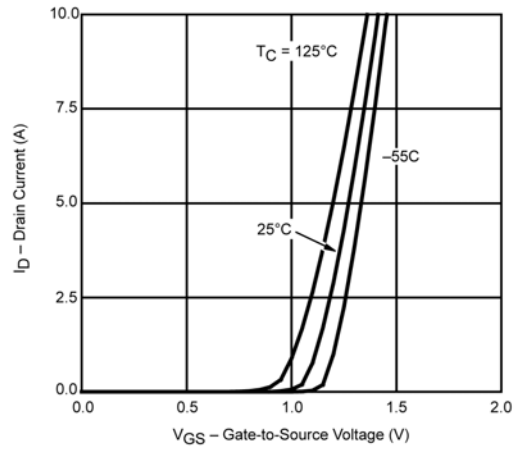
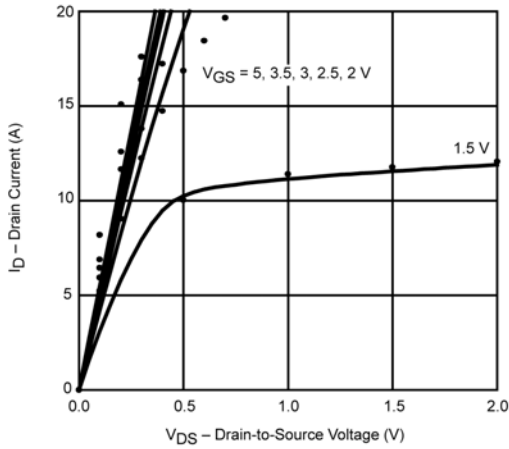
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si8417DB

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.