32Mbyte(8Mx32) EDO Mode 4K Ref. 100Pin SMM, 5V Design

Part No. HMD8M32F4E

GENERAL DESCRIPTION

The HMD8M32F4E is a 8M x 32bit dynamic RAM high density memory module. The module consists of four CMOS 4M x 16 bit DRAMs in 50-pin TSOP packages mounted on a 100-pin, double-sided, FR-4-printed circuit board. A 0.1uF or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM components.
The module is a single In-line memory module with edge connections and is intended for mounting in to 100-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Access times : 50, 60ns
- High-density 32MByte design
- Single +5V ± 0.5V power supply
- JEDEC Standard pinout
- EDO mode operation
- TTL compatible inputs and outputs
- FR4-PCB design

OPTIONS **MARKING**

- Timing
  - 50ns access -5
  - 60ns access -6
- Packages
  - 100-pin SMM F

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
5	50ns	13ns	90ns	26ns
6	60ns	15ns	110ns	30ns

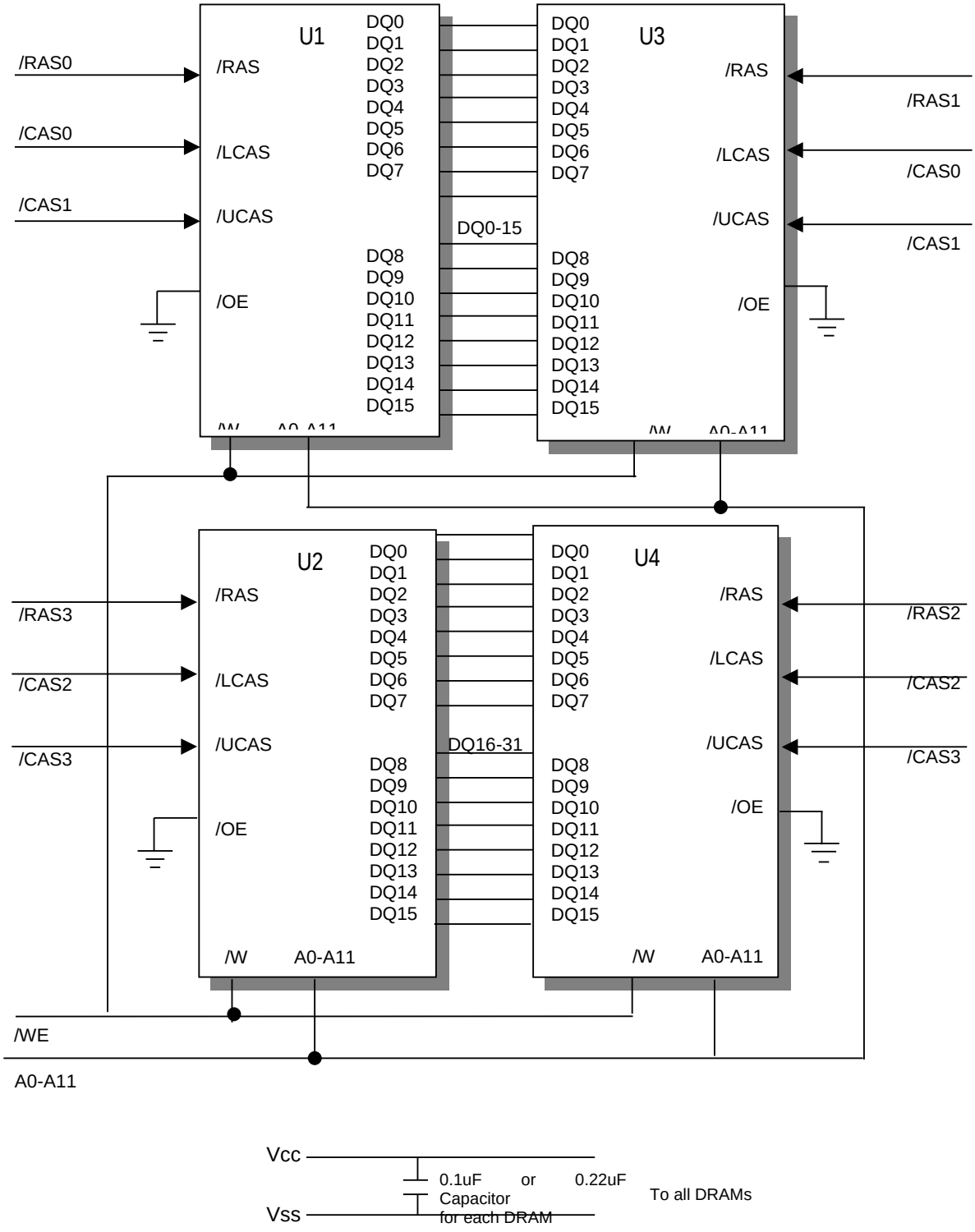
PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	26	Vcc	51	Vcc	76	Vcc
2	NC	27	/CAS0	52	NC	77	/CAS2
3	/RAS0	28	/CAS1	53	/RAS2	78	/CAS3
4	/RAS1	29	NC	54	/RAS3	79	DQ22
5	DQ15	30	NC	55	DQ31	80	DQ21
6	DQ14	31	NC	56	DQ30	81	DQ20
7	DQ13	32	NC	57	DQ29	82	DQ19
8	Vss	33	Vss	58	Vss	83	Vss
9	DQ12	34	NC	59	NC	84	DQ18
10	DQ11	35	NC	60	/WE	85	DQ17
11	DQ10	36	DQ9	61	NC	86	DQ16
12	DQ8	37	DQ7	62	NC	87	NC
13	Vss	38	Vss	63	Vss	88	Vss
14	DQ6	39	DQ5	64	NC	89	NC
15	DQ4	40	NC	65	NC	90	NC
16	DQ3	41	A11	66	DQ28	91	NC
17	DQ2	42	A10	67	DQ27	92	NC
18	Vss	43	Vss	68	Vss	93	Vss
19	DQ1	44	A9	69	DQ26	94	NC
20	DQ0	45	A8	70	DQ25	95	Vss
21	A0	46	A7	71	DQ24	96	NC
22	A1	47	A6	72	DQ23	97	NC
23	A2	48	A5	73	Vss	98	Vss
24	A3	49	A4	74	NC	99	NC
25	Vcc	50	Vcc	75	Vcc	100	Vcc

100PIN SMM

TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	4W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	816	mA
	-6	-	736	mA
I_{CC2}	Don't care	-	32	mA
I_{CC3}	-5	-	816	mA
	-6	-	736	mA
I_{CC4}	-5	-	896	mA
	-6	-	816	mA
I_{CC5}	Don't care	-	16	mA
I_{CC6}	-5	-	816	mA
	-6	-	736	mA
$I_{I(L)}$		-80	80	μA
$I_{O(L)}$		-10	10	μA
V_{OH}		2.4 -	- 0.4	V V
V_{OL}				

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V

V_{OH} : Output High Voltage Level (I_{OH}= -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	C_{IN1}	-	100	pF
Input Capacitance (/WE)	C_{IN2}	-	130	pF
Input Capacitance (/RAS0-/RAS3)	C_{IN3}	-	40	pF
Input Capacitance (/CAS0-/CAS3)	C_{IN4}	-	30	pF
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	20	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

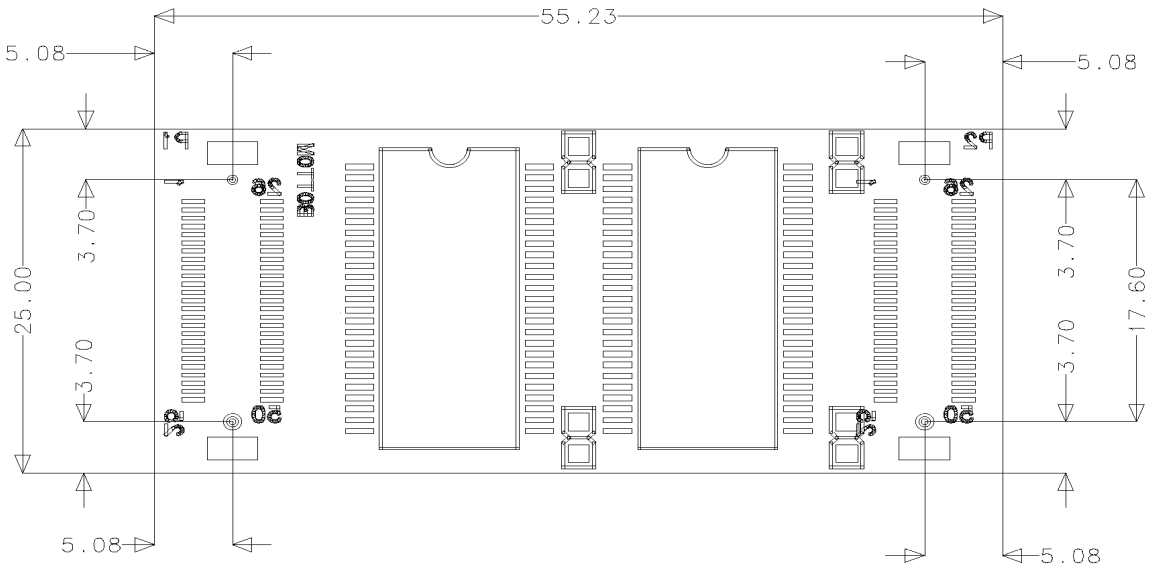
STANDARD OPERATION	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	90		110		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	3		3		ns
Output buffer turn-off delay	t_{OFF}	3	13	3	13	ns
Transition time (rise and fall)	t_T	2	50	2	50	ns
/RAS precharge time	t_{RP}	30			40	ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13			15	ns
/CAS hold time	t_{CSH}	38			45	ns
/CAS pulse width	t_{CAS}	8	10K	10	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	37	20	45	ns
/RAS to column address delay time	t_{RAD}	15	25	15	30	ns
/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns

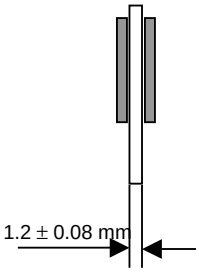
Column address hold time	t_{CAH}	8		10		ns
Column Address to /RAS lead time	t_{RAL}	25		30		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	10		10		ns
Write command hold referenced to /RAS	t_{WCR}	50		55		ns
Write command pulse width	t_{WP}	10		10		ns
Write command to /RAS lead time	t_{RWL}	13		10		ns
Write command to /CAS lead time	t_{CWL}	8		10		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	8		10		ns
Refresh period	t_{REF}		64		64	ns
Write command set-up time	t_{WCS}	0		0		ns
/CAS setup time (C-B-R refresh)	t_{CSR}	5		5		ns
/CAS hold time (C-B-R refresh)	t_{CHR}	10		10		ns
/RAS precharge to /CAS hold time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		30		35	ns
/CAS precharge time (Fast page)	t_{CP}	8		10		ns
/RAS pulse width (Fast page)	t_{RASP}	50	200K	60	200K	ns
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10		10		ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		10		ns

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. $V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.

PACKAGING INFORMATION





ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD8M32F4E- 5	32MByte	x 32	100 Pin-SMM	4EA	5.0V	EDO	50ns
HMD8M32F4E- 6	32MByte	x 32	100 Pin-SMM	4EA	5.0V	EDO	60ns