

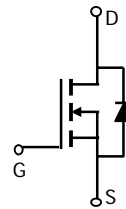
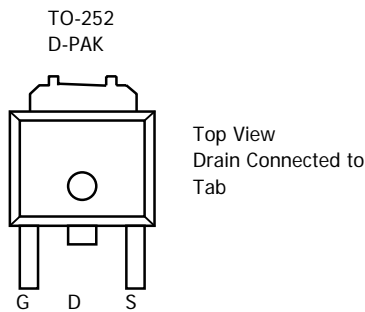
**AOD488**  
**N-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AOD488 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. *Standard Product AOD488 is Pb-free (meets ROHS & Sony 259 specifications). AOD488L is a Green Product ordering option. AOD488 and AOD488L are electrically identical.*

**Features**

$V_{DS}$  (V) = 40V  
 $I_D$  = 20 A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 26 m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 39 m $\Omega$  ( $V_{GS}$  = 4.5V)


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	15
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	50	A
Avalanche Current <sup>C</sup>	$I_{AR}$	12	A
Repetitive avalanche energy $L=0.3\text{mH}$ <sup>C</sup>	$E_{AR}$	22	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	10
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.3
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	17.4	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	40	45		V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			0.1	uA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	2.3	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	50			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		21.5	26	mΩ
		T <sub>J</sub> =125°C		34	41	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		31	39	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		25		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.76	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz		404	500	pF
C <sub>oss</sub>	Output Capacitance			95		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			37		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		2.7	4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		9.2	12	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			4.5		nC
Q <sub>gs</sub>	Gate Source Charge			1.6		nC
Q <sub>gd</sub>	Gate Drain Charge			2.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =1.0Ω, R <sub>GEN</sub> =3Ω		3.5		ns
t <sub>r</sub>	Turn-On Rise Time			6		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			13.2		ns
t <sub>f</sub>	Turn-Off Fall Time			3.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =20A, dI/dt=100A/μs		22.9	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=100A/μs		18.3		nC

A: The value of R<sub>qJA</sub> is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>thJA</sub> and the maximum allowed junction temperature of 150 °C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175 °C may be used if the PCB allows it.

B: The power dissipation PD is based on T<sub>J</sub>(MAX)=175 °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=175 °C.

D: The R<sub>qJA</sub> is the sum of the thermal impedance from junction to case R<sub>qJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

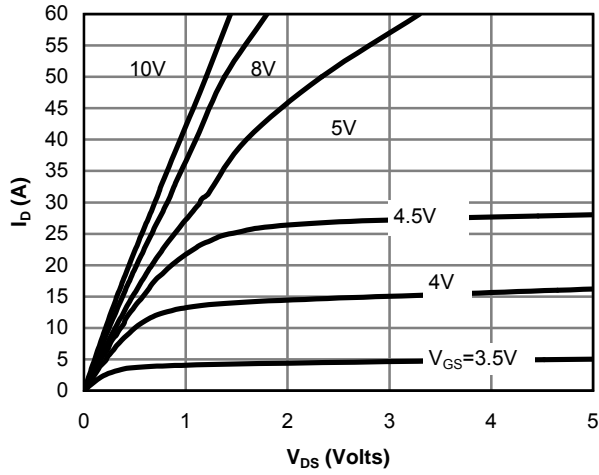
F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J</sub>(MAX)=175 °C.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25 °C. The SOA curve provides a single pulse rating.

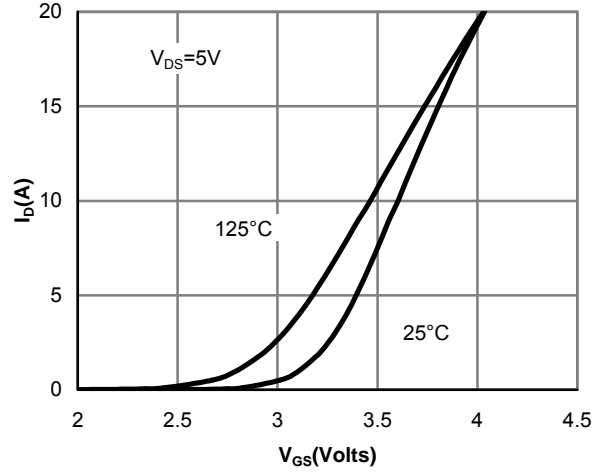
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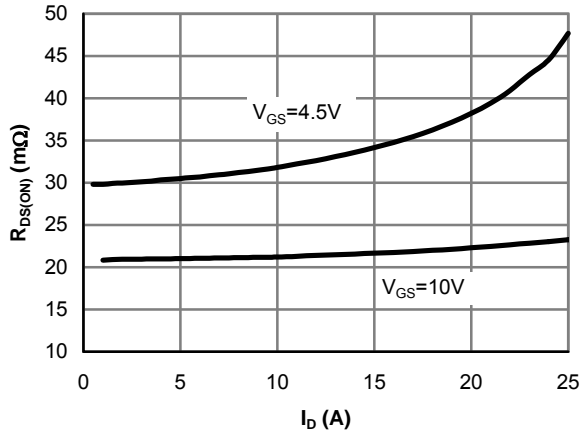
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



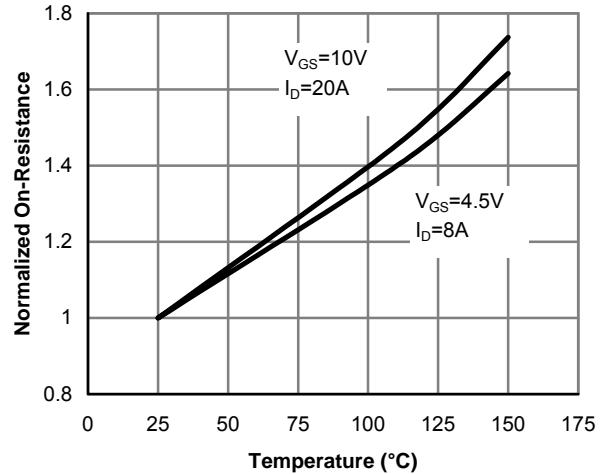
**Fig 1: On-Region Characteristics**



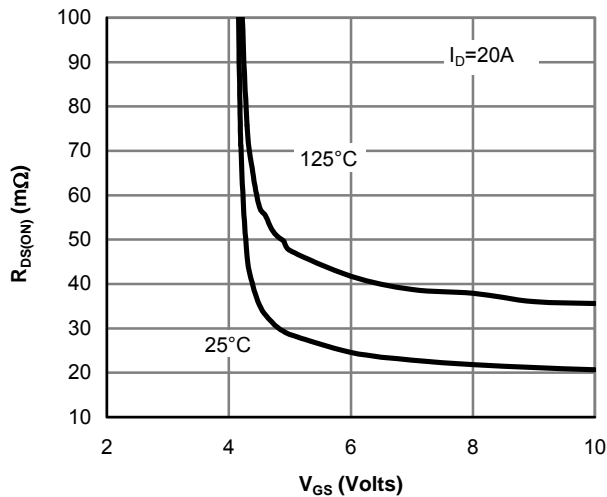
**Figure 2: Transfer Characteristics**



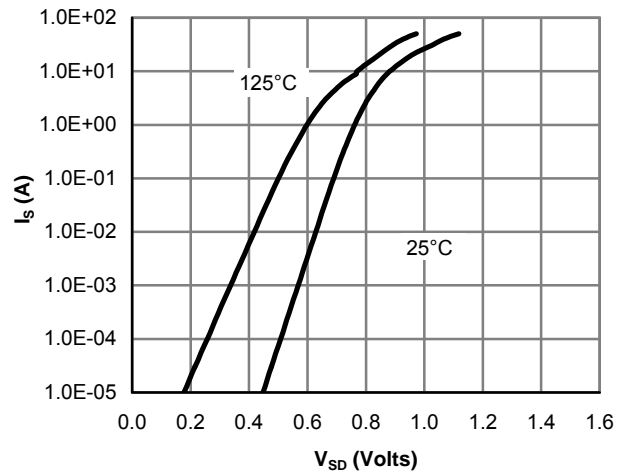
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

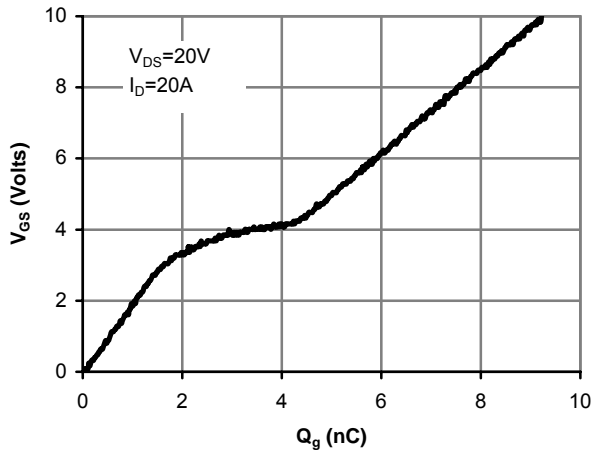


Figure 7: Gate-Charge Characteristics

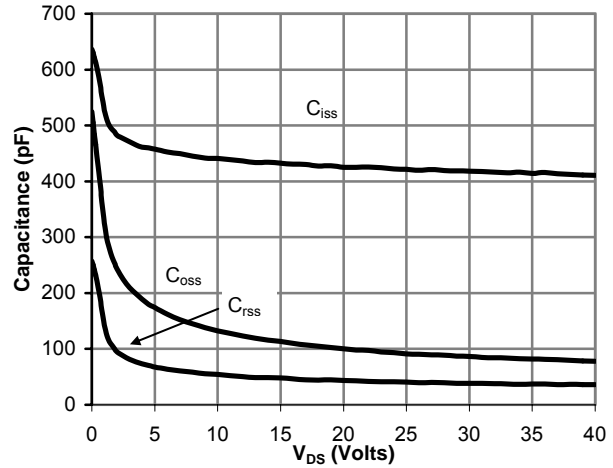


Figure 8: Capacitance Characteristics

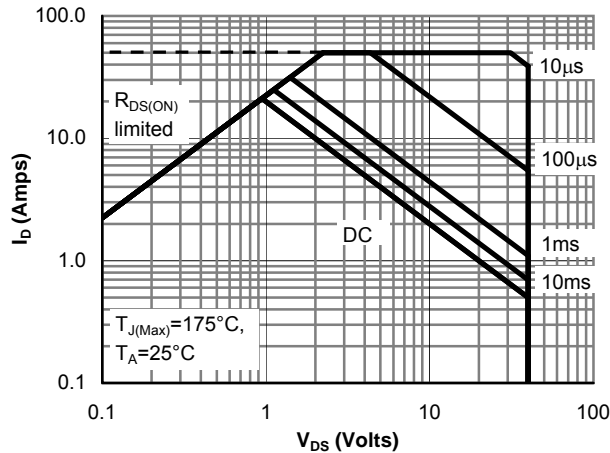


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

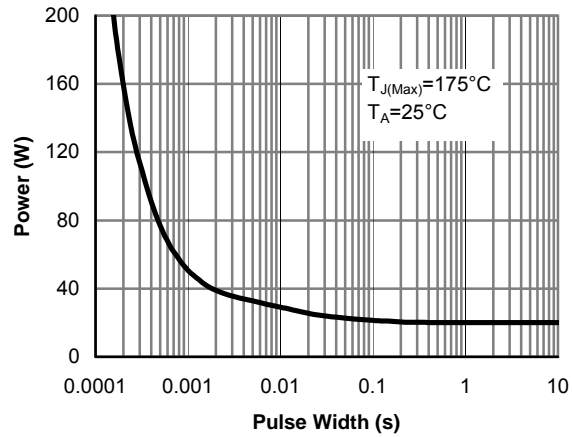


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

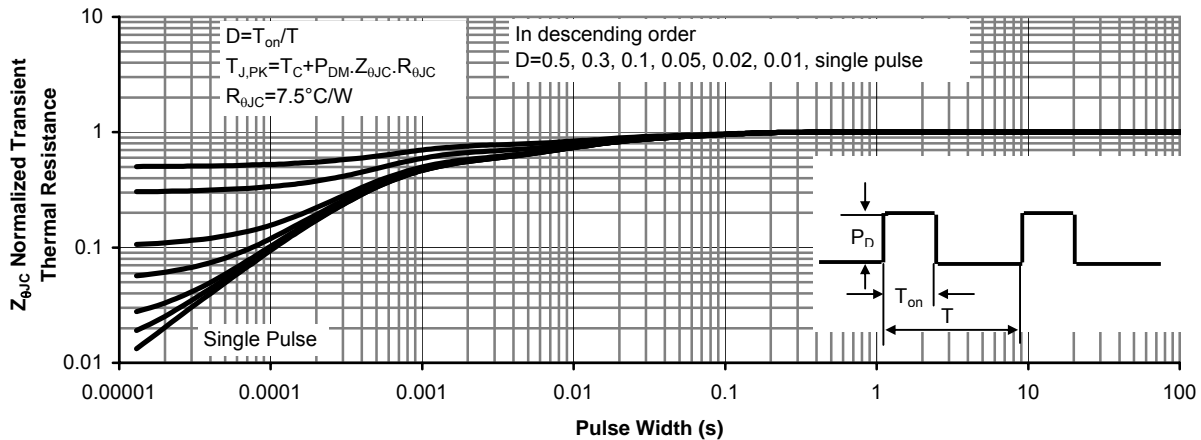


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

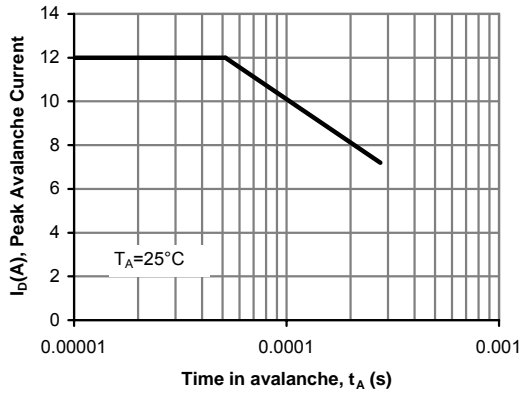


Figure 12: Single Pulse Avalanche capability

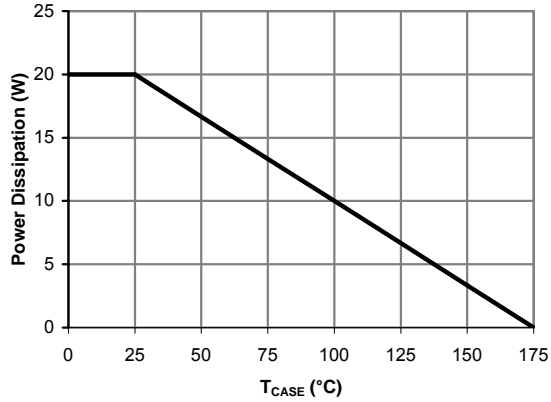


Figure 13: Power De-rating (Note B)

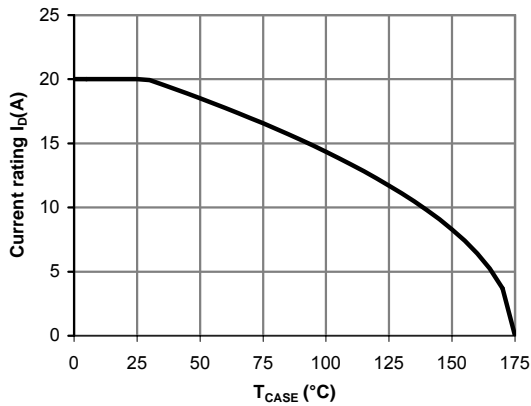


Figure 14: Current De-rating (Note B)

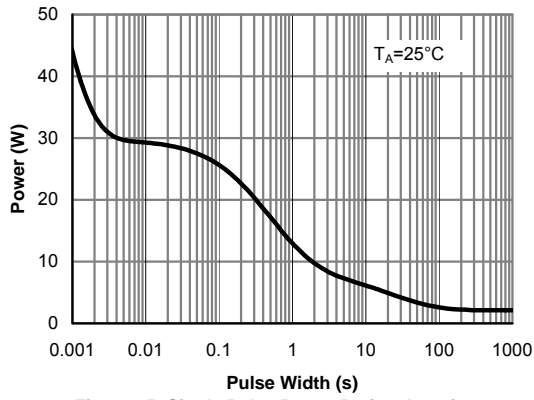


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

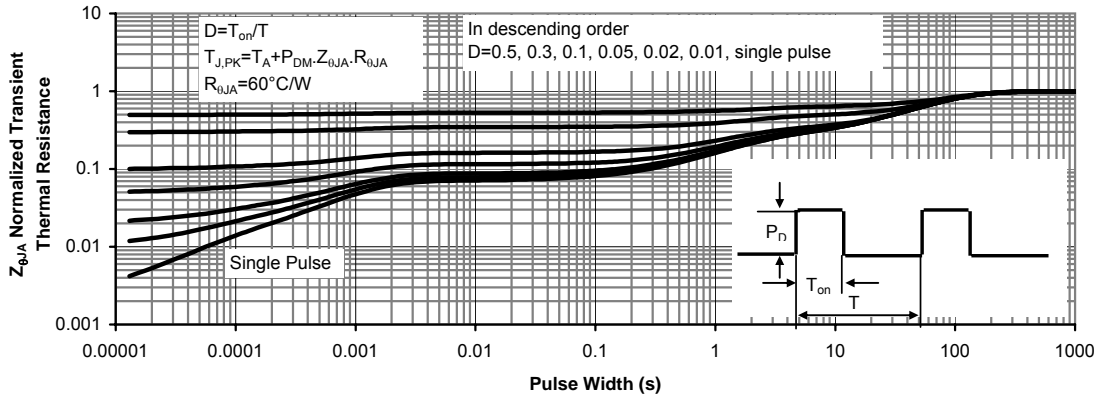


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)