

Product Features

- R_{ON} is 35 ohms max.
- Standard Operating Temperature: 0°C to +70°C
- Channel ON Capacitance: 15pF max.
- V_{CC} Operating Range: +3.0V to +3.6V
- Fast switching time: 3ns max.
- Package options include:
 - 64-ball Thin Fine Pitch Ball Grid Array (TFBGA)

Applications

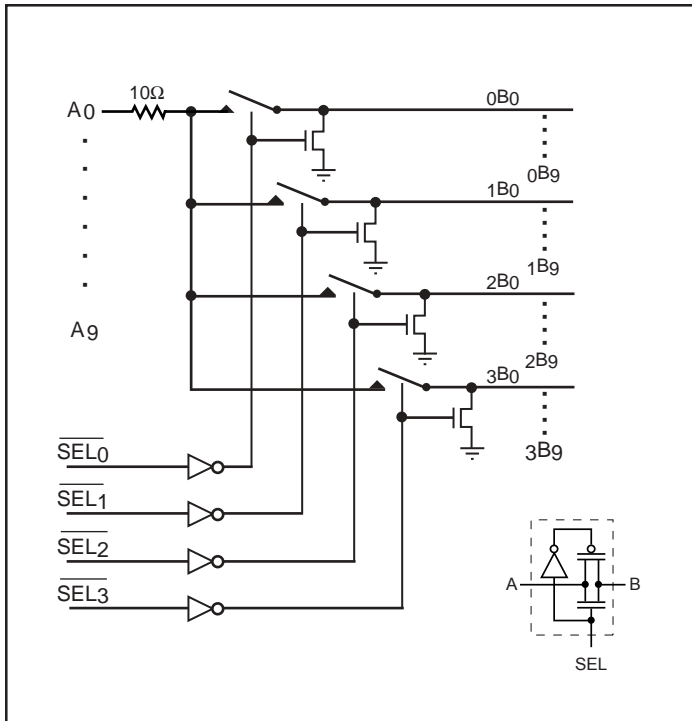
- DDR DIMM bank switching

Product Description

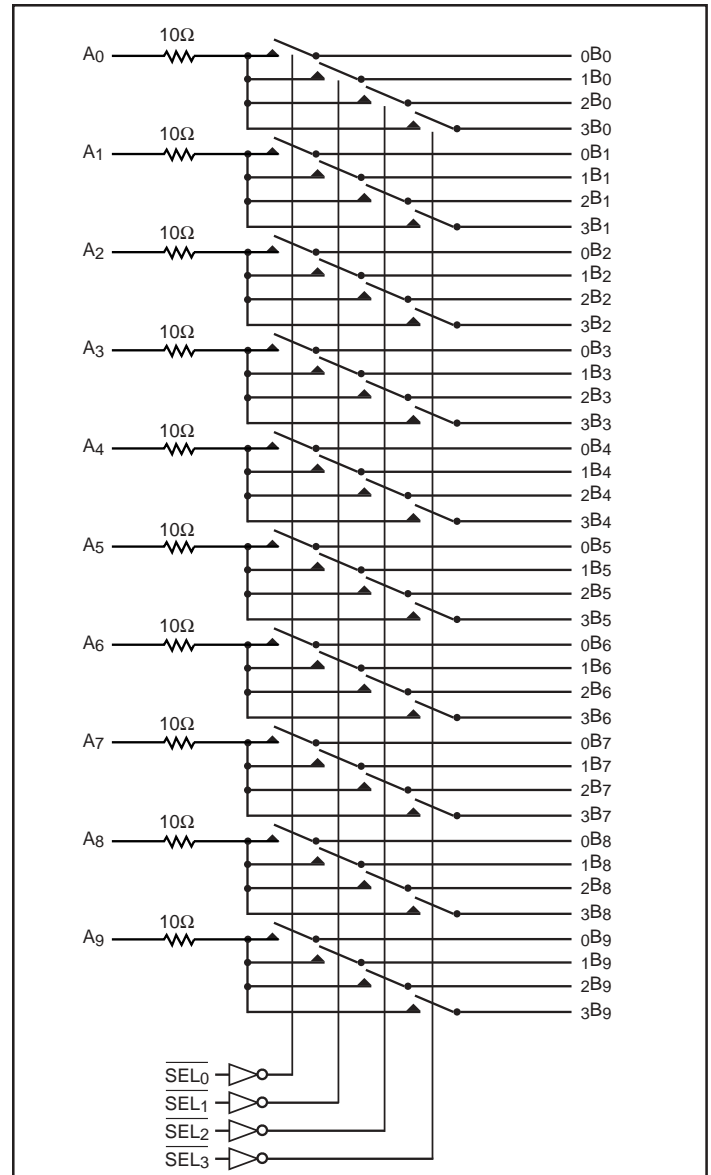
Pericom Semiconductor's PI3B series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry-leading performance.

The PI3B4010 is a 3.3V, 10- to 40-bit demultiplexing/multiplexing bus switch. It is intended for multiple data or address muxing. Industry leading advantages include a propagation delay of 300ps, resulting from the 35-ohm channel resistance, and low I/O capacitance. The A-port multiplexes to one of four or all outputs allowing a complete bank of 10 bits to switch. The switch is bidirectional.

Logic Block Diagram



Expanded Block Diagram



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Supply Voltage Range	-0.5V to +4.6V
DC Input Voltage	-0.5V to +4.6V
DC Output Current	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Product Pinout by Location on Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SEL ₁	V _{DD}		1B ₀	2B ₀	3B ₀		2B ₁	3B ₁	0B ₂
B	SEL ₂	NC	SEL ₀	GND	0B ₀	A ₀	0B ₁	1B ₁	A ₁	GND	1B ₂
C	V _{DD}	SEL ₃								A ₂	2B ₂
D		GND								3B ₂	
E	2B ₉	3B ₉								0B ₃	1B ₃
F	1B ₉	A ₉								A ₃	2B ₃
G	0B ₉	3B ₈								GND	3B ₃
H		2B ₈								0B ₄	
J	1B ₈	A ₈								A ₄	1B ₄
K	0B ₈	GND								A ₇	0B ₇
L	3B ₇	2B ₇	1B ₇		2B ₆	1B ₆	0B ₆		2B ₅	1B ₅	0B ₅

Top View

NC = No Connection

Product Pin Description

Pin Name	Description
A _N	Demux Input Pins
NB ₀ - NB ₉	Mux Input Pins
SEL _N	Bank Select Pins (Active LOW)
GND	Ground
V _{DD}	Power

Note: N = 0 through 3 for each set of 10 Bits

Truth Table

Function	SEL ₀	SEL ₁	SEL ₂	SEL ₃
Connect A _N to 0B _N	L	H	H	H
Connect A _N to 1B _N	H	L	H	H
Connect A _N to 2B _N	H	H	L	H
Connect A _N to 3B _N	H	H	H	L
0B _N , 1B _N , 2B _N , 3B _N = Pulldown, A _N = Hi-Z	H	H	H	H

DC Electrical Characteristics over Operating Range ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Level	1.6	–	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage	Guaranteed HIGH Level	–0.3	–	0.9	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Max.}, V_{IN} = -18\text{mA}$	–	–0.7	–1.2	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$	–	–	± 10	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$	–	–	± 10	
R_{ON}	Switch On Resistance ⁽³⁾	$V_{CC} = \text{Min.}, 0.8\text{V} \leq V_{IN} \leq 2.5\text{V}, I_{IN} = -20\text{mA}$	–	25	35	Ω
$R_{FLAT(ON)}$	On Resistance Flatness ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN@0.8\text{V}} \text{ and } 1.7\text{V}, I_{IN} = -20\text{mA}$	–	1.0	–	
ΔR_{ON}	On Resistance match from center ports to any other port ⁽⁴⁾	$V_{CC} = \text{Min.}, 0.8\text{V} \leq V_{IN} \leq 2.5\text{V}, I_{IN} = -20\text{mA}$	–	0.9	2	
R_{PD}	Pull-Down Resistance	$V_{IN} = 0\text{V}$ to 2.5V	80	100	130	

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameters	Description	Test Conditions	Typ. ⁽⁴⁾	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	3.5	–	pF
$C_{OFF(A)}$	Port A Capacitance, Switch OFF		12.0	–	
$C_{ON(A/B)}$	A/B Capacitance, Switch ON		15.0	–	
$C_{OFF(B)}$	Port B Capacitance, Switch OFF		4.5	–	

Notes:

1. For min. or max. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
3. Measured by the voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A & B) pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	–	–	10	μA

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^\circ\text{C}$ ambient.
3. Per TTL driven input (control inputs only); A and B pins do not contribute to I_{CC} .

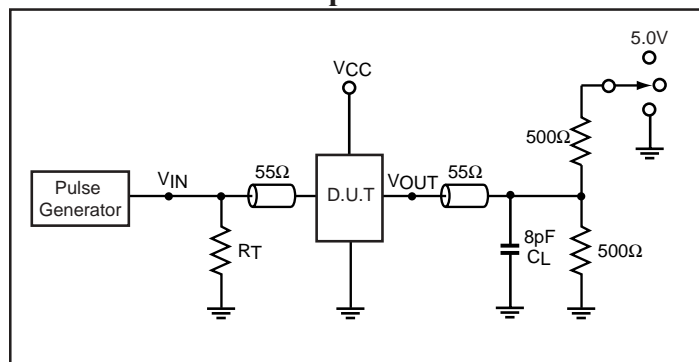
Switching Characteristics (over operating range over recommended operating free-air temperature range).

Parameter	Description	Conditions	Com			Units
			Min.	Typ	Max.	
t_{PY}	Propagation Delay ^(2,3) A_N to B_N w/ $Z_O = 50$ Ohms	–	–	0.3	–	ns
t_{SY}	Bus Select Time - \overline{SEL}_N to A_N, B_N	–	0.5	–	3.0	
t_{PZL}	Bus Enable Time - \overline{SEL}_N to A_N, B_N	–	0.5	–	3.0	
t_{PLZ}	Bus Disable Time - \overline{SEL}_N to A_N, B_N	–	0.5	–	3.0	
$t_{SK(o)}$	Output skew between center ports (A_4 & A_5) to any other port ⁽²⁾	–	–	0.1	0.2	
$t_{SK(p)}$	Skew between opposite transitions of the same output ($t_{pHL} - t_{pLH}$) ⁽²⁾	–	–	0.1	0.2	

Notes:

1. See test circuit and waveforms.
2. This parameter is guaranteed by design.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.75ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Test Circuits for All Outputs⁽¹⁾



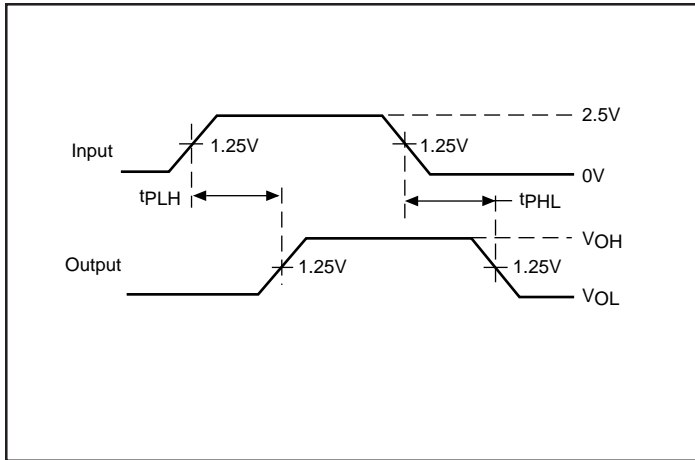
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: $PRR \leq$ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5ns$, $t_F \leq 2.5ns$.
5. The outputs are measured one at a time with one transition per measurement.

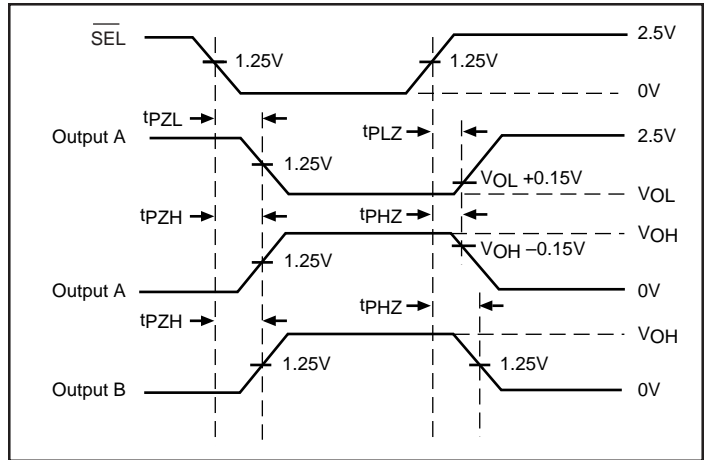
Switch Positions

Test	Switch
Disable LOW, Enable LOW (output on A side)	5.0V
Disable HIGH, Enable HIGH (output on A side)	GND
Disable/Enable High (output on B side) & Prop Delay	Open

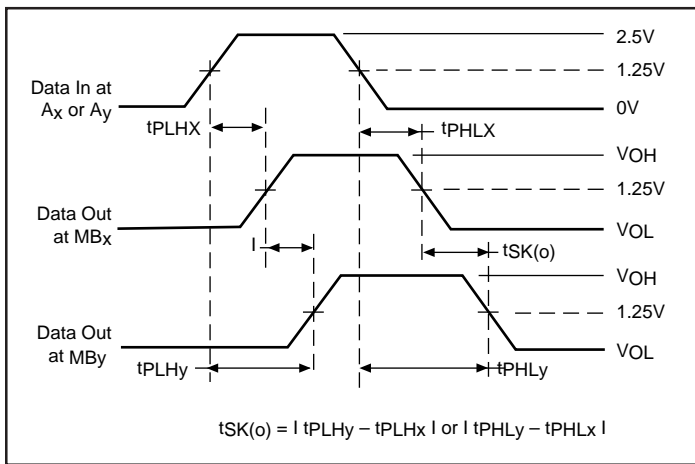
Switching Waveforms



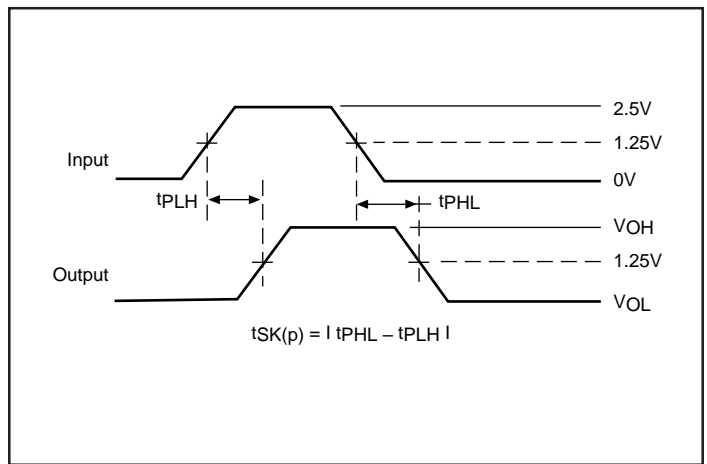
Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

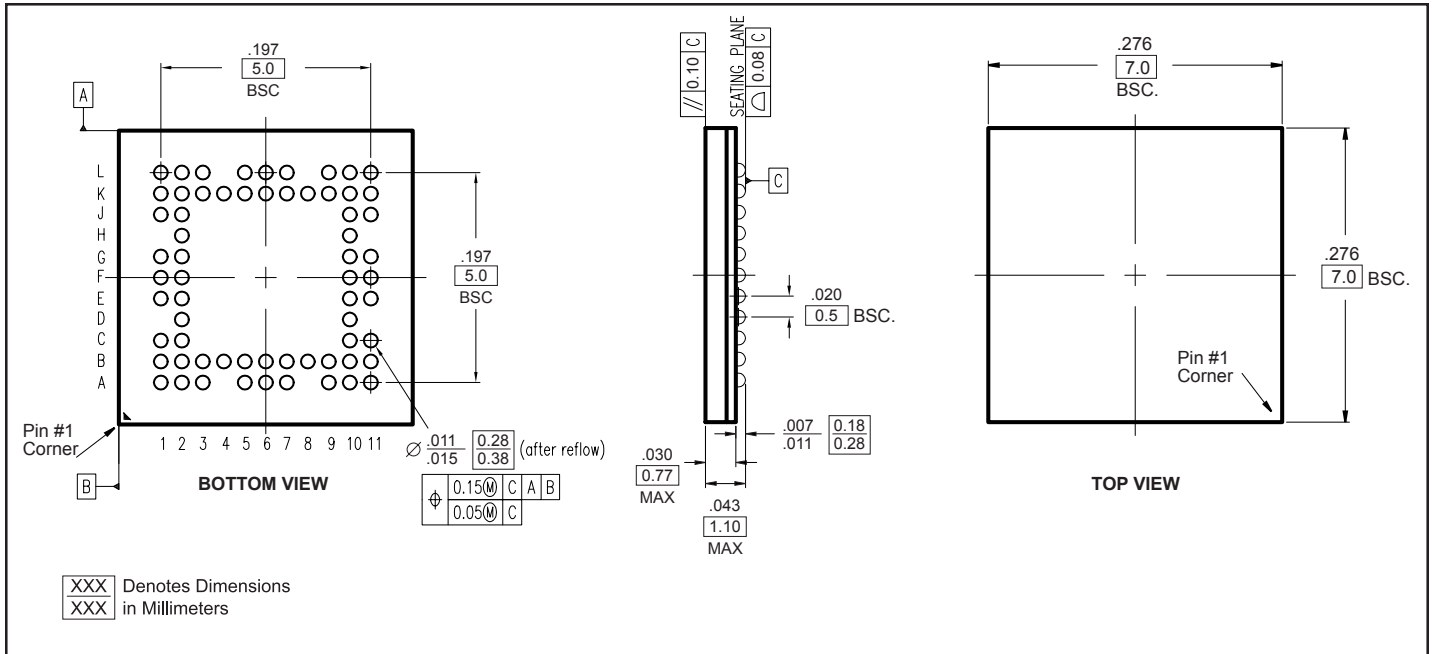


Output Skew - $t_{SK(o)}$



Pulse Skew - $t_{SK(p)}$

64-Pin TFBGA Package



Ordering Information

Part	Pin - Package
PI3B4010NC	64 - TFBGA

Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, IN may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing and Hot-Plug Information

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} and GND before applying signals to input/output or control pins.

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