

# MC12026A

## 1.1 GHz Dual Modulus Prescaler

### Description

The MC12026 is a high frequency, low voltage dual modulus prescaler used in phase-locked loop (PLL) applications.

The MC12026A can be used with CMOS synthesizers requiring positive edges to trigger internal counters in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of an 8/9 or 16/17 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

### Features

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of -40 to 85°C
- The MC12026 is Pin Compatible with the MC12022
- Short Setup Time ( $t_{set}$ ) 6.0 ns Typical @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Pb-Free Packages are Available

**Table 1. FUNCTIONAL TABLE**

SW	MC	Divide Ratio
H	H	8
H	L	9
L	H	16
L	L	17

1. SW: H =  $V_{CC}$ , L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V.

**Table 2. MAXIMUM RATINGS**

Characteristics	Symbol	Value	Unit
Power Supply Voltage, Pin 2	$V_{CC}$	-0.5 to 7.0	Vdc
Operating Temperature Range	$T_A$	-40 to 85	°C
Storage Temperature Range	$T_{stg}$	-65 to 150	°C
Modulus Control Input, Pin 6	MC	-0.5 to 6.5	Vdc
Maximum Output Current, Pin 4	$I_O$	10.0	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.



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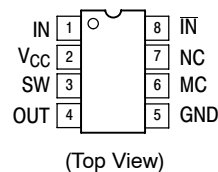
<http://onsemi.com>

### MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

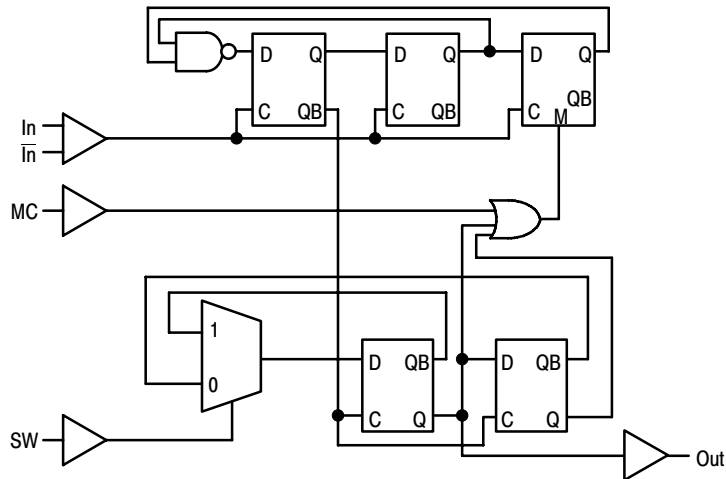
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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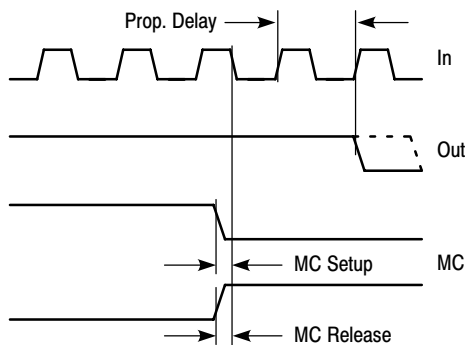
**Table 3. ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5$ ;  $T_A = -40$  to  $85^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sin Wave)	$f_t$	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	$I_{CC}$	-	4.0	5.3	mA
Modulus Control Input High (MC)	$V_{IH1}$	2.0	-	$V_{CC}$	V
Modulus Control Input Low (MC)	$V_{IL1}$	GND	-	0.8	V
Divide Ratio Control Input High (SW)	$V_{IH2}$	$V_{CC} - 0.5$ V	$V_{CC}$	$V_{CC} + 0.5$ V	V
Divide Ratio Control Input Low (SW)	$V_{IL2}$	OPEN	OPEN	OPEN	-
Output Voltage Swing ( $R_L = 560 \Omega$ ; $I_O = 5.5$ mA) (Note 3) ( $R_L = 1.1$ k $\Omega$ ; $I_O = 2.9$ mA) (Note 4)	$V_{out}$	1.0	1.6	-	$V_{pp}$
Modulus Setup Time MC to Out (Note 5)	$t_{SET}$	-	6.0	9.0	ns
Input Voltage Sensitivity 100–250 MHz 250–1100 MHz	$V_{in}$	400 100	- -	1000 1000	mVpp

3. Divide Ratio of  $\pm 8/9$  at 1.1 GHz,  $C_L = 8.0$  pF.
4. Divide Ratio of  $\pm 16/17$  at 1.1 GHz,  $C_L = 8.0$  pF.
5. Assuming  $R_L = 560 \Omega$  at 1.1 GHz.



**Figure 1. Logic Diagram (MC12026A)**



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

**Figure 2. Modulus Setup Time**

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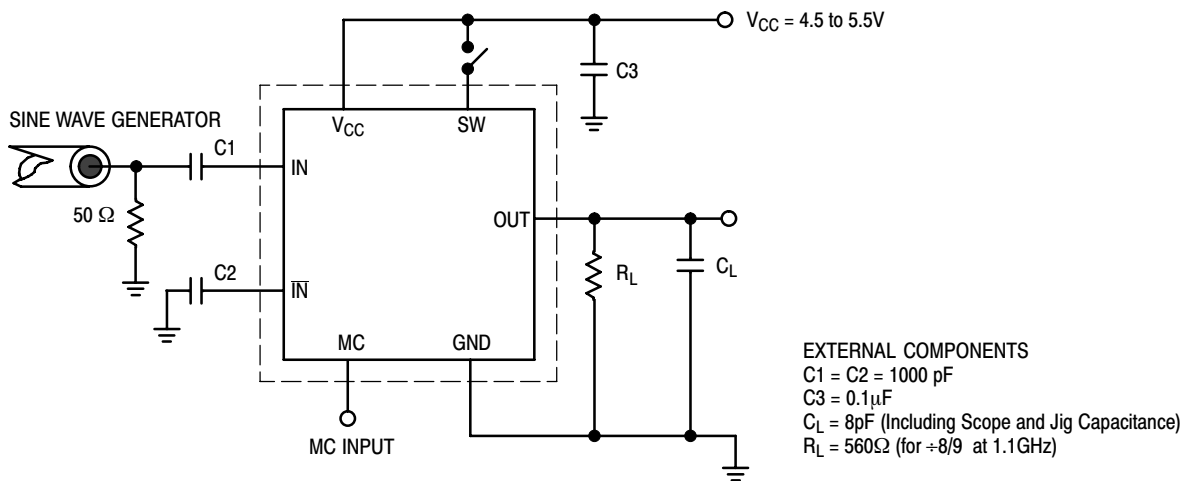


Figure 3. AC Test Circuit

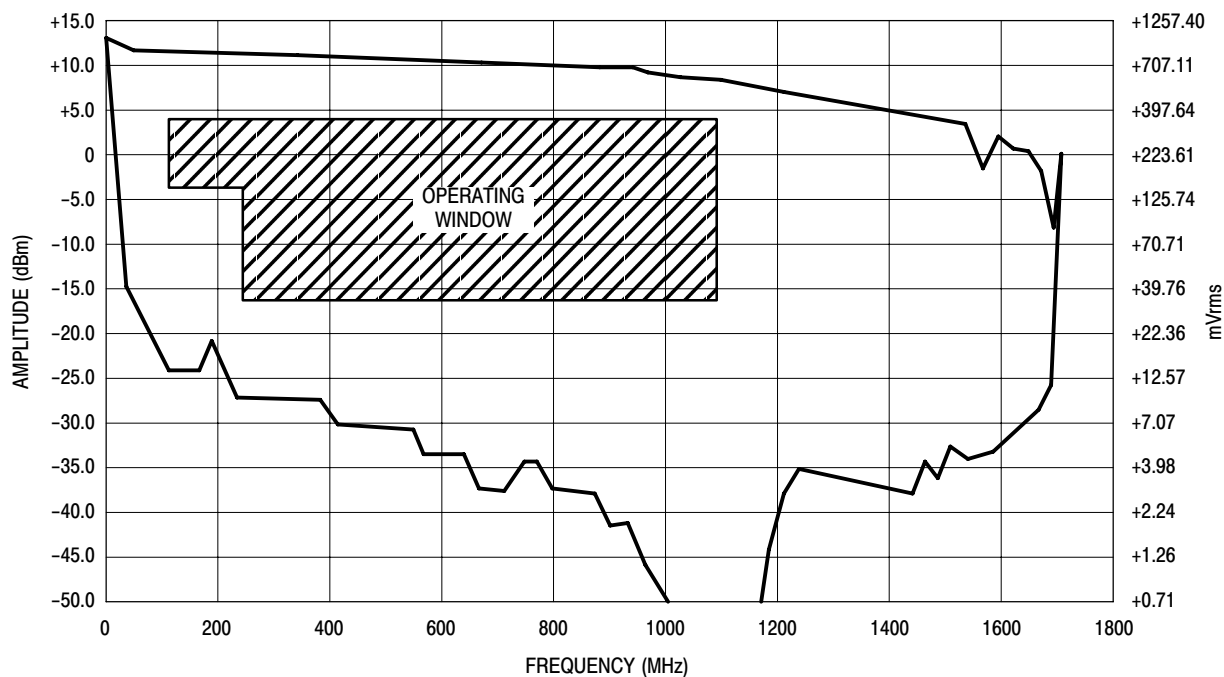


Figure 4. Input Signal Amplitude versus Input Frequency

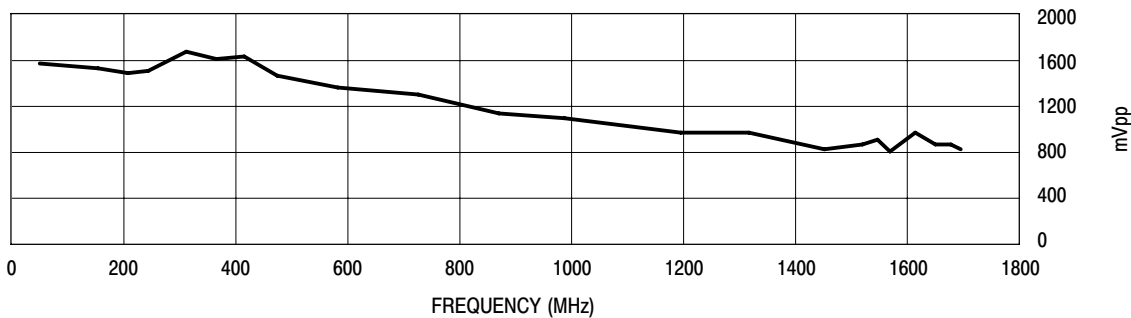
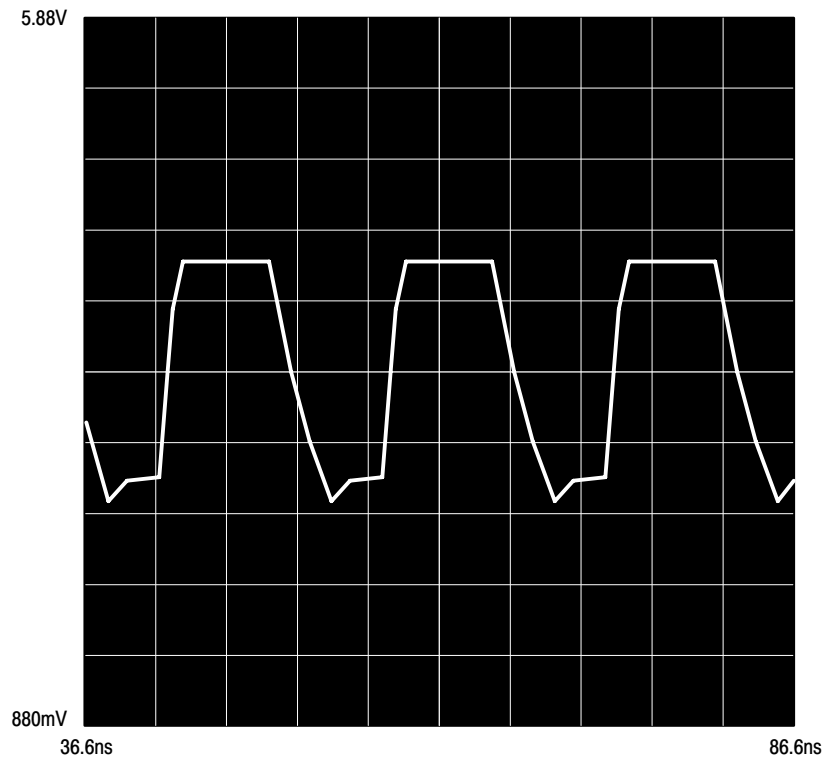


Figure 5. Output Amplitude versus Input Frequency

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(±8, 1.1 GHz Input Frequency,  $V_{CC} = 5.0$ ,  $T_A = 25^\circ\text{C}$ , Output Loaded With 8.0pF)

**Figure 6. Typical Output Waveform**

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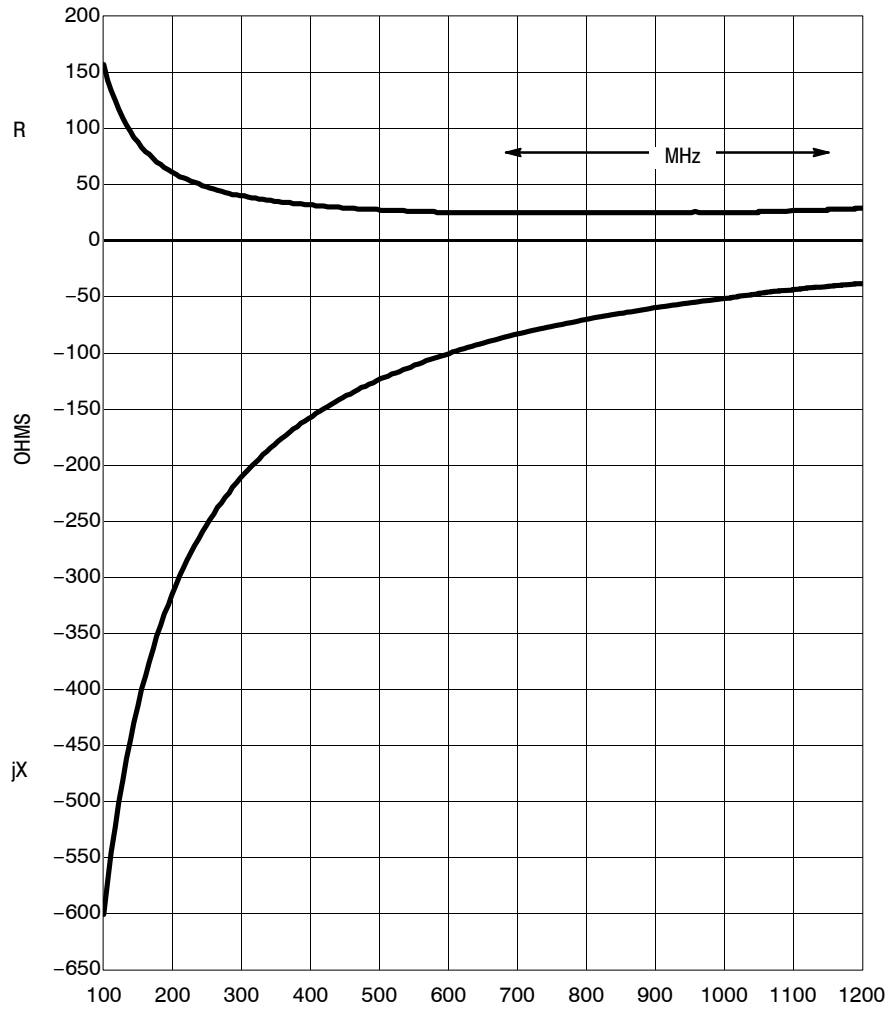


Figure 7. Typical Input Impedance versus Input Frequency

## ORDERING INFORMATION

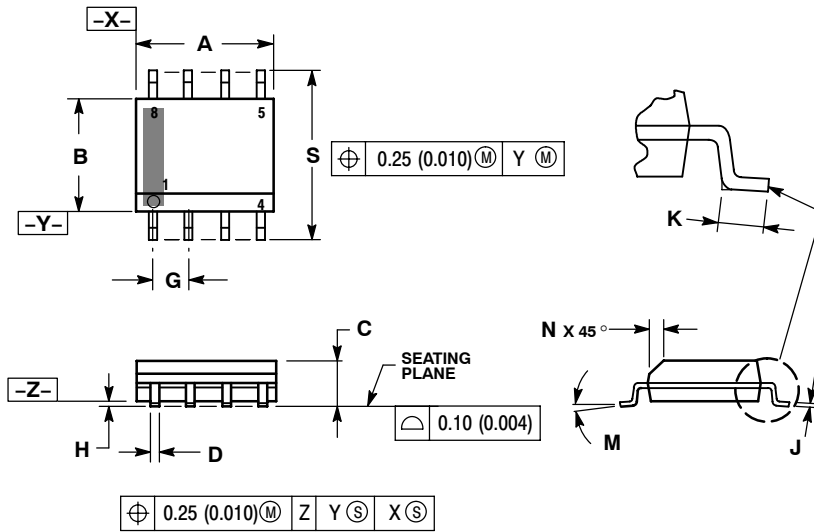
Device	Package	Shipping <sup>†</sup>
MC12026AD	SOIC-8	98 Units / Rail
MC12026ADG	SOIC-8 (Pb-Free)	98 Units / Rail
MC12026ADR2	SOIC-8	2500 / Tape & Reel
MC12026ADR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

### SOIC-8 NB CASE 751-07 ISSUE AG

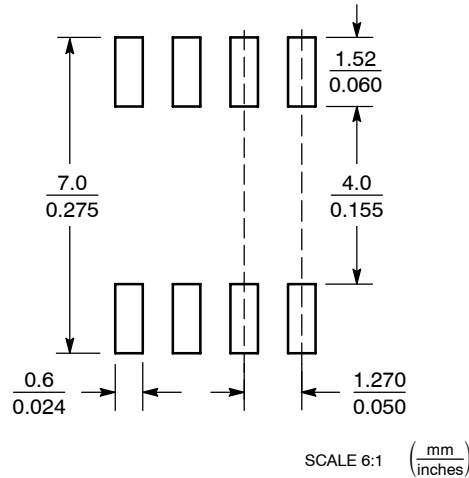


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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