MHS

data sheet

T-46-23-12

# HM 65764

## 8K x 8
## HIGH SPEED CMOS SRAM

OCTOBER 1987

### Features

- **FAST ACCESS TIME : 35/45/55 ns max**
- **STANDBY CURRENT : 20 mA**
- **OPERATING CURRENT : 150 mA**
- **ASYNCHRONOUS INPUTS**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SINGLE 5 VOLT SUPPLY**
- **300 MILS WIDTH PACKAGE**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE**
- **WIDE TEMPERATURE RANGE : – 55°C TO + 125°C**

### Description

The HM 65764 is a high speed CMOS static RAM organised as 8192 x 8 bits. It is manufactured using MHS's high performance, CMOS technology.

Access times as fast as 35 ns are available with maximum power consumption of only 825 mW.

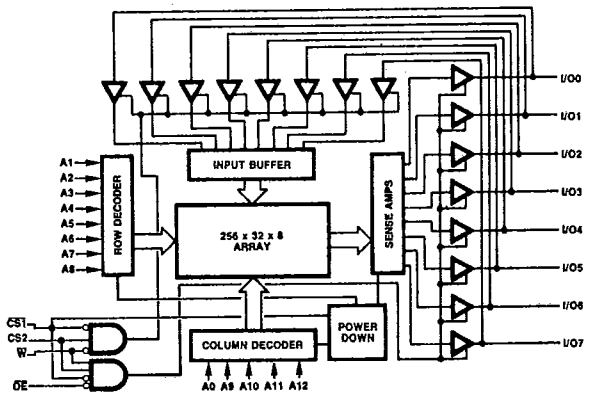
The HM 65764 features fully static operation requiring no external clocks or timing strobes, additionally the automatic power-down feature reduces the power consumption by 73 % when deselected. Easy memory expansion is provided by an active low chip select ($\overline{CS1}$) and three state drivers, an active high chip select (CS2), an active low output enable.

All inputs and outputs of the HM 65764 are TTL compatible and operate from a single 5V supply thus simplifying system design.

The HM 65764 is packaged in a plastic/ceramic 300 mils 28 pins DIL, SO 28 pins DIL, or a 32 pins Leadless Chip Carrier allowing high board-level packing densities.

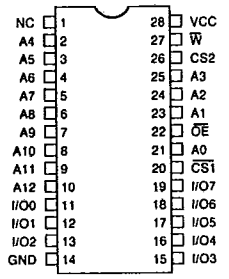
The HM 65764 is 100 % processed following the test methods of MIL STD 883C.

### Block Diagram

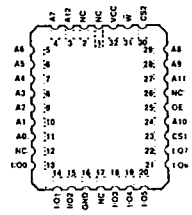



### Pinouts (TOP VIEW)

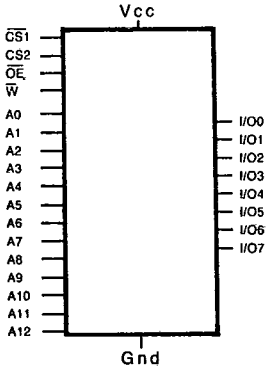
DIL (28 PINS)




LCC (32 PINS)



### Logic Symbol




### PIN NAMES

| | | | |
|---|---|---|---|
| A0-A12 | : Address inputs | OE | : Output enable |
| I/O | : Input/Output | Gnd | : Ground |
| CS1-CS2 | : Chip select | W | : Write enable |
| Vcc | : Power | | |

### TRUTH TABLE

| CS1 | CS2 | OE | W | Din | Dout | MODE |
|---|---|---|---|---|---|---|
| H | X | X | X | Z | Z | Deselect (power down) |
| L | H | L | H | Z | Valid | Read |
| L | H | X | L | Valid | Z | Write |
| L | H | H | H | Z | Z | Deselect |
| X | L | X | X | Z | Z | Deselect |

L = Low, H = High, X = H or L

| • ABSOLUTE MAXIMUM RATINGS | • OPERATING RANGE | | |
|---|---|---|---|
| | | Operating Voltage | Operating Temperature |
| Supply voltage to GND potential — 0.5 V* to + 7.0V<br>DC input or output voltage : – 3.0V to 7.0V<br>DC output voltage in high Z state : – 0.5V to 7.0V<br>Storage temperature : – 65° C to + 150° C<br>Output current into outputs (low) : 20 mA | Military (– 2) | VCC ± 10 % | – 55° C to + 125° C |
| | Commercial (– 5) | VCC ± 10 % | 0°C to + 70°C |

Electro Static Discharge Voltage ≅ 2000V
(per MIL STD 883, Method 3015.2)

## ELECTRICAL CHARACTERISTICS

### DC PARAMETERS

| Symbol | Parameter | 65764K-5<br>65764M-5 | 65764M-2 | 65764N-5 | 65764N-2 | Unit | Value |
|---|---|---|---|---|---|---|---|
| ICCSB1 (1) | Stand by supply current | 40 | 40 | 40 | 40 | mA | max |
| ICCSB2 (2) | Stand by supply current | 20 | 20 | 20 | 20 | mA | max |
| ICCOP (3) | Average operating supply current | 150 | 150 | 150 | 150 | mA | max |
| IIX (4) | Input leakage current | ± 10 | ± 10 | ± 10 | ± 10 | µA | max |
| IOZ (4 ) | Output leakage current | ± 10 | ± 10 | ± 10 | ± 10 | µA | max |
| VIL (5) | Input low voltage | 0.8 | 0.8 | 0.8 | 0.8 | V | max |
| VIH (5) | Input high voltage | 2.2 | 2.2 | 2.2 | 2.2 | V | min |
| VOL (6) | Output low voltage | 0.4 | 0.4 | 0.4 | 0.4 | V | max |
| VOH (6) | Output high voltage | 2.4 | 2.4 | 2.4 | 2.4 | V | min |
| I OS (7) | Output short circuit current | – 350 | – 350 | – 350 | – 3 | mA | max |
| C IN (8) | Input capacitance | 5 | 5 | 5 | 5 | pF | max |
| C OUT (8) | Output capacitance | 7 | 7 | 7 | 7 | pF | max |

**Note 1 :** $\overline{CS} \geqslant$ VIH
**Note 2 :** $\overline{CS} \geqslant$ VCC – 0.3V, VIN $\geqslant$ VCC – 0.3V or VIN $\leqslant$ 0.3V
**Note 3 :** VCC max, Iout = 0 mA
**Note 4 :** GND $\leqslant$ VI $\leqslant$ VCC, GND $\leqslant$ VO $\leqslant$ VCC Output disabled
**Note 5 :** VIL min = – 3.0V, VIH max = VCC
**Note 6 :** VCC = min, IOH = – 4 mA, IOL = 8.0 mA
**Note 7 :** VCC = max, Vout = GND, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time
**Note 8 :** This parameter is sampled and not 100 % tested. TA = 25°C, F = 1 MHz, VCC = 5.0V

**AC PARAMETERS :**

Conditions : Input pulse levels GND to 3.0V
Input rise 5 ns
Input timing reference levels 1.5V
Output loading IOL/IOH (see fig. 1a and 1b) + 30 pF

**Read cycle**

| Parameter | Description | 65764-K5 | 65764M-5 | 65764M-2 | 65764N-5 | 65764N-2 | Unit | Value |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 35 | 45 | 45 | 55 | 55 | ns | min |
| TAVQV | Address to data valid | 35 | 45 | 45 | 55 | 55 | ns | max |
| TAVQX | Data hold from address change | 3 | 5 | 5 | 5 | 5 | ns | min |
| TEL1QV | $\overline{CS1}$ low to data valid | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL2QV | CS2 high to data valid | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL1QX | $\overline{CS1}$ low to low Z (9) | 5 | 10 | 10 | 10 | 10 | ns | min |
| TEH2QX | CS2 low to low Z | 5 | 10 | 10 | 10 | 10 | ns | max |
| TEH1QZ | $\overline{CS1}$ high to high Z (8, 9) | 15 | 20 | 20 | 20 | 20 | ns | max |
| TEL2QZ | CS2 low to high Z | 15 | 20 | 20 | 20 | 20 | ns | max |
| TELIC | $\overline{CS1}$ low to power up | 0 | 0 | 0 | 0 | 0 | ns | min |
| TEHICCL | $\overline{CS1}$ high to power down | 20 | 25 | 25 | 25 | 25 | ns | max |
| TGLQV | $\overline{OE}$ low to data valid | 15 | 20 | 20 | 25 | 25 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 0 | 0 | 0 | 0 | 0 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 20 | 25 | 25 | 30 | 30 | ns | max |

**Write cycle (10)**

| Parameter | Description | 65764K-5 | 65764M-5 | 65764M-2 | 65764N-5 | 65764N-2 | Unit | Value |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 30 | 40 | 40 | 50 | 50 | ns | min |
| TEL1WH | $\overline{CS1}$ low to write end | 30 | 40 | 40 | 45 | 45 | ns | min |
| TEH2WH | CS2 high to write end | 30 | 40 | 40 | 45 | 45 | ns | min |
| TAVWH | Address set up to write end | 30 | 40 | 40 | 45 | 45 | ns | min |
| TWHAX | Address hold from write end | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWL | Address set up to write start | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWLWH | $\overline{W}$ pulse width | 20 | 25 | 25 | 30 | 30 | ns | min |
| TDVWH | Data set up to write end | 15 | 20 | 20 | 25 | 25 | ns | min |
| TWHDX | Data hold from write end | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWLQZ | $\overline{W}$ high to low Z (10) | 15 | 20 | 20 | 20 | 20 | ns | max |
| TWHQX | $\overline{W}$ low to high Z (9, 10) | 0 | 0 | 0 | 0 | 0 | ns | min |

**Note 9 :** TEHQZ, TWLQZ are tested with C1 = 5 pF as in figure 1b. Transition is measured ± 500 mV from steady state voltage.
**Note 10 :** At any given temperature and voltage condition, TEHQZ is less than TELQX for all devices. These parameters are sampled and not 100 % sampled.
**Note 11 :** The data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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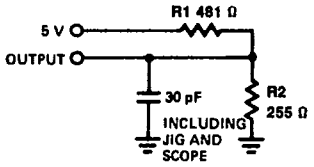



Figure 1a

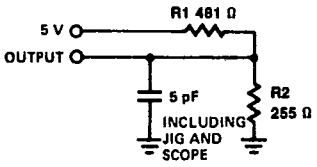



Figure 1b

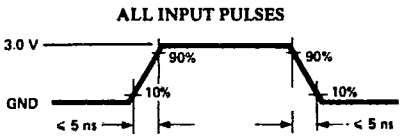
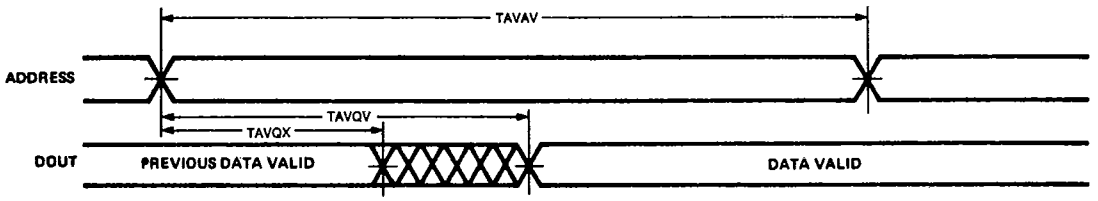


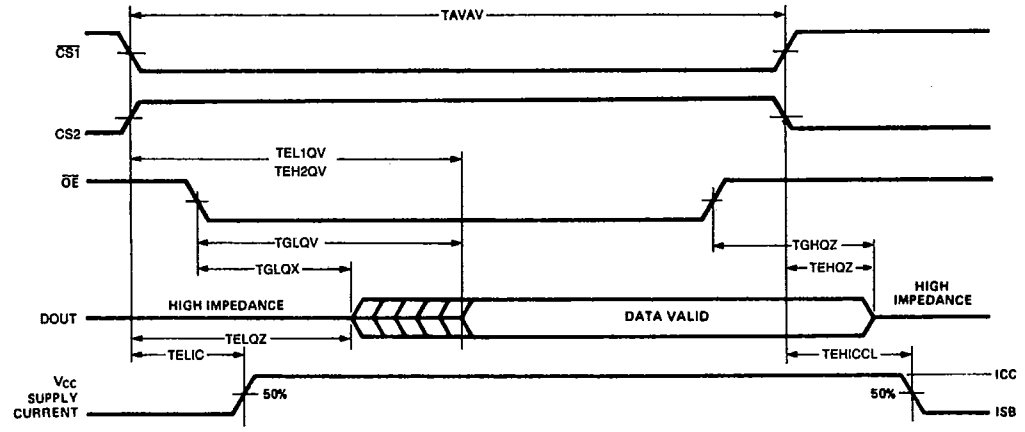

Figure 2

## Switching Waveforms

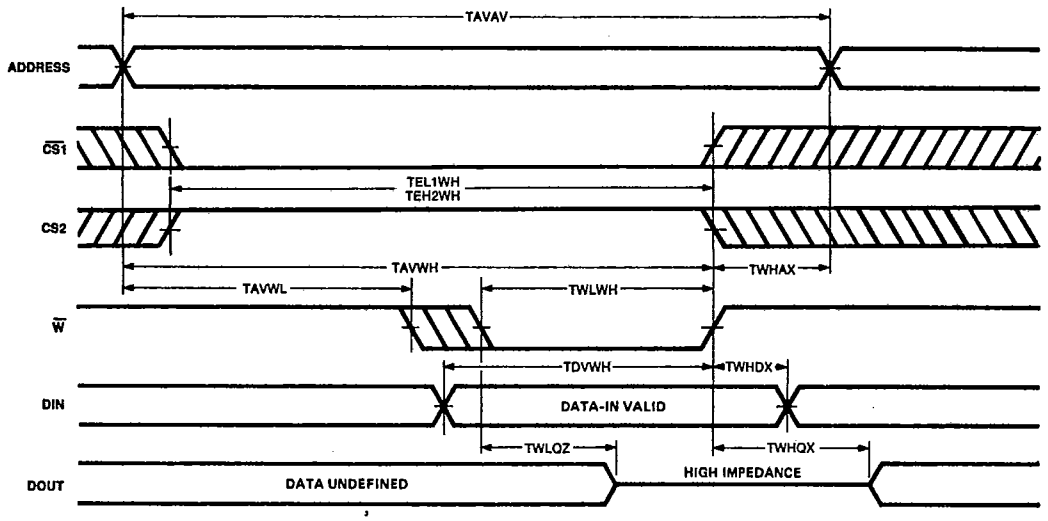
**READ CYCLE No. 1** (Notes 11, 12)



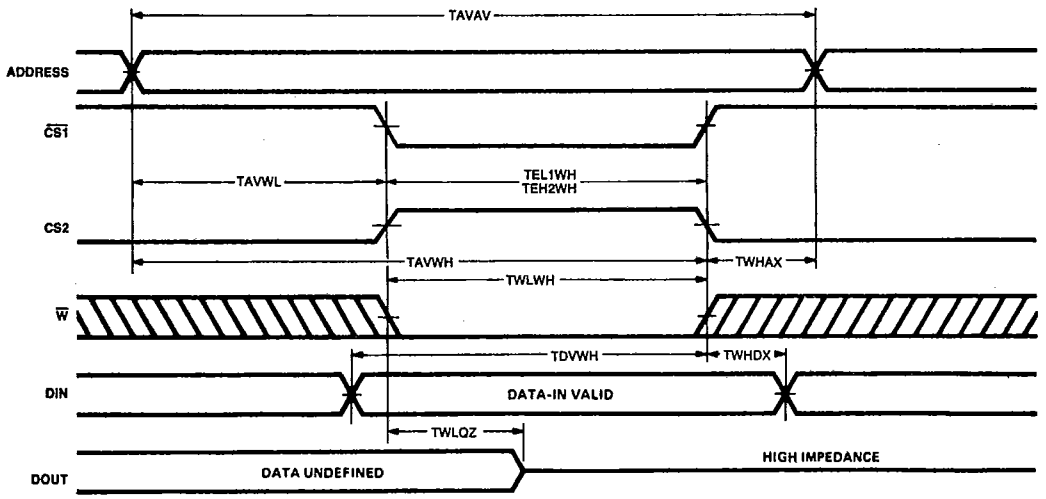

**READ CYCLE No. 2** (Notes 11, 13)



**Write Cycle No. 1 ($\overline{W}$ Controlled)** (Note 7)




**Write Cycle No. 2 ($\overline{CS}$ Controlled)** (Note 7)




**Note :** If $\overline{CS}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.

**Note 12 :** $\overline{W}$ is high for read cycle.
**Note 13 :** Device is continuously selected, $\overline{CS}$ = VIL.
**Note 14 :** Address valid prior to or coincident with $\overline{CS}$ transition low.

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## *Ordering information*

| DEVICE TYPE | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| HM1-65764 ( ) -5 | CERAMIC DIL | 0°C to + 70°C |
| HM1-65764 ( ) -2 | CERAMIC DIL | – 55°C to + 125°C |
| HM1-65764 ( ) -8 | CERAMIC DIL | – 55°C to + 125°C |
| HM3-65764 ( ) -5 | PLASTIC DIL | 0°C to + 70°C |
| HMT-65764 ( ) -5 | SO PLASTIC DIL | 0°C to + 70°C |
| HM4-65764 ( ) -5 | LCC 28 pin | 0°C to + 70°C |
| HM4-65764 ( ) -2 | LCC 28 pin | – 55°C to + 125°C |
| HM4-65764 ( ) -8 | LCC 28 pin | – 55°C to + 125°C |

TEMPERATURE RANGE (– 2, – 5, – 8)

PERFORMANCE :
K : 35 ns (commercial only)
M : 45 ns
N : 55 ns

DEVICE TITLE

PACKAGE (1, 3, 4, T)
1 : CERAMIC
3 : PLASTIC
4 : LCC
T : SO