ICS331
QTClock™ Single Output Clock

Description

The ICS331 is a low cost frequency generator that is factory programmable. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal or clock input to produce a spread or non-spread output clock.

The chip has two select inputs that allow the selection of up to four different frequencies stored in memory. If multiple output selections and spread spectrum are not required, refer to the ICS300 and ICS301 for lower cost solutions.

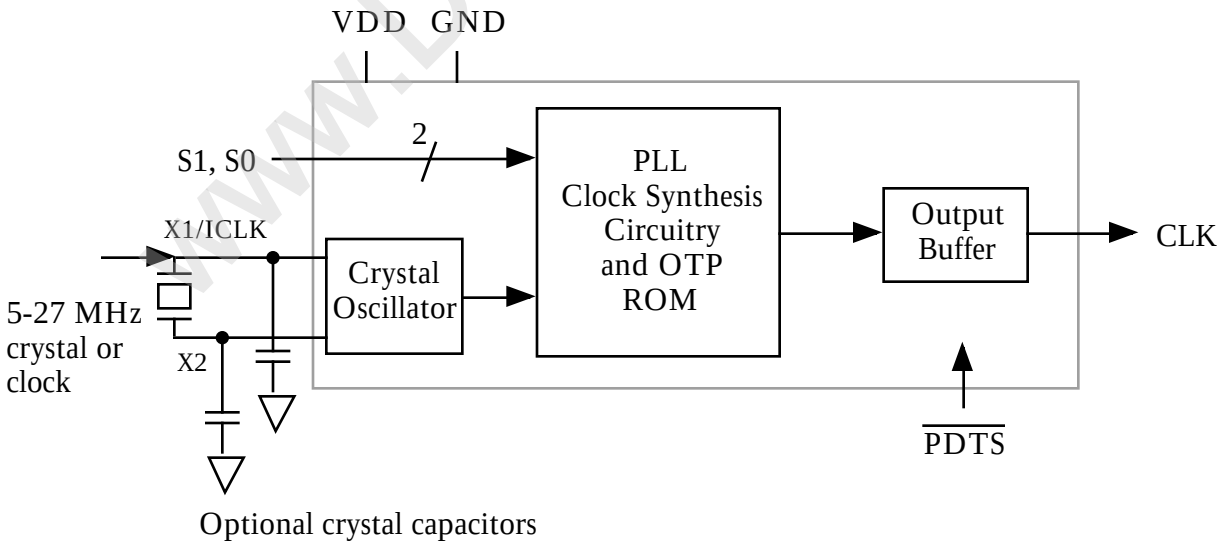
The device also has an power down feature that tri states the clock outputs and turns off the PLL when the $\overline{\text{PDTS}}$ pin is taken low.

This data sheet is to be used with the one-page programming information for the complete specification on the device.

Features

- Packaged as 8 pin SOIC
- Zero ppm synthesis error in most applications
- Input crystal frequency from 5 to 27 MHz
- Input clock frequency from 3 to 50 MHz
- Output clock frequencies up to 200 MHz
- Four ROM locations for frequency and spread selection
- Spread spectrum capability for low EMI
- Duty cycle of 45/55
- 3.3 V operating voltage (consult ICS for 5V)
- Advanced, low power CMOS pr

Block Diagram



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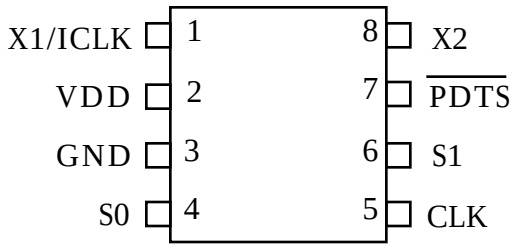
Pin Assignment



Output Select Table

S1	S0	CLK (MHz)	Spread Amount
0	0	TBD	TBD
0	1	TBD	TBD
1	0	TBD	TBD
1	1	TBD	TBD

The select pins can also be defined as power down or tri state pins.

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	XI	Crystal connection. Connect to an 5 to 27 MHz fundamental crystal or clock input.
2	VDD	P	Connect to +3.3 V.
3	GND	P	Connect to ground.
4	S0	I	Select pin S0 for frequency selections on CLK. Internal pull-up.
5	CLK	O	CMOS level clock output. Weak internal pull-down when tri state.
6	S1	I	Select pin S1 for frequency selections on CLK. Internal pull-up.
7	$\overline{\text{PDTS}}$	I	Powers down entire chip, tri states CLK output, when low. Internal pull-up.
8	X2	XO	Crystal connection. Connect to an 5 to 27 MHz fundamental crystal. Float for clock.

Key: XI/XO = Crystal Connections, I = Input, O = output, P = power supply connection

External Components / Crystal Selection

The ICS331 requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS331 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω terminating resistor can be used next to each output pin. A parallel resonant, fundamental mode crystal should be used. Crystal capacitors should be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L-6)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are required for all applications.

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Operating Voltage, VDD		3.13		3.47	V
Input High Voltage, VIH	$\overline{\text{PDTS}}$, S1, S0	2			V
Input Low Voltage, VIL	$\overline{\text{PDTS}}$, S1, S0			0.4	V
Input High Voltage, VIH	ICLK	(VDD/2)+1			V
Input Low Voltage, VIL	ICLK			(VDD/2)-1	V
Output High Voltage, VOH, CMOS high	IOH=-8mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
IDD Operating Supply Current	No Load		TBD		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor	Input pins		270		kΩ
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		3		50	MHz
Output Frequency		TBD		200	MHz
Output Frequency Synthesis Error				0	ppm
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%
Output Enable Time, $\overline{\text{PDTS}}$ high to output on				TBD	µs
Output Disable Time, $\overline{\text{PDTS}}$ low to tri state				TBD	µs
Absolute Clock Period Jitter	Deviation from mean		TBD		ps
One Sigma Clock Period Jitter			TBD		ps

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Typical values are at 25°C.

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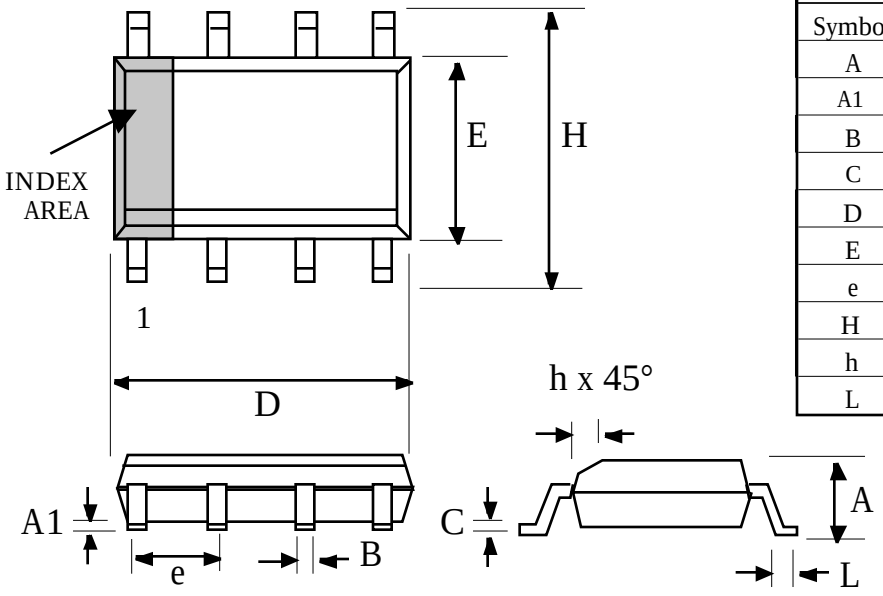
Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS331M-xx	ICS331M	8 pin SOIC	0 to 70 °C
ICS331M-xxT	ICS331M	8 pin SOIC on tape and reel	0 to 70 °C

The -xx indicates a two-character programming code, which must be specified when ordering parts.