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Application Note

LAYOUT AND DESIGN RULES FOR DATA CONVERTERS AND OTHER MIXED SIGNAL DEVICES

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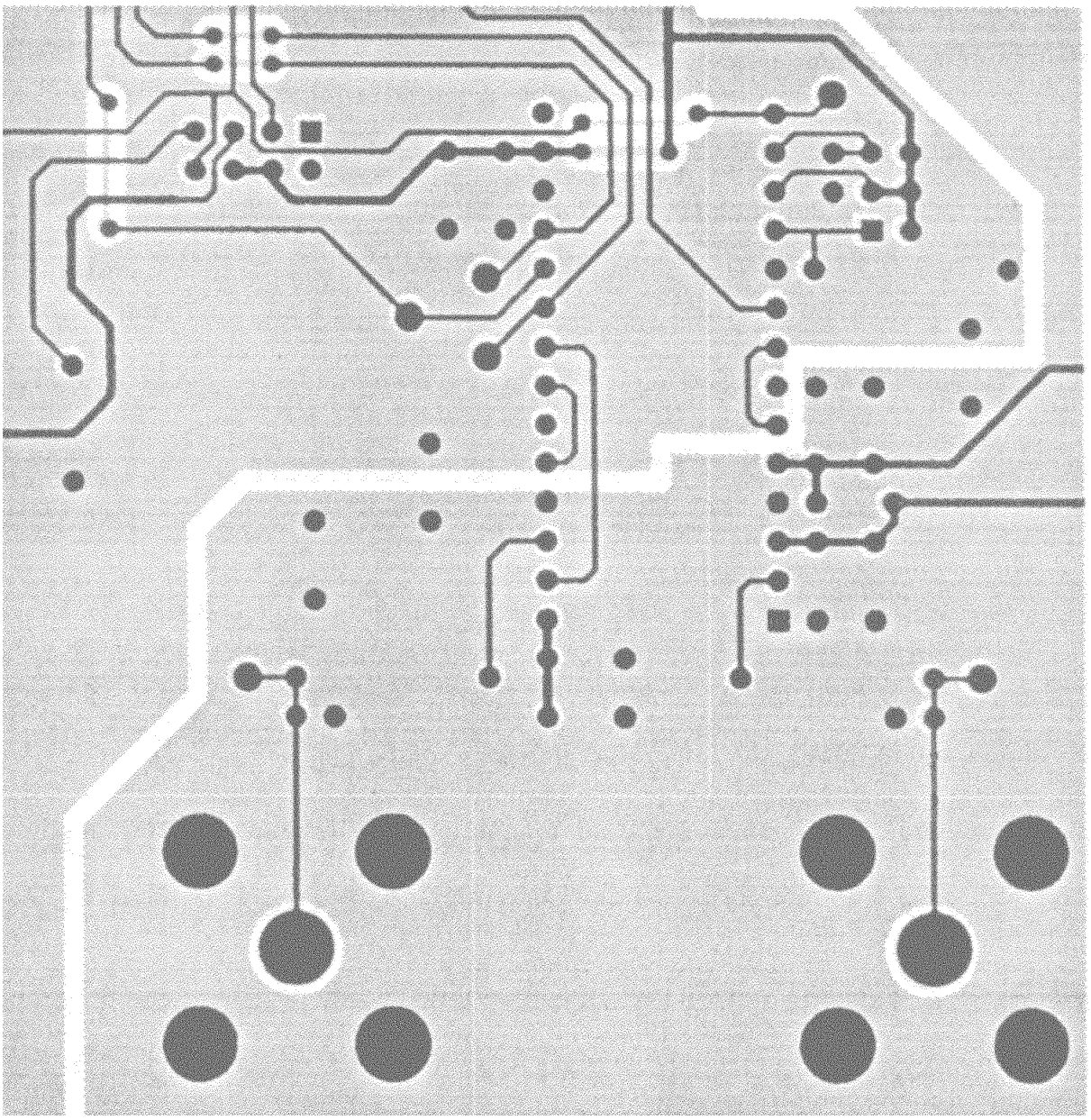

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Here is a list of guidelines for optimum printed circuit board layout for Crystal ADCs, DAC's, and codecs. Use these pages as a checklist during and after layout by checking the boxes when each line item is OK. Many Crystal products have specific individual requirements. Check in the device and evaluation board/reference design data sheets for specific layout recomendations. Specific device requirements take precedence over the general guidelines given here. Remember, Crystal offers a free schematic and layout review service. Try hard to use this service before building your first prototype board. Comments or additional items are very welcome.

❑ 1) Partition the board with all analog components grouped together in one area and all digital components in the other. Common power supply related components should be centrally located.

❑ 2) Have separate analog and digital ground planes on the same layer, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes should be >1/8".

❑ 3) Mixed signal components, including the data converters, should bridge the partition in the ground plane with only analog pins in the analog area, and only digital pins in the digital area. Rotating the data converter can often make this task easier. Look at the evaluation board data sheet to see where the split should be located.

For our serial codecs, and most single die converters, the device should be placed over the analog ground plane, positioned next to the ground plane split. The digital pins should be next to the split, with the digital traces crossing directly over into the digital region of the board. The analog ground pins and digital ground pins should be connected with zero impedance (same ground plane). See the CS4215 and CS4216, CDB4215 and CDB4216 data sheets for examples.

❑ 4) Analog and digital ground planes should only be connected at one point (in most cases). Have vias available in the board to allow alternative connection points.

❑ 5) Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane. These regions should not be left floating, which only make the interference worse. Using ground plane fill has been shown to reduce digital to analog coupling by up to 30 dB.

❑ 6) The analog to digital ground plane connection should be near to the power supply, or near to the power supply connections to the board, or near to the data converter. In the case of multiple converters, leave jumper options at each converter.

❑ 7) Analog power and analog signal traces should be over the analog ground plane.

❑ 8) Digital power and digital signal traces should be over the digital ground plane.

❑ 9) Keep digital signal traces, especially the clock, as far away from analog input and voltage reference pins as possible.

❑ 10) Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connection to pins with wide traces to reduce impedance.

- ❑ 11) If both large electrolytic and small ceramic capacitors are recommended, make the small ceramic capacitor closest to the IC pins. For multi-layer pc boards, make the connections to the converter and to the capacitors on the same layer (this avoids the additional impedance of vias).
- ❑ 12) All filtering capacitors in the signal path should be NPO/COG dielectric. BX/X7R dielectric is OK for DC voltages where voltage coefficient is not a factor.
- ❑ 13) All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors are OK for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor. Avoid wire wound resistors and potentiometers.
- ❑ 14) Avoid multiple crystal oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D or D/A sampling clock.
- ❑ 15) When using converters with DSP IC's, operate everything from one crystal using dividers if necessary.
- ❑ 16) In systems requiring multiple crystals for selectable sampling frequencies, enable only one at a time. Shut off all other oscillators by removing power. Make sure other oscillators are off either with an active crowbar on Vcc or very high impedance switch. Often the leakage from a transistor or FET which is not completely off is sufficient for the oscillator to produce a low level output frequency.
- ❑ 17) When using DC-DC switching regulators, synchronize the switching frequency to the A/D if possible. This applies to CMOS chopper amplifiers as well.
- ❑ 18) Avoid connecting the clock source oscillator to the converter sampling clock input through analog multiplexers, PAL's, gate arrays, opto-couplers or circuits which can cause jitter.
- ❑ 19) Locate the crystal or oscillator close to the converter. Avoid overshoot and undershoot on the master clock for the converter.
- ❑ 20) Use buffers for digital signals directly to or from the converter to connectors which go off the board.
- ❑ 21) In the case of piggy-back boards, or boards which plug into a slot adjacent to other boards, consider the circuits which will be above or below the converter as sources of interference. A mu-metal screen may be required.
- ❑ 22) For delta sigma converters, make sure that potential interfering clocks are not in sensitive frequency regions. Sensitive regions are defined as ± passband either side of multiples of the input sample rate. Two examples are: a) for a CS5336 operating at 48 kHz word rate, the frequencies to avoid are (N X 3.072 MHz) ±24 kHz. b) for a CS5501 with a 4 MHz crystal, the frequencies to avoid are (N X 16 kHz) ±10 Hz. Frequencies which are synchronous to the input sample rate will not cause problems, since they will be converted to dc, and calibrated out.
- ❑ 23) For boards with more than 2 layers, do not overlap analog related and digital related planes. Do not have a plane which crosses the split between the analog ground plane region and the digital ground plane region.

- ❑ 24) For boards with both A/D converters and D/A converters, provide a means for testing each function separately. Possible methods include providing a header to allow access to the digital data paths, and allowing for easy attachment of a CS8402 and CS8412 AES/EBU transmitter and receiver parts.
- ❑ 25) Terminate unused op-amps in dual and quad packs by grounding the + input and connecting the - input to the output.
- ❑ 26) Digital control lines which must cross into the analog region should be as short as possible and should be mostly static. For example, digital gain and analog mux control lines.
- ❑ 27) The pins of DIP or SOIC packages should not have ground plane in between adjacent pins.
- ❑ 28) In systems using a delta-sigma converter, then avoid the use of clocks (particularly the serial bit clock) at half the frequency of the input sample rate. If this frequency interferes with the voltage reference, then tones can occur.
- ❑ 29) Do not surround the analog region with digital components. Do not surround the digital region with the analog region.

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