M52755SP

WIDE BAND ANALOG SWITCH

DESCRIPTION

The M52755SP is a semiconductor integrated circuit for the RGBHV interface. The device features switching signals input from two types of image sources and outputting the signals to the CRT display, etc. Synchronous signals, meeting a frequency band of 10kHz to 200kHz, are output at TTL. The frequency band of video signals is 250MHz, acquiring high-resolution images, and are optimum as an interface IC with high-resolution CRT display and various new media.

FEATURES

- Frequency band: RGB.....250MHz
  HV.....10Hz to 200kHz
  Input level: RGB.....0.7V_{P-P} (typ.)
  HV TTL input.....3.5V_{O-P} (both channel)
- Only the G channel is provided with sync-on video output.
- The TTL format is adopted for HV output.

APPLICATION

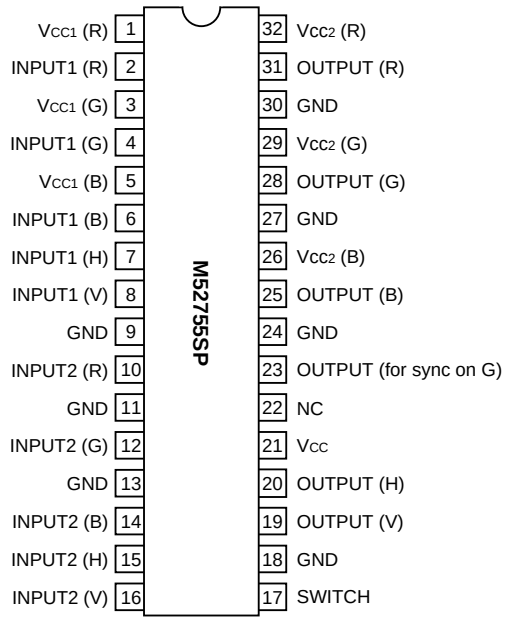
Display monitor

RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.5 to 5.5V

Rated supply voltage.....5.0V

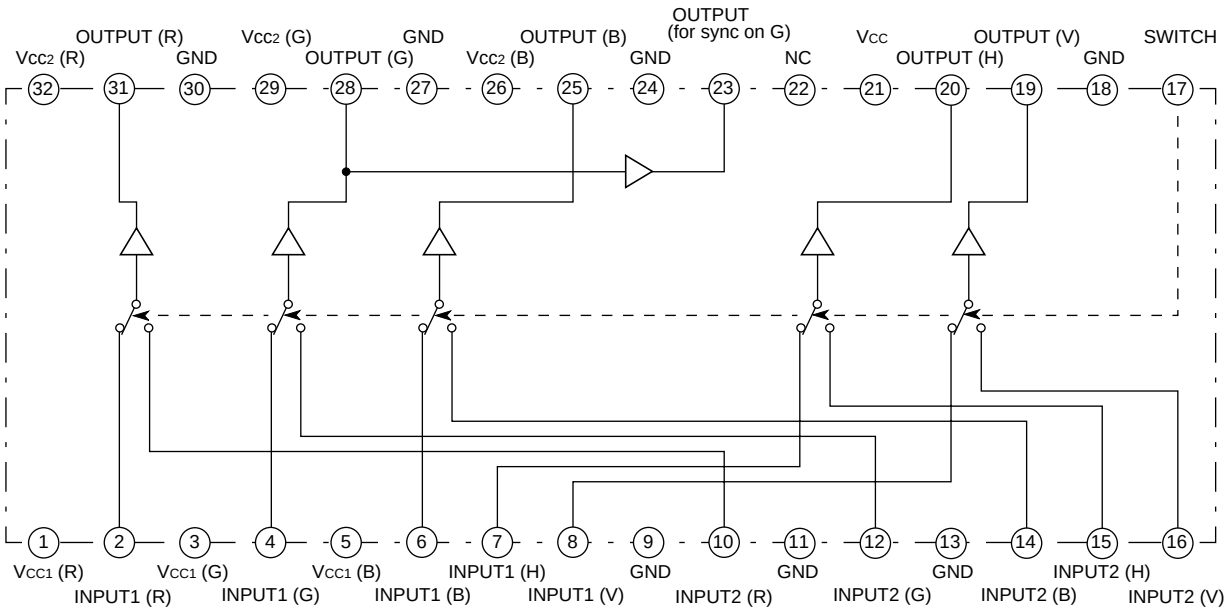
PIN CONFIGURATION (TOP VIEW)



Outline 32P4B

NC : NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	7.0	V
P_d	Power dissipation	1603	mW
T_{opr}	Ambient temperature	-20 to +85	°C
T_{stg}	Storage temperature	-40 to +150	°C
V_{opr}	Recommended supply voltage	5.0	V
$V_{opr'}$	Recommended supply voltage range	4.5 to 5.5	V
Surge	Electrostatic discharge	±200	V

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions													Limits			Unit
		Test point (s)	V_{CC} (V)	Input										SW				
			V_{CC}	SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW17 Switch	Min.	Typ.	Max.	
I_{CC1}	Circuit current1 (no signal)	A	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b GND	46	66	86	mA
I_{CC2}	Circuit current2 (no signal)	A	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a OPEN	46	66	86	mA
(RGB SW)																		
V_{DC1}	Output DC voltage1	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b GND	1.85	2.05	2.25	V
V_{DC2}	Output DC voltage2	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a OPEN	1.85	2.05	2.25	V
V_{DC3}	Output DC voltage3	T.P.23	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b GND	0.75	1.15	1.55	V
V_{DC4}	Output DC voltage4	T.P.23	5	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a OPEN	0.75	1.15	1.55	V
V_{imax1}	Maximum allowable input1	T.P.2 T.P.4 T.P.6	5	abb SG1	bab SG1	bba SG1	b –	b –	b –	b –	b –	b –	b –	b GND	2.0	2.4	–	V_{P-P}
V_{imax2}	Maximum allowable input2	T.P.10 T.P.12 T.P.14	5	b –	b –	b –	b –	b –	abb SG1	bab SG1	bba SG1	b –	b –	a OPEN	2.0	2.4	–	V_{P-P}
G_{V1}	Voltage gain1	T.P.31 T.P.28 T.P.25	5	abb SG2	bab SG2	bba SG2	b –	b –	b –	b –	b –	b –	b –	b GND	0.3	0.9	1.5	dB
ΔG_{V1}	Relative voltage gain1	Relative to measured values above													-0.4	0	0.4	dB
G_{V2}	Voltage gain2	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG2	bab SG2	bba SG2	b –	b –	a OPEN	0.3	0.9	1.5	dB
ΔG_{V2}	Relative voltage gain2	Relative to measured values above													-0.4	0	0.4	dB
G_{V3}	Voltage gain3	T.P.23	5	b –	a SG2	b –	b –	b –	b –	b –	b –	b –	b –	b GND	-0.4	0.2	0.8	dB
G_{V4}	Voltage gain4	T.P.23	5	b –	b –	b –	b –	b –	b –	a SG2	b –	b –	b –	a OPEN	-0.4	0.2	0.8	dB
F_{C1}	Freq. characteristic1 (100MHz)	T.P.31 T.P.28 T.P.25	5	abb SG4	bab SG4	bba SG4	b –	b –	b –	b –	b –	b –	b –	b GND	-1.0	0	1.0	dB
ΔF_{C1}	Relative Freq. characteristic1 (100MHz)	Relative to measured values above													-1.0	0	1.0	dB
F_{C2}	Freq. characteristic2 (100MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG4	bab SG4	bba SG4	b –	b –	a OPEN	-1.0	0	1.0	dB
ΔF_{C2}	Relative Freq. characteristic2 (100MHz)	Relative to measured values above													-1.0	0	1.0	dB
F_{C3}	Freq. characteristic3 (250MHz)	T.P.31 T.P.28 T.P.25	5	abb SG5	bab SG5	bba SG5	b –	b –	b –	b –	b –	b –	b –	b GND	-3.0	-1.5	1.0	dB
F_{C4}	Freq. characteristic4 (250MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG5	bab SG5	bba SG5	b –	b –	a OPEN	-3.0	-1.5	1.0	dB

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions													Limits			Unit
		Test point (s)	Vcc (V)	Input										SW				
			Vcc	SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW17 Switch	Min.	Typ.	Max.	
C.T.I.1	Crosstalk between two inputs1 (10MHz)	T.P.31 T.P.28 T.P.25	5	abb SG3	bab SG3	bba SG3	b –	b –	b –	b –	b –	b –	b –	GND ↓ OPEN	–	-60	-50	dB
C.T.I.2	Crosstalk between two inputs2 (10MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG3	bab SG3	bba SG3	b –	b –	GND ↓ OPEN	–	-60	-50	dB
C.T.I.3	Crosstalk between two inputs3 (100MHz)	T.P.31 T.P.28 T.P.25	5	abb SG4	bab SG4	bba SG4	b –	b –	b –	b –	b –	b –	b –	GND ↓ OPEN	–	-40	-35	dB
C.T.I.4	Crosstalk between two inputs4 (100MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG4	bab SG4	bba SG4	b –	b –	GND ↓ OPEN	–	-40	-35	dB
C.T.C.1	Crosstalk between channels1 (10MHz)	T.P.31 T.P.28 T.P.25	5	abb SG3	bab SG3	bba SG3	b –	b –	b –	b –	b –	b –	b –	b GND	–	-50	-40	dB
C.T.C.2	Crosstalk between channels2 (10MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG3	bab SG3	bba SG3	b –	b –	a OPEN	–	-50	-40	dB
C.T.C.3	Crosstalk between channels3 (100MHz)	T.P.31 T.P.28 T.P.25	5	abb SG4	bab SG4	bba SG4	b –	b –	b –	b –	b –	b –	b –	b GND	–	-30	-25	dB
C.T.C.4	Crosstalk between channels4 (100MHz)	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	abb SG4	bab SG4	bba SG4	b –	b –	a OPEN	–	-30	-25	dB
Tr1	Pulse characteristic1	T.P.31 T.P.28 T.P.25	5	a SG6	a SG6	a SG6	b –	b –	b –	b –	b –	b –	b –	b GND	–	1.6	2.5	nsec
Tf1		T.P.31 T.P.28 T.P.25	5	a SG6	a SG6	a SG6	b –	b –	b –	b –	b –	b –	b –	b GND	–	1.6	2.5	nsec
Tr2	Pulse characteristic2	T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	a SG6	a SG6	a SG6	b –	b –	a OPEN	–	1.6	2.5	nsec
Tf2		T.P.31 T.P.28 T.P.25	5	b –	b –	b –	b –	b –	a SG6	a SG6	a SG6	b –	b –	a OPEN	–	1.6	2.5	nsec
(HV SW)																		
VoH1	High level output voltage1	T.P.19 T.P.20	5	b –	b –	b –	c 5.0V	c 5.0V	b –	b –	b –	b –	b –	b GND	4.5	5.0	–	V
VoH2	High level output voltage2	T.P.19 T.P.20	5	b –	b –	b –	b –	b –	b –	b –	b –	c 5.0V	c 5.0V	a OPEN	4.5	5.0	–	V
VoL1	Low level output voltage1	T.P.19 T.P.20	5	b –	b –	b –	c 0V	c 0V	b –	b –	b –	b –	b –	b GND	–	0.2	0.5	V
VoL2	Low level output voltage2	T.P.19 T.P.20	5	b –	b –	b –	b –	b –	b –	b –	b –	c 0V	c 0V	a OPEN	–	0.2	0.5	V
Vith1	Input selectional voltage1	T.P.7 T.P.8	5	b –	b –	b –	c Variable	c Variable	b –	b –	b –	b –	b –	b GND	2.0	2.5	3.0	V
Vith2	Input selectional voltage2	T.P.15 T.P.16	5	b –	b –	b –	b –	b –	b –	b –	b –	c Variable	c Variable	a OPEN	2.0	2.5	3.0	V
Trd1	Rising delay time1	T.P.19 T.P.20	5	b –	b –	b –	a SG7	a SG7	b –	b –	b –	b –	b –	b GND	–	100	150	nsec
Trd2	Rising delay time2	T.P.19 T.P.20	5	b –	b –	b –	b –	b –	b –	b –	b –	a SG7	a SG7	a OPEN	–	100	150	nsec
Tfd1	Falling delay time1	T.P.19 T.P.20	5	b –	b –	b –	a SG7	a SG7	b –	b –	b –	b –	b –	b GND	–	50	100	nsec
Tfd2	Falling delay time2	T.P.19 T.P.20	5	b –	b –	b –	b –	b –	b –	b –	b –	a SG7	a SG7	a OPEN	–	50	100	nsec
Vsth1	Switching selectional voltage1	T.P.17	5	a SG1	a SG1	a SG1	a SG7	a SG7	b –	b –	b –	b –	b –	c	0.5	1.5	2.0	V
Vsth2	Switching selectional voltage2	T.P.17	5	b –	b –	b –	b –	b –	a SG1	a SG1	a SG1	a SG7	a SG7	c	0.5	1.5	2.0	V

ELECTRICAL CHARACTERISTICS TEST METHOD

It omits the SW.No accorded with signal input pin because it is already written in Table.

SW A, SW1, SW3, SW5 is in side a if there is not defined specially.

I_{CC1}, I_{CC2} Circuit current (no signal)

The condition is shown as Table 1. Set SW17 to GND (or OPEN) and SW A to side b, measure the current by current meter A. The current is as $I_{CC}1$ ($I_{CC}2$).

V_{DC1}, V_{DC2} Output DC voltage

Set SW17 to GND (or OPEN), measure the DC voltage of T.P.31 (T.P.28, T.P.25) when there is no signal input. The DC voltage is as $V_{DC}1$ (or $V_{DC}2$).

V_{DC3}, V_{DC4} Output DC voltage

Measure the DC voltage of T.P.23 same as note2, the DC voltage is as $V_{DC}3$ (or $V_{DC}4$).

V_{imax1}, V_{imax2} Maximum allowable input

Set SW17 to GND, SG1 as the input signal of Pin 2. Rising up the amplitude of SG1 slowly, read the amplitude of input signal when the output waveform is distorted. The amplitude is as $V_{imax}1$. And measure $V_{imax}1$ when SG2 as the input signal of Pin 4, Pin 6 in same way. Next, set SW to OPEN, measure $V_{imax}2$ when SG2 as the input signal of Pin10, 12, 14.

G_{V1}, ΔG_{V1}, G_{V2}, ΔG_{V2}

1. The condition is shown as Table.
2. Set SW17 to GND, SG2 as the input signal of Pin 2. At this time, read the amplitude output from T.P 31. The amplitude is as $V_{OR}1$.
3. Voltage gain G_V1 is

$$G_V1 = 20 \text{ LOG } \frac{V_{OR}1 \ [V_{P\text{-}P}]}{0.7 \ [V_{P\text{-}P}]} \text{ [dB]}$$

4. The method as same as 2 and 3, measure the voltage gain G_V1 when SG2 as the input signal of Pin 4, 6.
5. The difference of each channel relative voltage gain is as ΔG_V1.
6. Set SW17 to OPEN, measure G_V2, ΔG_V12 in the same way.

G_{V3}, G_{V4}, Voltage gain

1. The condition is shown as table. This test is by active probe.
2. Measure the amplitude output from T.P.23.
3. Measure the G_V3, G_V4 by the same way as G_{V1}, ΔG_{V1}, G_{V2}, ΔG_{V2}.

F_{C1}, ΔF_{C1}, F_{C2}, ΔF_{C2}

1. The condition is shown as table. This test is by active probe.
2. Set SW17 to GND, SG2 as the input signal of Pin 2. Measure the amplitude output from T.P.31. The amplitude is as $V_{OR}1$. By the same way, measure the output when SG4 is as input signal of Pin 2, the output is as $V_{OR}2$.
3. The frequency characteristic F_C1 is

$$F_C1 = 20 \text{ LOG } \frac{V_{OR}2 \ [V_{P\text{-}P}]}{V_{OR}1 \ [V_{P\text{-}P}]} \text{ [dB]}$$

4. The method as same as 2 and 3, measure the frequency F_C1 when input signal to Pin 4, 6.
5. The difference between of each channel frequency characteristic is as ΔF_C1.
6. Set SW17 to OPEN, measure F_C2, ΔF_C2.

F_{C3}, F_{C4} Freq. characteristic

By the same way as Note7 measure the F_C3, F_C4 when SG5 of input signal.

C.T.I.1, C.T.I.2 Crosstalk between two input

1. The condition is shown as Table. This test is by active prove.
2. Set SW17 to GND, SG3 as the input signal of Pin 2. Measure the amplitude output from T.P.31. The amplitude is as $V_{OR}3$.
3. Set SW17 to OPEN, measure the amplitude output from T.P.31. The amplitude is as $V_{OR}3'$.
4. The crosstalk between two inputs C.T.I.1 is

$$\text{C.T.I.1} = 20 \text{ LOG } \frac{V_{OR}3' \ [V_{P\text{-}P}]}{V_{OR}3 \ [V_{P\text{-}P}]} \text{ [dB]}$$

5. By the same way, measure the crosstalk between two inputs when SG3 as the input signal of Pin 4, Pin 6.
6. Next, set SW17 to OPEN, SG3 as the input signal of Pin 10, measure the amplitude output from T.P.31. Theamplitude is as $V_{OR}4$.
7. Set SW17 to GND, measure the amplitude output from T.P.31. The amplitude is as $V_{OR}4'$.
8. The crosstalk between two inputs C.T.I.2 is

$$\text{C.T.I.2} = 20 \text{ LOG } \frac{V_{OR}4' \ [V_{P\text{-}P}]}{V_{OR}4 \ [V_{P\text{-}P}]} \text{ [dB]}$$

9. By the same way, measure the crosstalk between channels when SG3 as the input signal of Pin 12,14.

C.T.I.3, C.T.I.4 Crosstalk between two input

Set SG4 as the input signal, and then the same method as table, measure C.T.I.3, C.T.I.4.

C.T.C.1, C.T.C.2 Crosstalk between channel

1. The condition is as Table. This test is by active prove.
2. Set SW17 to GND, SG3 as the input signal of Pin 2. Measure the amplitude output from T.P.31. The amplitude is as $V_{OR}5$.
3. Next, measure T.P.28, T.P.25 in the same state, and the amplitude is as $V_{OG}5$, $V_{OB}5$.
4. The crosstalk between channels C.T.C.1 is

$$\text{C.T.C.1} = 20 \text{ LOG } \frac{V_{OG}5 \text{ or } V_{OB}5}{V_{OR}5} \text{ [dB]}$$

5. Measure the crosstalk between channels when SG3 is as the input signal of Pin 4, Pin 6 .
6. Next, set SW17 to OPEN, SG3 as the input signal of Pin10, measure the amplitude output from T.P.31. The amplitude is as $V_{OR}6$.
7. Next, measure the amplitude output from T.P.28, T.P.25 in the same state. The amplitude is as $V_{OG}6$, $V_{OB}6$.
8. The crosstalk between channels C.T.C.2 is

$$C.T.C.2 = 20 \log \frac{V_{OG}6 \text{ or } V_{OB}6}{V_{OR}6} \text{ [dB]}$$

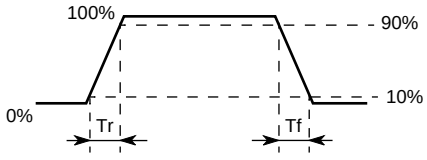
9. By the same way, measure the crosstalk between channels when input signal to Pin12, 14 .

C.T.C.3, C.T.C.4 Crosstalk between channel

Set SG4 as the input signal, and the same method as table, measure C.T.C.3, C.T.C.4.

Tr1, Tf1, Tr2, Tf2 Pulse characteristic

1. The condition is as Table. Set SW17 to GND (or OPEN).
2. The rising of 10% to 90% for input pulse is Tri, the falling of 10% to 90% for input pulse is Tfi.
3. Next, the rising of 10% to 90% for output pulse is Tro, the falling of 10% to 90% for output pulse is Tfo.
4. The pulse characteristic Tr1, Tf1 (Tr2, Tf2) is



$Tr1\ (Tr2) = \sqrt{(Tro)^2 - (Tri)^2}$ (nsec)

$Tf1\ (Tf2) = \sqrt{(Tfo)^2 - (Tfi)^2}$ (nsec)

VoH1, VoH2 High level output voltage

The condition is as Table. Set SW17 to GND (OPEN), input 5V at input terminal. Measure the output voltage, the voltage is as $V_{OH}1$ ($V_{OH}2$).

VoL1, VoL2 Low level output voltage

The condition is as Table. Set SW17 to GND (OPEN), input 0V at input terminal. Measure the output voltage, the voltage is as VoL1 (VoL2).

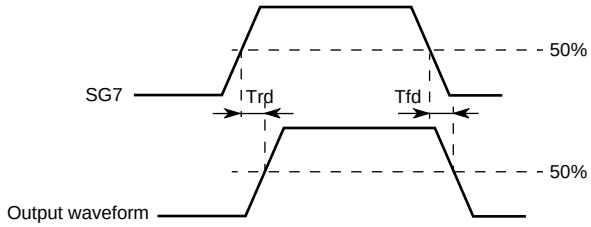
Vith1, Vith2 Input selectional voltage

The condition is as table. Set SW17 to GND (OPEN), increasing gradually the voltage of input terminal from 0V, measure the voltage of input terminal when output terminal is 4.5V. The input voltage is as Vith1 (Vith 2).

Trd1, Trd2 Rising delay time

Tfd1, Tfd2 Falling delay time

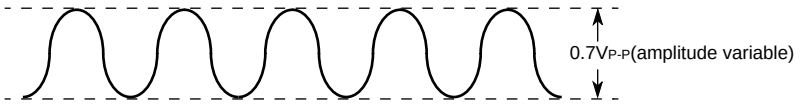
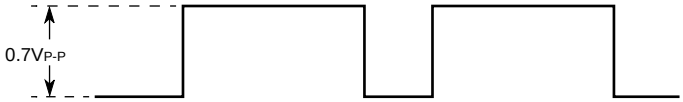
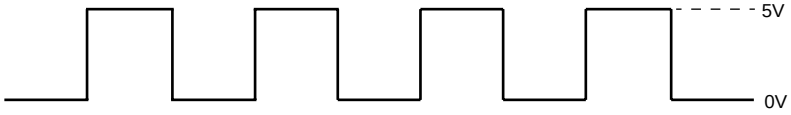
The condition is as table. Set SW17 to GND (OPEN), SG7 is as the input signal of input terminal, measure the waveform of output. Rising delay time is as Trd1 (Trd2). Falling delay time is as Tfd1 (Tfd2). Reference to the Fig. as shown below.



Vsth1, Vsth2 Switching selectional voltage

1. The condition is as table. SG1 is as the input signal of Pin 2, Pin4, Pin6, and SG7 is as the input signal of Pin7, Pin8. There is no input at another pins.
2. Input 0V at Pin17, confirm that there are signals output from T.P.19, T.P.20, T.P.23, T.P.25, T.P.28, T.P.31.
3. Increase gradually the voltage of terminal Pin17. Read the voltage when there is no signal output from the terminals listed as above. The voltage is as Vsth1.
4. SG1 as the input signal of Pin10, Pin12, Pin14, and SG7 as the input signal of Pin15, Pin16. There is no input at another pins.
5. Inputs 5V at Pin17, confirm that there is no signal output from T.P.19, T.P.20, T.P.23, T.P.25, T.P.28, T.P.31.
6. Decreasing gradually the voltage of terminal Pin 17. Read the voltage when there are signals output from the terminals listed as above. The voltage is as Vsth2.

INPUT SIGNAL

SG No.	Signals
SG1	Sine wave (f=60kHz, 0.7V_{P-P}, amplitude variable) 
SG2	Sine wave (f=1MHz, amplitude 0.7V_{P-P})
SG3	Sine wave (f=10MHz, amplitude 0.7V_{P-P})
SG4	Sine wave (f=100MHz, amplitude 0.7V_{P-P})
SG5	Sine wave (f=250MHz, amplitude 0.7V_{P-P})
SG6	Pulse with amplitude 0.7V_{P-P} (f=60kHz, duty80%) 
SG7	Square wave (Amplitude 5.0V_{O-P} TTL, f=60kHz, duty50%) 

NOTE HOW TO USE THIS IC

1. R, G, B input signal is 0.7V_{P-P} of standard video signal.

2. H, V input is 5.0V TTL type.

3. Input signal with sufficient low inpedance to input terminal.

4. The terminal of H, V output pin are shown as Fig.1. It is possible to reduce rise time by insert the resister between Vcc line and H, V output Pin, but set the value of resister in order that the current is under 7.5mA. Setting the value of R is more than 2kΩ as shown in Fig.1.

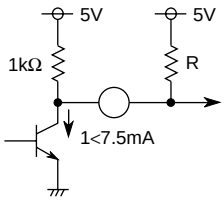


Fig.1

5. The terminal of R,G,B output pin (Pin 25, 28, 31). It is possible to add a pull-up resister according as drive ability. but set the value of resister in order that the current is under 10mA. Setting the value of R is more than 500Ω as shown in Fig.2.

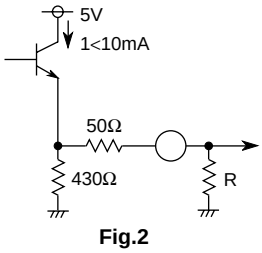


Fig.2

6. Switch (Pin 17) can be changed when this terminal is GND or OPEN

When GND : Signal output from input 1

When OPEN : Signal output from input 2

When the switch is being used as Fig.3

0 to 0.5V : Signal output from input 1

2 to 5V : Signal output from input 2

It is not allowable to set voltage higher than V_{CC}.

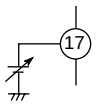


Fig.3

NOTICE OF MAKING PRINTED CIRCUIT BOARD.

Please notice following as shown below. It will maybe cause something oscillation because of the P.C.B. layout of the wide band analog switch.

· The distance between resister and output pin is as short as possible when insert a output pull-down resister.

· The capitance of output terminal as small as possible.

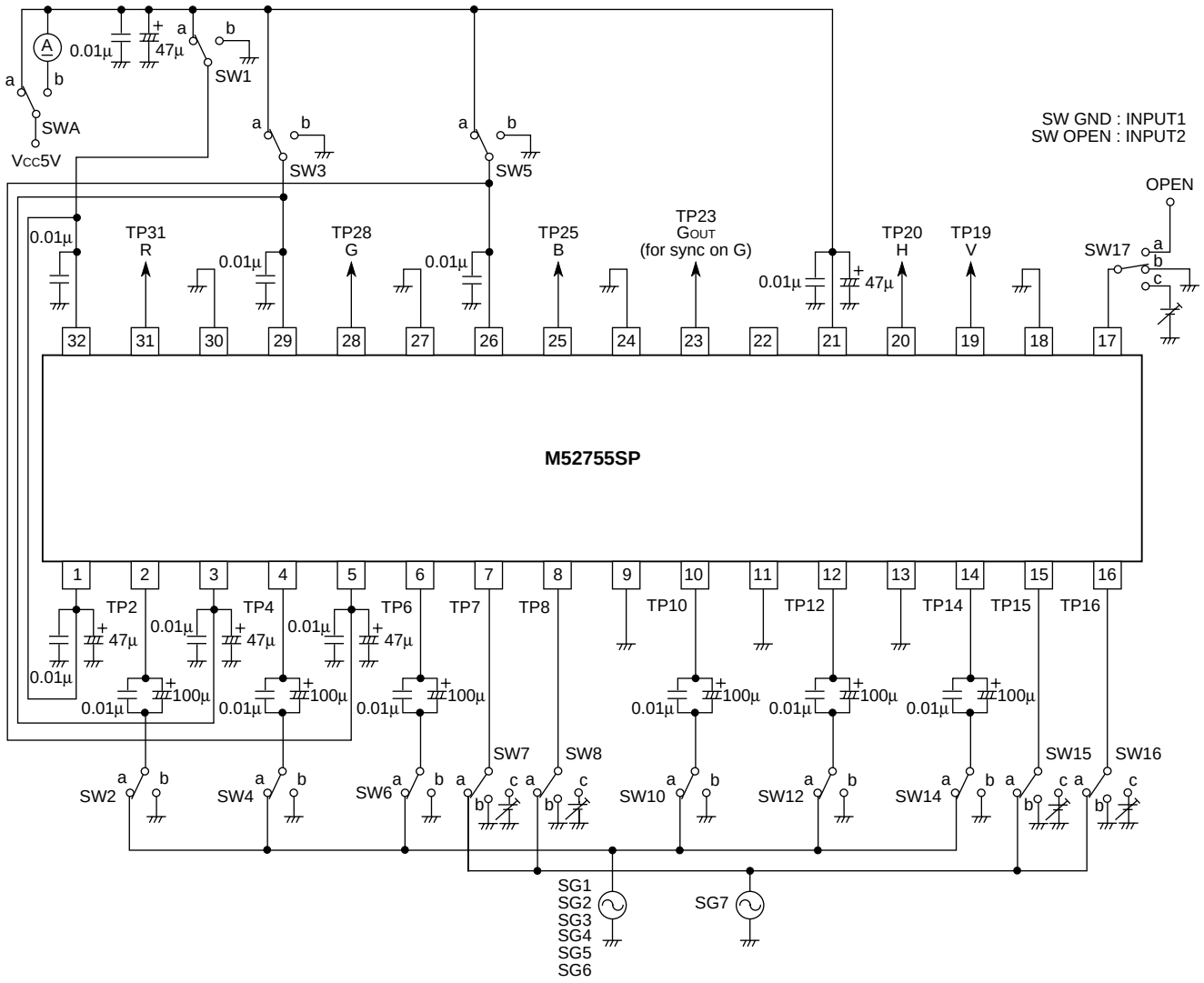
· Set the capitance between Vcc and GND near the pins if possible.

· Using stable power-source (if possible the separated power-source will be better).

· It will reduce the oscillation when add a resister that is tens of ohms between output pin and next stage.

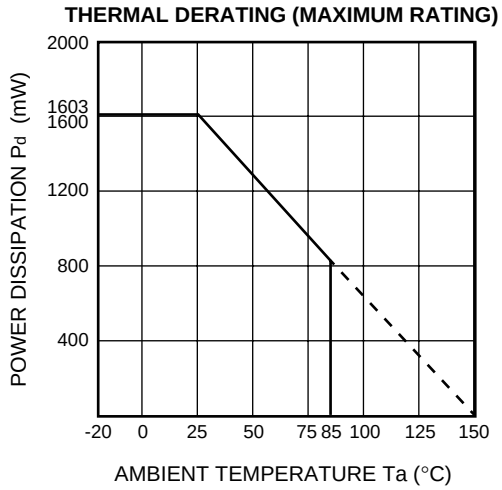
· Assign an area as large as possible for grounding.

TEST CIRCUIT

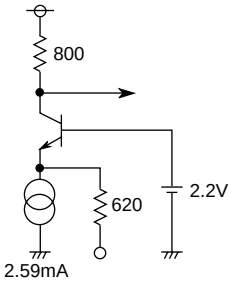
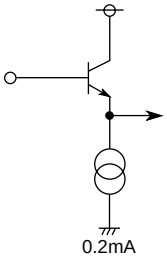
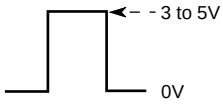


Units Resistance : Ω
Capacitance : F

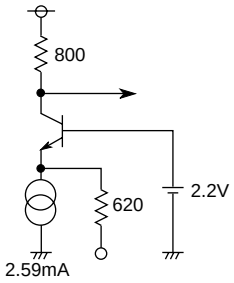
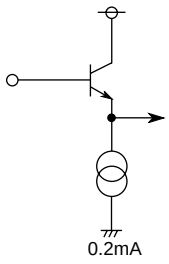
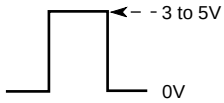
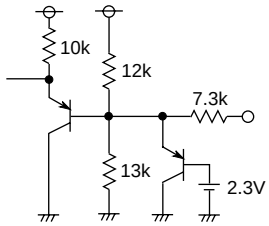
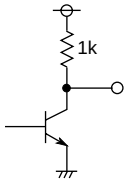
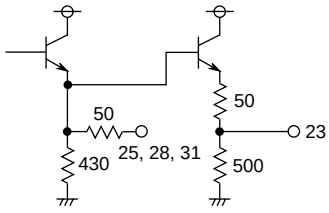
TYPICAL CHARACTERISTICS



DESCRIPTION OF PIN

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Remarks
1 3 5	V_{CC1} (R) V_{CC1} (G) V_{CC1} (B)	5.0	–	
2 4 6	Input1 (R) Input1 (G) Input1 (B)	1.5		Input signal with low impedance.
7 8	Input1 (H) Input1 (V)	–		Input pulse between 3V and 5V. 
9, 11, 13, 18, 24, 27, 30	GND	GND	–	

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Remarks
10 12 14	Input2 (R) Input2 (G) Input2 (B)	1.5		Input signal with low impedance.
15 16	Input2 (H) Input2 (V)	–		Input pulse between 3V and 5V. 
17	Switch	2.6		Switch by OPEN and GND.
19 20	Output (V) Output (H)	–		Output impedance is built-in.
21	Vcc (H, V, Switch)	5	–	
22	NC	–	–	
23 25 28 31	Output (Sync onG) Output (B) Output (G) Output (R)	1.15 2.05		Output impedance is built-in.
26 29 32	Vcc2 (B) Vcc2 (G) Vcc2 (R)	5	–	