

24-BIT SERIAL TO PARALLEL CONVERTER

■ GENERAL DESCRIPTION

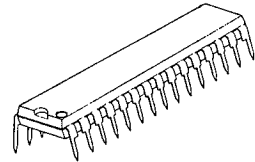
The NJU3719 is a 24-bit serial to parallel converter especially apply to MPU outport expander.

The effective outport assignment of MPU is available as the connection between NJU3719 and MPU is required only 4 lines.

Up to 5MHz signal can be input to the serial data input terminal and the data is output from parallel output buffer through serial in parallel out shift register and parallel data latches.

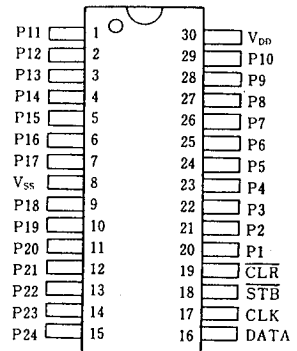
The hysteresis input circuit realized wide noise margin and high drivability output buffer (25mA) can drive LED directly.

■ PACKAGE OUTLINE



NJU3719L

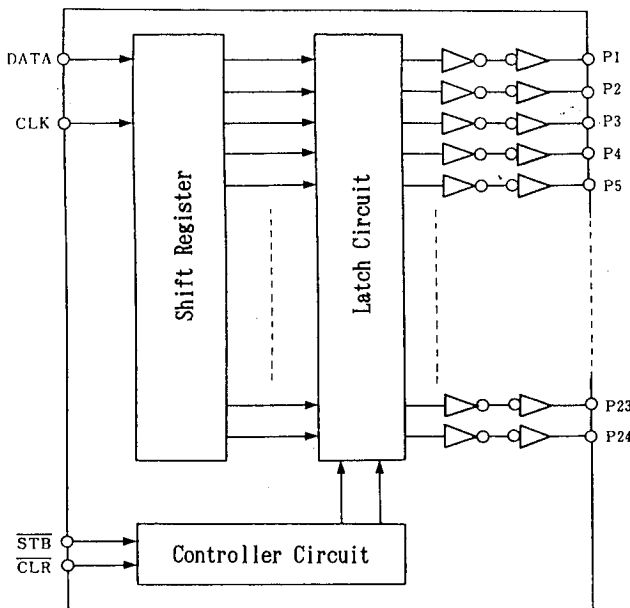
■ PIN CONFIGURATION



7 ■ FEATURES

- 24-Bit Serial In Parallel Out
- Hysteresis Input ----- 0.5V typ
- Operating Voltage ----- 5V±10%
- Operating Frequency ----- 5MHz or more
- Output Current ----- 25mA
- C-MOS Technology
- Package Outline ----- SDIP 30

■ BLOCK DIAGRAM



**■ TERMINAL DESCRIPTION**

NO.	SYMBOL	FUNCTION	NO.	SYMBOL	FUNCTION
1	P11	Parallel Converts Data Output Terminals	16	DATA	Serial Data Input Terminal
2	P12		17	CLK	Clock Signal Input Terminal
3	P13		18	$\overline{\text{STB}}$	Strobe Signal Input Terminal
4	P14		19	$\overline{\text{CLR}}$	Clear Signal Input Terminal
5	P15		20	P1	Parallel Converts Data Output Terminals
6	P16		21	P2	
7	P17		22	P3	
8	V <sub>SS</sub>	23	P4		
9	P18	24	P5		
10	P19	25	P6		
11	P20	26	P7		
12	P21	27	P8		
13	P22	28	P9		
14	P23	29	P10		
15	P24	30	V <sub>DD</sub>	Power Supply Terminal	

**■ FUNCTIONAL DESCRIPTION**
**(1) Reset**

When the "L" level is input to the  $\overline{\text{CLR}}$  terminal, all latches are reset and all parallel conversion output are "L" level.

Normally, the  $\overline{\text{CLR}}$  terminal should be "H" level.

**(2) Data Transmission**

In the  $\overline{\text{STB}}$  terminal is "H" level and input the clock signal to the CLK terminal, the serial data input from DATA terminal shift in the shift register by synchronizing at rising edge of the clock signal.

When the  $\overline{\text{STB}}$  terminal change to "L" level, the data in the shift register transfer to the latch.

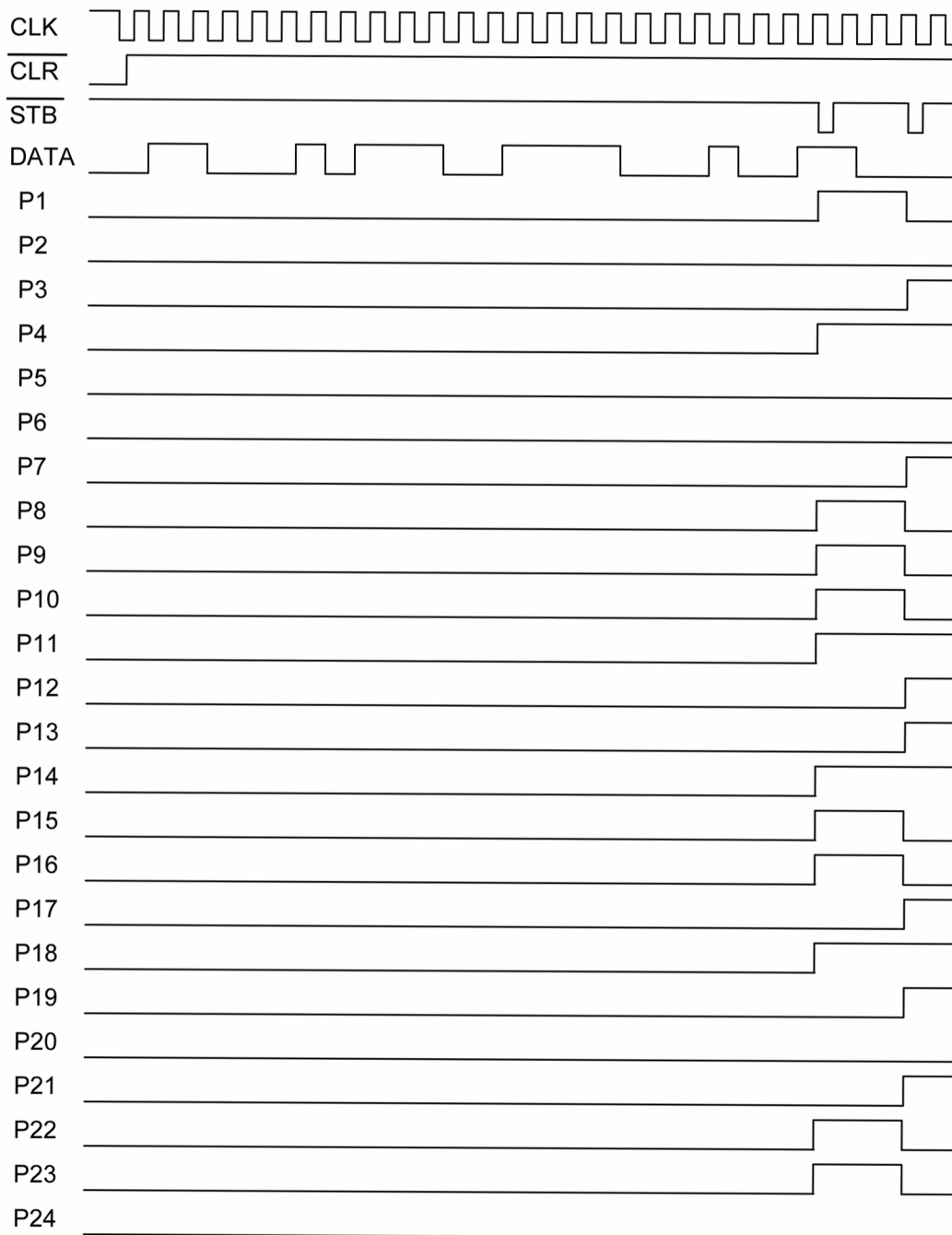
Even if the  $\overline{\text{STB}}$  terminal is "L" level, the input clock signal shift the data in the shift register, therefore, the clock signal control is needed.

Furthermore, the 4 input circuits have a hysteresis characteristics by using the schmitt trigger structure to protect the noise.

CLK	$\overline{\text{STB}}$	$\overline{\text{CLR}}$	OPERATION
X	X	L	All latch are reset (the data in the shift register is no change). All of Parallel convert output are "L".
	H	H	The serial data input from DATA terminal input to the shift register. In this stage, the data in the latch is no change.
L	L	H	The data in the shift register transfer to the latch. And the data in the latch output from parallel output.
H			
	L	H	The CLK input in the $\overline{\text{STB}}="L"$ and $\overline{\text{CLR}}="H"$ state, the data shift in the shift register and latched data also change in accordance with the shift register.

Note ) X: Don't care

## ■ TIMING CHART



## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V <sub>cc</sub>	-0.5 ~ 7.0	V
Input Voltage Range	V <sub>i</sub>	V <sub>ss</sub> -0.5 ~ V <sub>cc</sub> +0.5	V
Output Voltage Range	V <sub>o</sub>	V <sub>ss</sub> -0.5 ~ V <sub>cc</sub> +0.5	V
Output Current	I <sub>o</sub>	±25	mA
Power Dissipation	P <sub>o</sub>	700 (SDIP)	mW
Operating Temperature Range	T <sub>opr</sub>	-25 ~ +85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ +150	°C

**DC ELECTRICAL CHARACTERISTICS**

 ( $V_{DD}=4.5\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Operating Current	$I_{DD5}$	$V_{IH}=V_{DD}$ , $V_{IL}=V_{SS}$			0.1	mA
Input Voltage	High-Level		$0.7V_{DD}$		$V_{DD}$	V
	Low-Level		$V_{SS}$		$0.3V_{DD}$	
Input Leakage Current	$I_{LI}$	$V_I=0\sim V_{DD}$	-10		10	$\mu A$
High-Level Output Voltage	$V_{OHD}$	$I_{OH}=-25mA$ $I_{OH}=-15mA$ $I_{OH}=-10mA$	P1~P24 Terminals (Note 1)	$V_{DD}-1.5$	$V_{DD}$	V
				$V_{DD}-1.0$	$V_{DD}$	
				$V_{DD}-0.5$	$V_{DD}$	
Low-Level Output Voltage	$V_{OLD}$	$I_{OL}=+25mA$ $I_{OL}=+15mA$ $I_{OL}=+10mA$	P1~P24 Terminals (Note 1)	$V_{SS}$	1.5	V
				$V_{SS}$	0.8	
				$V_{SS}$	0.4	
Output Short Current	$I_{OSD}$	$V_O=7V$ , $V_I=0V$	P1~P24 Terminals (Note 2)		20	mA
		$V_O=0V$ , $V_I=7V$			-20	

Note 1) Specified value represent output current per pin. When use, total current consideration and less than power dissipation rating operation should be required.

Note 2)  $V_{DD}=7V$ ,  $V_{SS}=0V$ , 1 second per pin.

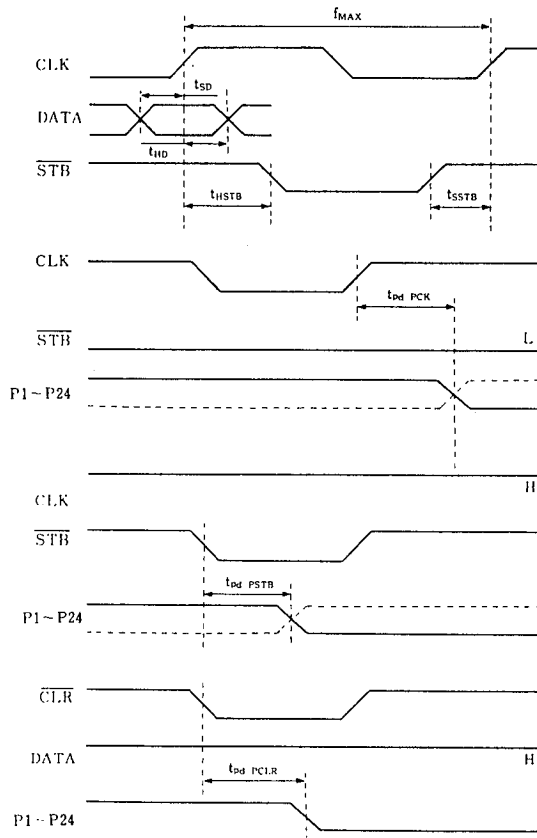
**SWITCHING CHARACTERISTICS**

 ( $V_{DD}=4.5V\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-20\sim 75^\circ C$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Set-Up Time	$t_{SD}$	DATA - CLK	20			ns
Hold Time	$t_{HD}$	CLK - DATA	20			ns
Set-Up Time	$t_{SSTB}$	STB - CLK	30			ns
Hold Time	$t_{HSTB}$	CLK - STB	30			ns
Output Delay Time	$t_{pd\ PCK}$	CLK - P1~P24			100	ns
	$t_{pd\ PSTB}$	STB - P1~P24			80	ns
	$t_{pd\ PCLR}$	CLR - P1~P24			80	ns
Max. Operating Frequency	$f_{MAX}$		5			MHz

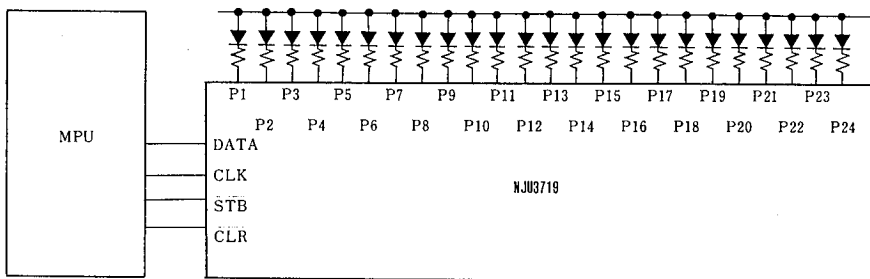
\* )  $C_{OUT}=50pF$

## ■ SWITCHING CHARACTERISTICS TEST WAVEFORM



7

## ■ APPLICATION CIRCUIT



## MEMO

**[CAUTION]**

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