# PHM18NQ15T

TrenchMOS™ standard level FET

**Rev. 01 — 30 January 2003** **Preliminary data**

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHM18NQ15T in SOT685-1 (QLPAK).

### 1.2 Features

- SOT96 (SO-8) footprint compatible
- Surface mount package
- Low thermal resistance
- Low profile.

### 1.3 Applications

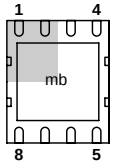
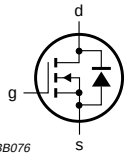
- DC-DC converter primary side switch
- Portable equipment applications.

### 1.4 Quick reference data

- $V_{DS} \leq 150$ V
- $P_{tot} \leq 62.5$ W
- $I_D \leq 17.9$ A
- $R_{DSon} \leq 75$ mΩ.

## 2. Pinning information

**Table 1: Pinning - SOT685-1 (QLPAK), simplified outline and symbol**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1,2,3 | source (s) |  |  |
| 4 | gate (g) | | |
| 5,6,7,8 | drain (d) | | |
| mb | mounting base connected to drain (d) | | |





**SOT685-1 (QLPAK)**

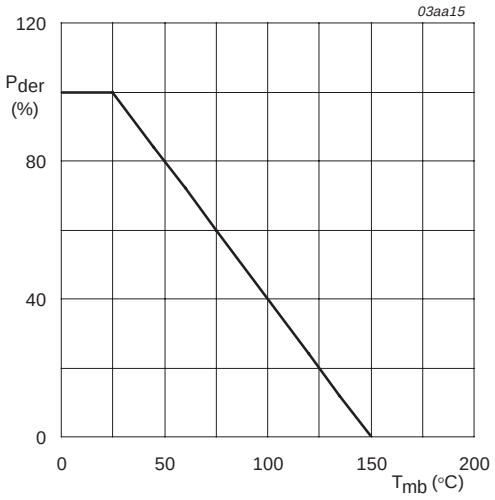
[1] Shaded area indicates pin 1 identifier.

## 3. Limiting values

**Table 2: Limiting values**

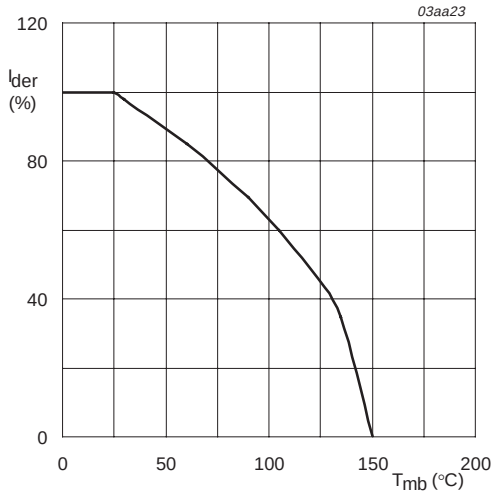
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | 150 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 150 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±20 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | - | 17.9 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | - | 11.3 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | - | 60 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | - | 62.5 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{mb}$ = 25 °C | - | 17.9 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 60 | A |




$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

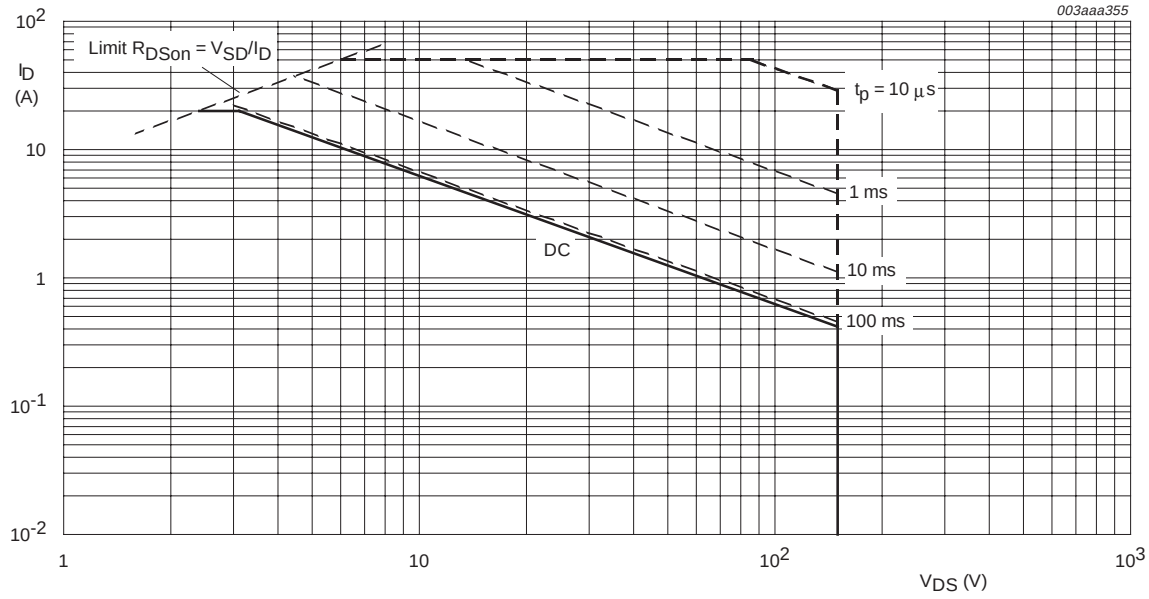
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**




$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

# 4. Thermal characteristics

**Table 3: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 2 | K/W |

## 4.1 Transient thermal impedance

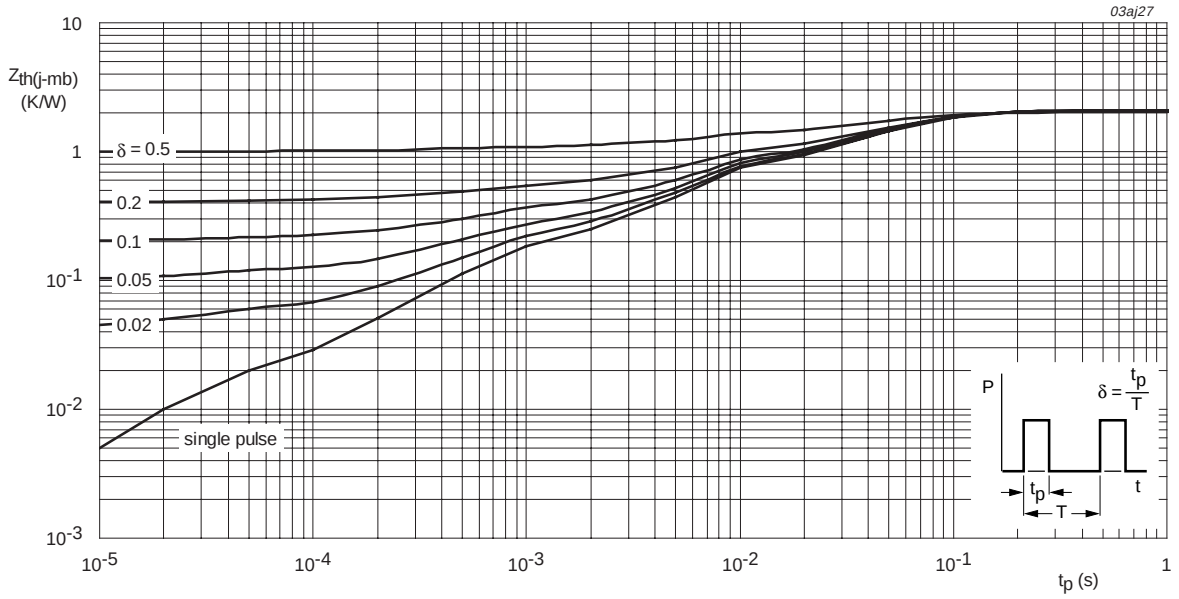


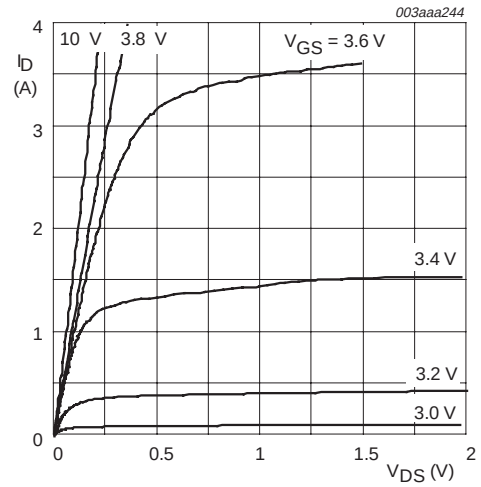

**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

## 5. Characteristics

**Table 4: Characteristics**

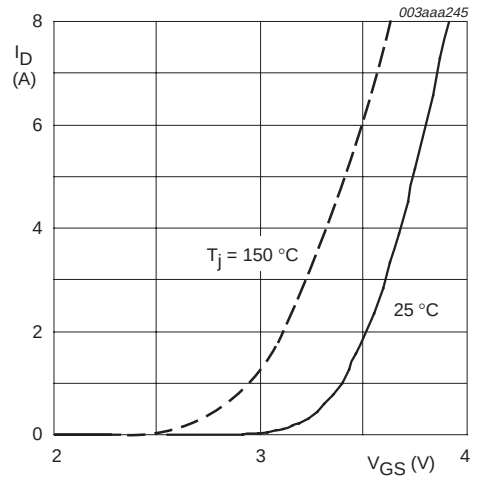
*$T_j$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 150 | - | - | V |
| | | $T_j$ = –55 °C | 134 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 2 | 3 | 4 | V |
| | | $T_j$ = 150 °C | 1.2 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 6 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 120 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1 | µA |
| | | $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±10 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 12 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 56 | 75 | mΩ |
| | | $T_j$ = 150 °C | - | 129 | 173 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 3 A | - | 60 | 80 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 5 A; $V_{DD}$ = 75 V; $V_{GS}$ = 10 V; Figure 13 | - | 29 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 3 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 12 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; Figure 12 | - | 1150 | - | pF |
| $C_{oss}$ | output capacitance | | - | 187 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 61 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 75 V; $I_D$ = 5A; $V_{GS}$ = 10 V; $R_G$ = 6 Ω | - | 12 | - | ns |
| $t_r$ | rise time | | - | 11 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 35 | - | ns |
| $t_f$ | fall time | | - | 18 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 5 A; $V_{GS}$ = 0 V; Figure 11 | - | 0.76 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 5 A; $dI_S/dt$ = –100 A/µs; $V_R$ = 90 V; $V_{GS}$ = 0 V | - | 87 | - | ns |
| $Q_r$ | recovered charge | | - | 162 | - | nC |



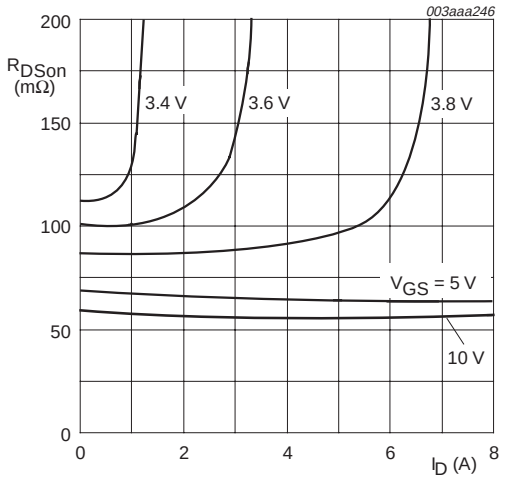

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



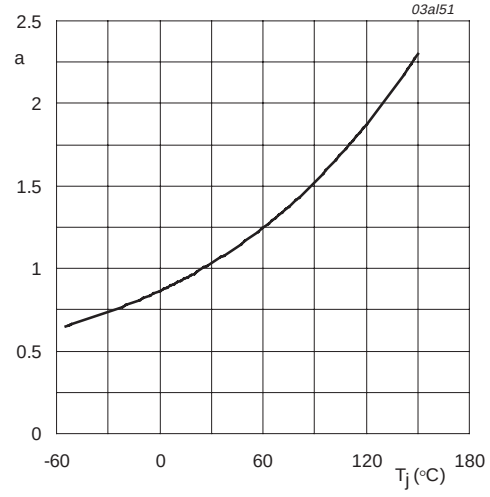

$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



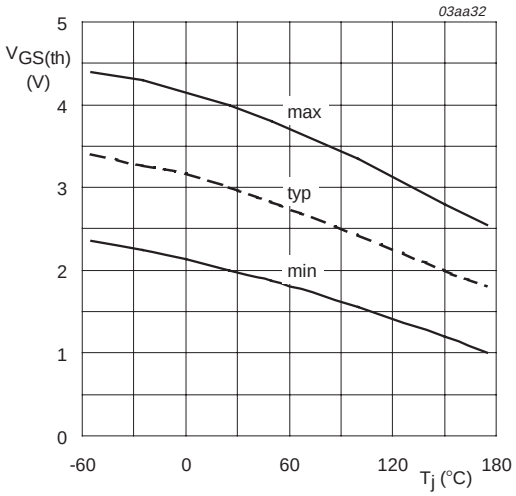

$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



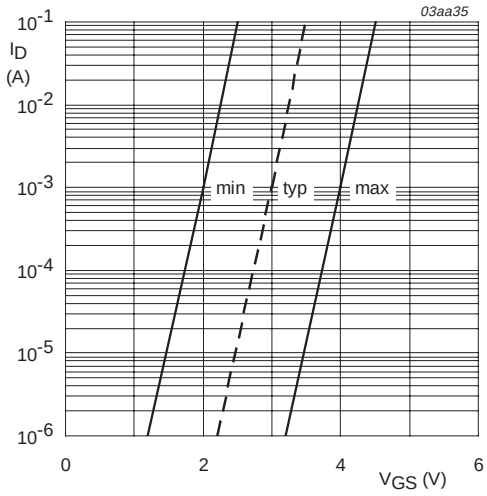

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



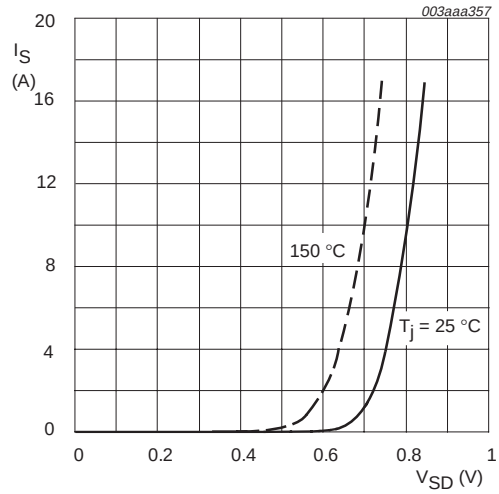

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



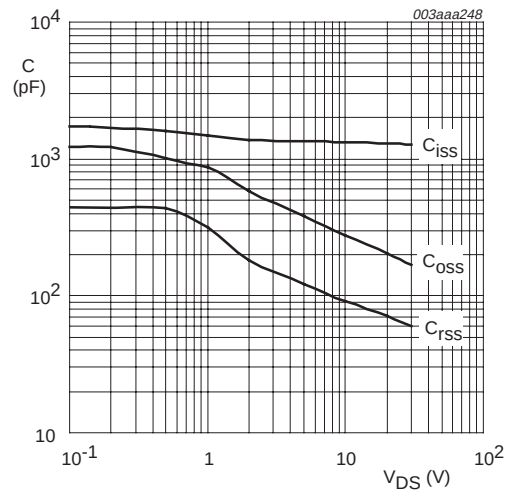

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



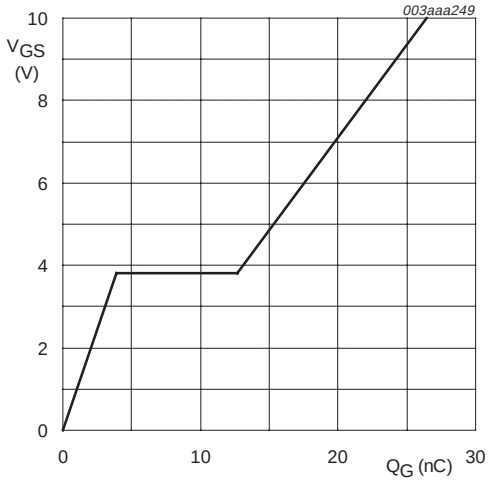

$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**

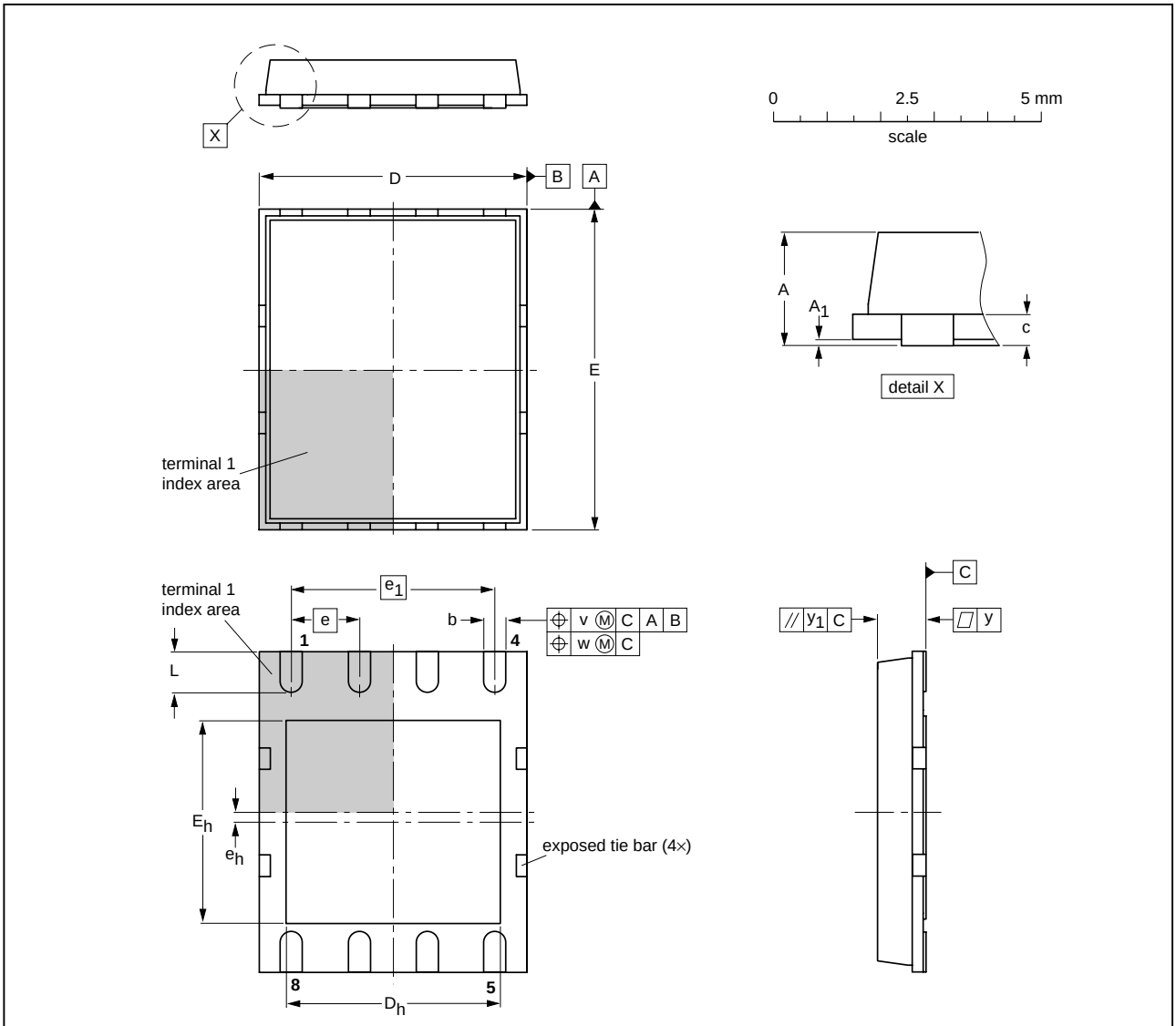



$I_D$ = 5 A; $V_{DD}$ = 75 V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

## 6. Package outline

**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 6 x 5 x 0.85 mm** **SOT685-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_h$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.48<br>0.35 | 0.2 | 5.15<br>4.85 | 4.15<br>3.85 | 6.15<br>5.85 | 3.95<br>3.65 | 1.27 | 3.81 | 0.2 | 0.75<br>0.50 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT685-1 | | - - - | | | | ~~02-05-24~~<br>02-08-12 |

**Fig 14. SOT685-1 (QLPAK).**

# 7. Revision history

Table 5: Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20030130 | - | Preliminary data (9397 750 10877) |

## 8. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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