

HD74LS165A

Parallel-Load 8-bit Shift Register

REJ03D0449-0300
 Rev.3.00
 Jul.15.2005

The LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift / load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift / load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift / load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift / load input independently of the levels of the clock, clock inhibit, or serial inputs.

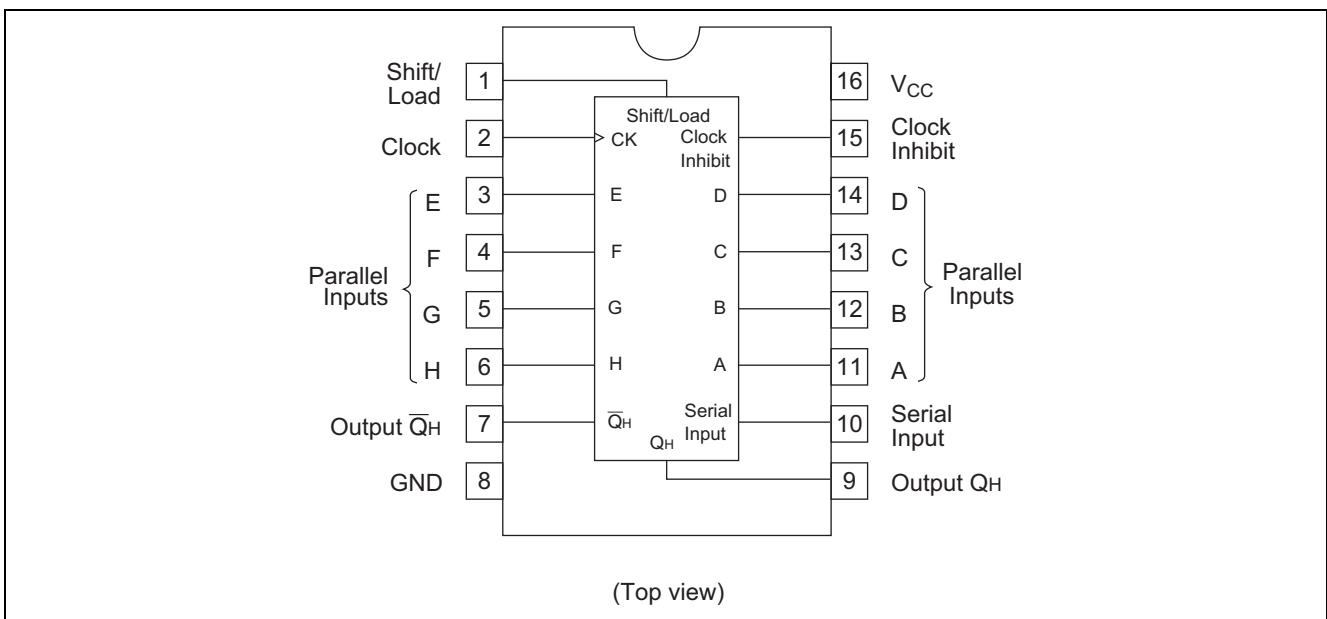
Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|----------------|--------------------|------------------------------|----------------------|--------------------------------|
| HD74LS165AP | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74LS165AFPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement

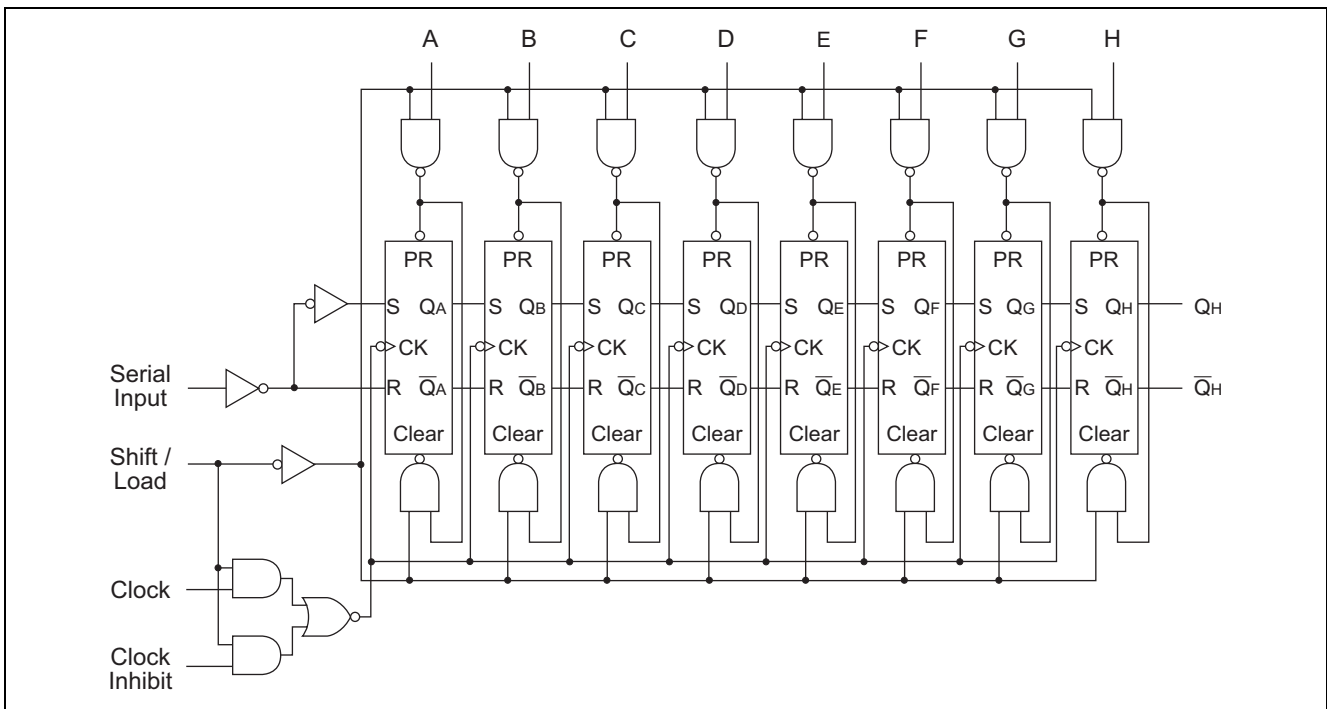


Function Table

| Shift / Load | Clock Inhibit | Inputs | | | Internal outputs | | Output Q _H |
|--------------|---------------|--------|--------|----------------|------------------|-----------------|-----------------------|
| | | Clock | Serial | Parallel A...H | Q _A | Q _B | |
| L | X | X | X | a...h | a | b | h |
| H | L | ↑ | X | X | Q _{A0} | Q _{B0} | Q _{H0} |
| H | L | ↑ | H | X | H | Q _{An} | Q _{Gn} |
| H | L | ↑ | L | X | L | Q _{An} | Q _{Gn} |
| H | H | X | X | X | Q _{A0} | Q _{B0} | Q _{H0} |

- Notes:
1. H; high level, L; low level, X; irrelevant
 2. ↑; transition from low to high level
 3. a to h; the level of steady-state input at inputs A to H respectively
 4. Q_{A0} to Q_{H0}; the level of Q_A to Q_H, respectively, before the indicated steady-state input conditions were established.
 5. Q_{An} to Q_{Gn}; the level of Q_A to Q_G, respectively, before the most recent ↓ transition of the clock.

Block Diagram



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---------------------|------------------|-------------|------|
| Supply voltage | V _{CC} | 7 | V |
| Input voltage | V _{IN} | 7 | V |
| Power dissipation | P _T | 400 | mW |
| Storage temperature | T _{stg} | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|---------------------------|---------------|------|------|------|-------------|
| Supply voltage | V_{CC} | 4.75 | 5.00 | 5.25 | V |
| Output current | I_{OH} | — | — | -400 | μA |
| | I_{OL} | — | — | 8 | mA |
| Operating temperature | T_{opr} | -20 | 25 | 75 | $^{\circ}C$ |
| Clock frequency | f_{clock} | 0 | — | 25 | MHz |
| Clock pulse width | $t_w (clock)$ | 25 | — | — | ns |
| Load pulse width | $t_w (load)$ | 15 | — | — | ns |
| Clock enable setup time | t_{su} | 30 | — | — | ns |
| Parallel input setup time | t_{su} | 10 | — | — | ns |
| Serial input setup time | t_{su} | 20 | — | — | ns |
| Shift setup time | t_{su} | 45 | — | — | ns |
| Hold time | t_h | 0 | — | — | ns |

Electrical Characteristics

($T_a = -20$ to $+75^{\circ}C$)

| Item | | Symbol | min. | typ.* | max. | Unit | Condition |
|------------------------------|--------------|----------|------|-------|------|---------|--|
| Input voltage | | V_{IH} | 2.0 | — | — | V | |
| | | V_{IL} | — | — | 0.8 | V | |
| Output voltage | | V_{OH} | 2.7 | — | — | V | $V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -400 \mu A$ |
| | | V_{OL} | — | — | 0.4 | V | $I_{OL} = 4 mA$ |
| Input current | Shift / Load | I_i | — | — | 0.3 | mA | $V_{CC} = 5.25 V, V_i = 7 V$ |
| | Other inputs | | — | — | 0.1 | mA | |
| High level input current | Shift / Load | I_{IH} | — | — | 60 | μA | $V_{CC} = 5.25 V, V_i = 2.7 V$ |
| | Other inputs | | — | — | 20 | μA | |
| Low level input current | Shift / Load | I_{IL} | — | — | -1.2 | mA | $V_{CC} = 5.25 V, V_i = 0.4 V$ |
| | Other inputs | | — | — | -0.4 | mA | |
| Short-circuit output current | | I_{OS} | -20 | — | -100 | mA | $V_{CC} = 5.25 V$ |
| Supply current** | | I_{CC} | — | 21 | 36 | mA | $V_{CC} = 5.25 V$ |
| Input clamp voltage | | V_{IK} | — | — | -1.5 | V | $V_{CC} = 4.75 V, I_{IN} = -18 mA$ |

Note: * $V_{CC} = 5 V, T_a = 25^{\circ}C$

** With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift / load, I_{CC} is measured with the parallel inputs at 4.5 V, than with the parallel inputs grounded.

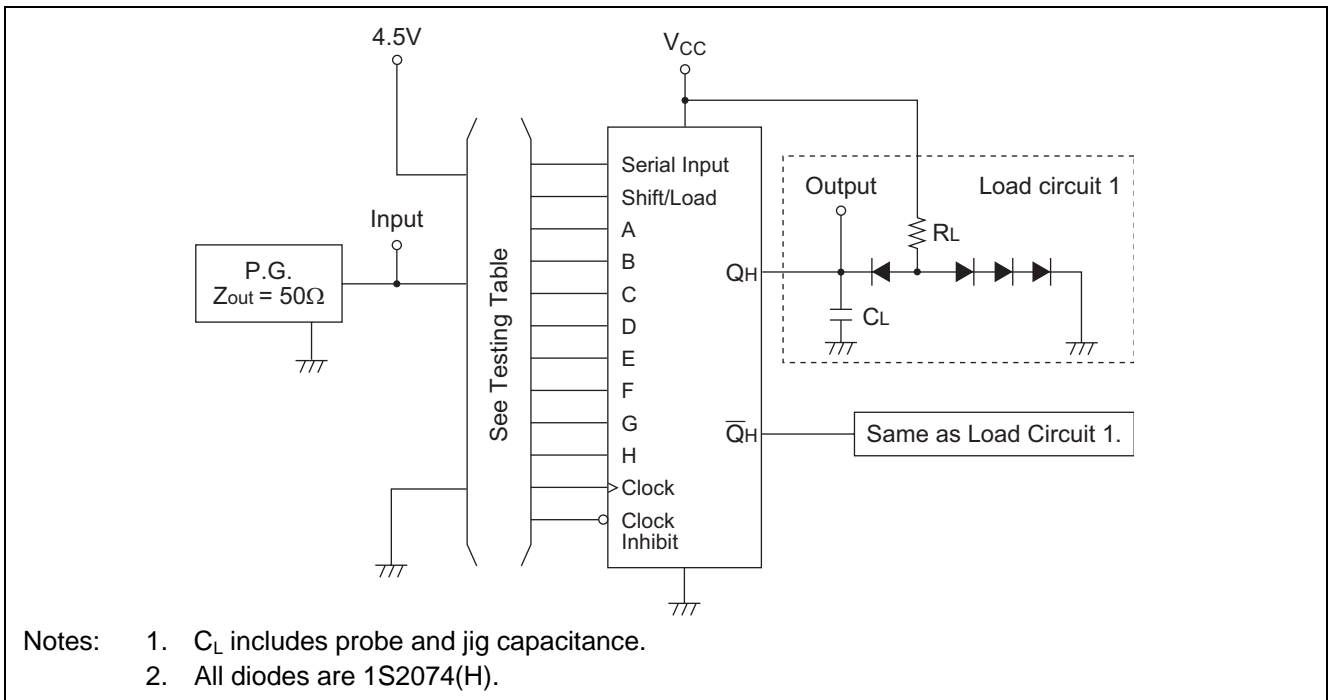
Switching Characteristics

($V_{CC} = 5 V, T_a = 25^{\circ}C$)

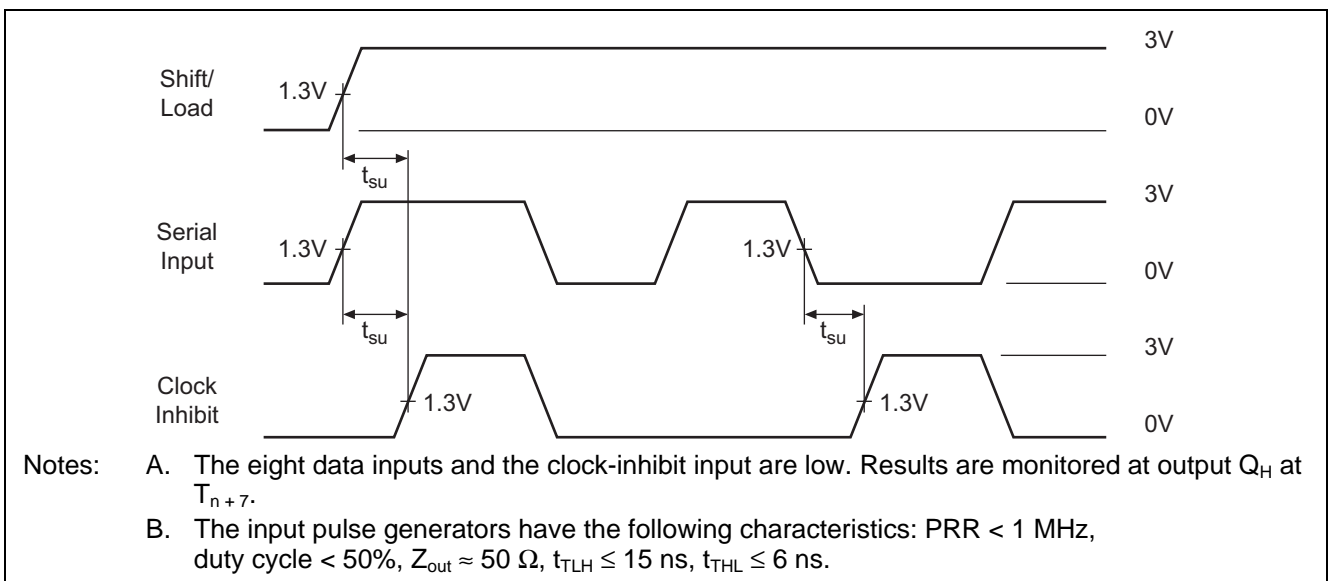
| Item | Symbol | Inputs | Outputs | min. | typ. | max. | Unit | Condition |
|-------------------------|-----------|--------|---------|------|------|------|------|--------------------------------|
| Maximum clock frequency | f_{max} | | | 25 | 35 | — | MHz | $C_L = 15 pF, R_L = 2 k\Omega$ |
| Propagation delay time | t_{PLH} | Load | Any | — | 21 | 35 | ns | |
| | t_{PHL} | | | — | 26 | 35 | ns | |
| | t_{PLH} | Clock | Any | — | 14 | 25 | ns | |
| | t_{PHL} | | | — | 16 | 25 | ns | |
| | t_{PLH} | H | Q_H | — | 13 | 25 | ns | |
| | t_{PHL} | | | — | 24 | 30 | ns | |
| | t_{PLH} | H | Q_H | — | 19 | 30 | ns | |
| | t_{PHL} | | | — | 17 | 25 | ns | |

Testing Method

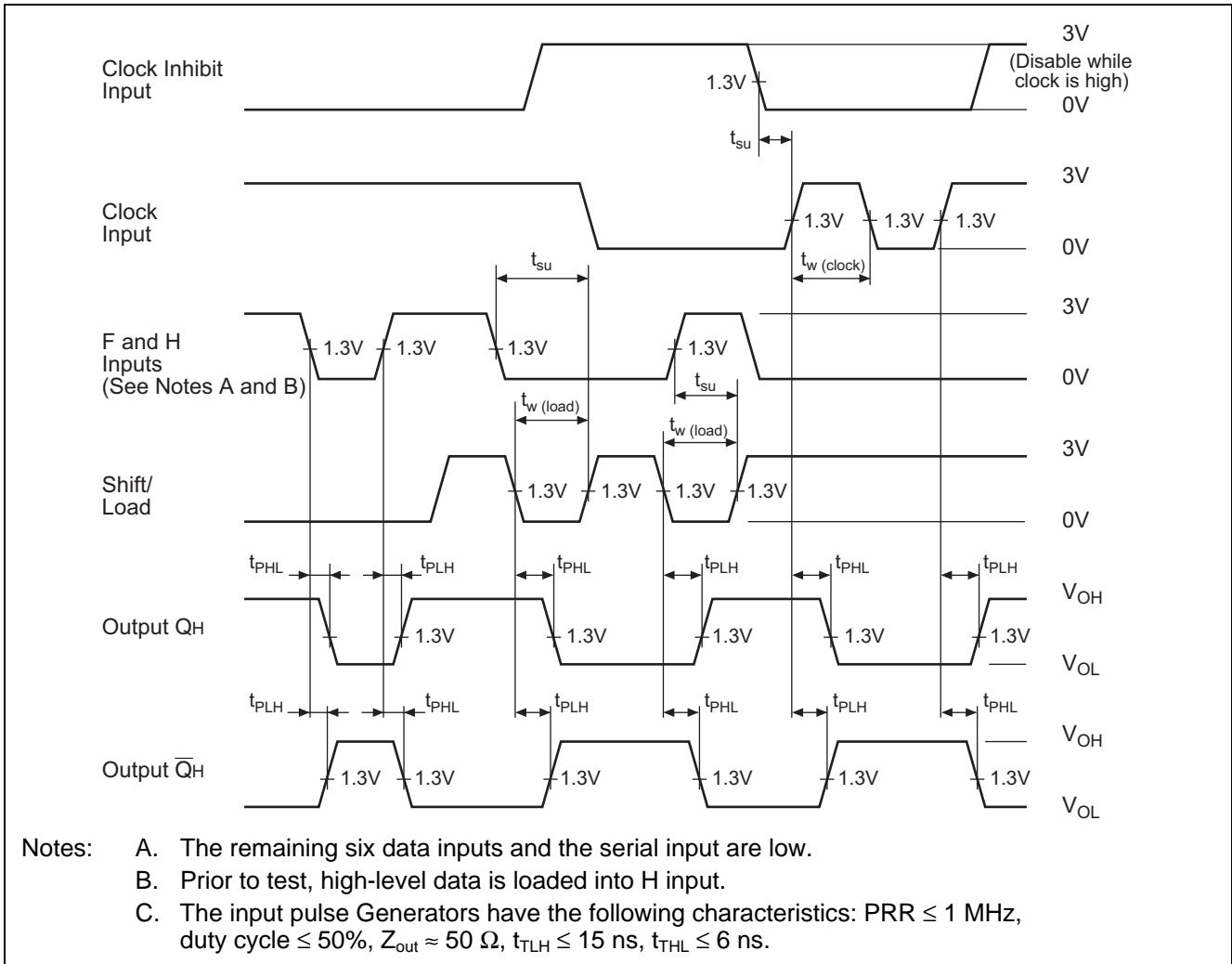
Test Circuit



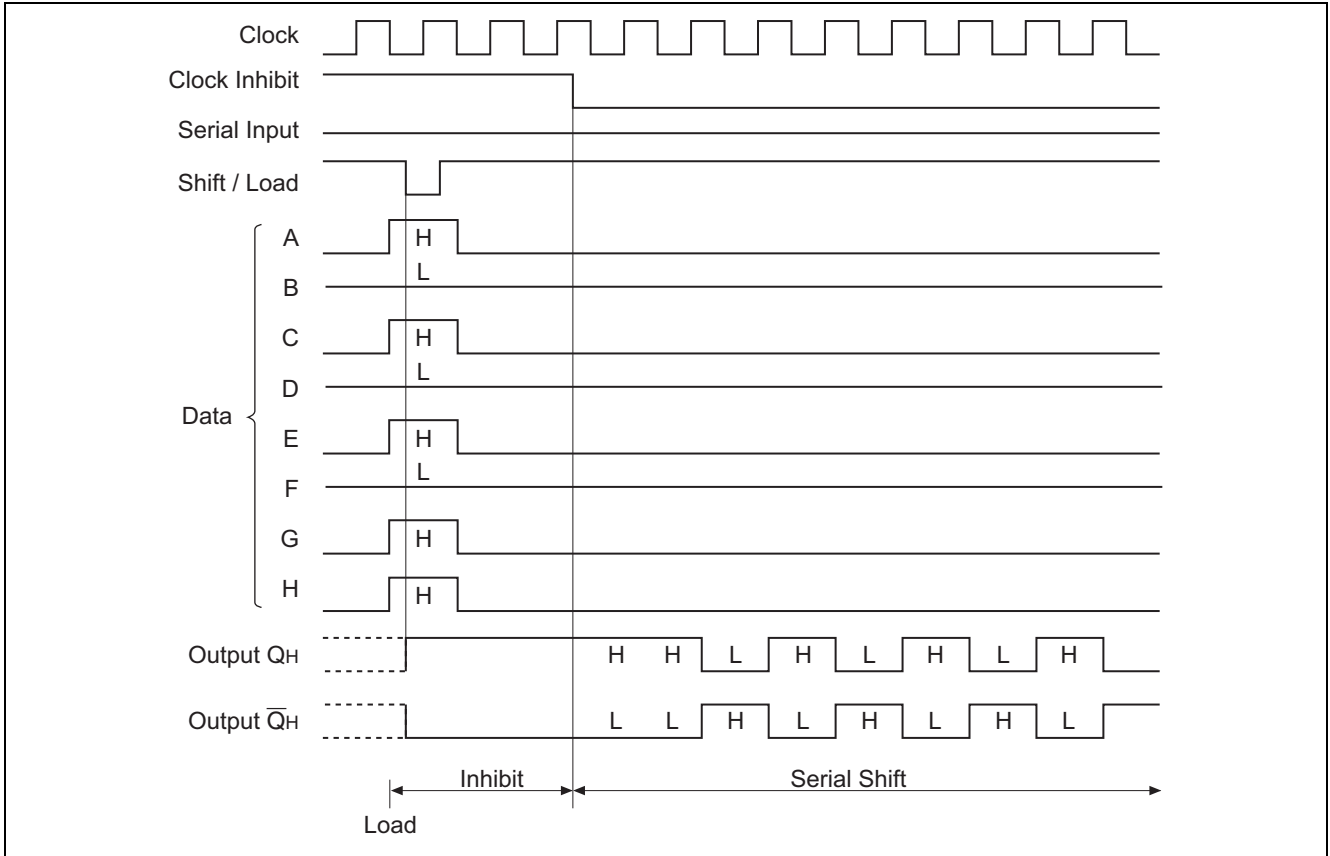
Waveforms 1



Waveforms 2

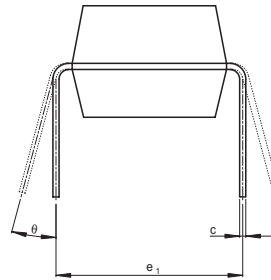
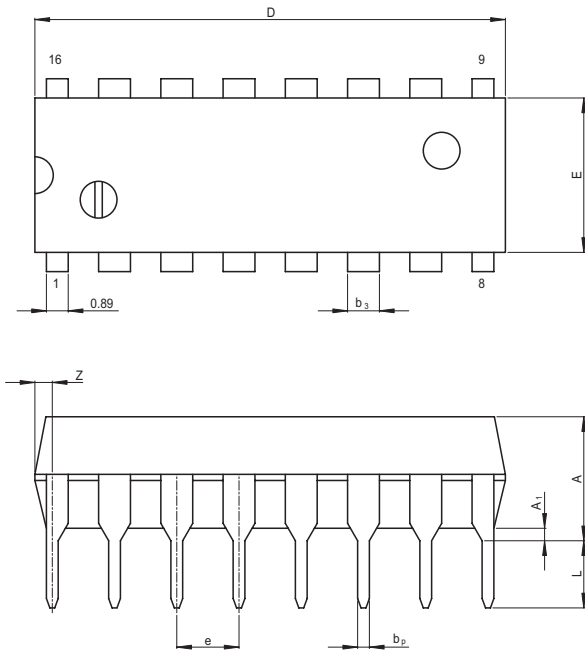


Typical Shift, Load and Inhibit Sequences



Package Dimensions

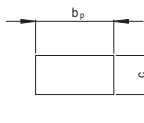
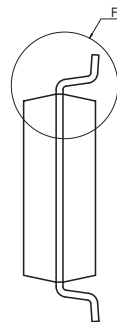
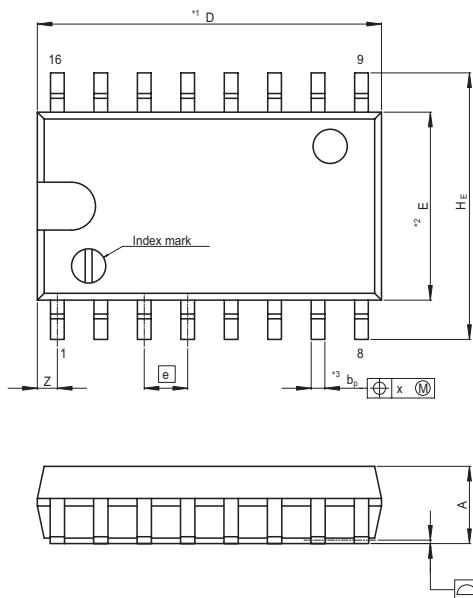
| | | | |
|-----------------------|--------------|---------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-DIP16-6.3x19.2-2.54 | PRDP0016AE-B | DP-16FV | 1.05g |



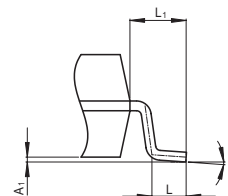
(Ni/Pd/Au plating)

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|-------|
| | Min | Nom | Max |
| e ₁ | — | 7.62 | — |
| D | — | 19.2 | 20.32 |
| E | — | 6.3 | 7.4 |
| A | — | — | 5.06 |
| A ₁ | 0.51 | — | — |
| b _p | 0.40 | 0.48 | 0.56 |
| b ₃ | — | 1.30 | — |
| c | 0.19 | 0.25 | 0.31 |
| θ | 0° | — | 15° |
| e | 2.29 | 2.54 | 2.79 |
| Z | — | — | 1.12 |
| L | 2.54 | — | — |

| | | | |
|------------------------|--------------|---------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-B | FP-16DAV | 0.24g |



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.50 | — |
| A ₂ | — | — | — |
| A ₁ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| b _p | 0.34 | 0.40 | 0.46 |
| b ₁ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 7.50 | 7.80 | 8.00 |
| a | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| L ₁ | — | 1.15 | — |

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