

Features

- **1.5 Gbps Bi-directional Transceiver**
 - Compliant with Serial ATA Gen1 Revision 1.0a Specification
- **Low Power Operation**
 - 75 mW per Channel Nominal
- **Key Blocks Include**
 - Integrated OOB Processor
 - K28.5 COMMA Detection
 - Digital Clock and Data Recovery (CDR) with Digital Equalization
 - Spread Spectrum Clocking
 - Optional 8B/10B Encoder and Decoder
- **Parallel I/O**
 - Synchronous 8-bit/10-bit Parallel Interface @ 150 MHz
- **Serial I/O**
 - Programmable Pre-emphasis
 - Support for Spread Spectrum Clocking
 - Integrated 100Ω Matched Differential Termination
 - AC and DC Coupling Support
- **Test Features**
 - Far-end and Near-end Loopback Support
 - At Speed BIST

Overview

The AT78C5091 is a 1-channel SATA PHY supporting Gen 1 speeds of 1.5 Gbps. The IP has been designed based on the requirements stated in the Serial ATA Standard, Rev 1.0a, Jan 2003.

On the transmit path, parallel data is registered, passed through a transmit FIFO to compensate for phase differences between the link and PHY clocks, 8B/10B encoded and then passed out via a high speed serializer using a spread spectrum clock. Built-in flexibility permits bypassing the encoding block in addition to optionally disabling the spread spectrum clocking. The user can control the transmit buffer output swing and pre-emphasis levels via direct input signals.

On the receive path, the AT78C5091 performs the serial-to-parallel conversion, using a high bandwidth clock and data recovery (CDR) block. The recovered data is then passed through a comma alignment block and an optional 8B/10B decode block before being passed to the phyCtrl layer via a parallel interface. This interface is synchronous to the recovered clock.

The PHY core has an out of band (OOB) processor. As specified by the Serial ATA standard, three out of band (OOB) signals are used/detected by the PHY, namely COMRESET, COMINIT, and COMWAKE. Each of these signals are indicated by a number of bursts of four ALIGN primitives followed by defined idle periods during which the differential voltage on the serial line is null. OOB signals are observed by detecting the temporal spacing between adjacent bursts of activity.

Test functions including BIST, scan, parallel and serial loopback modes are configured and controlled by the use of direct input signals. Similarly, error/status bits are indicated through direct output signals such as bistErr.



1-channel Serial ATA PHY

AT78C5091

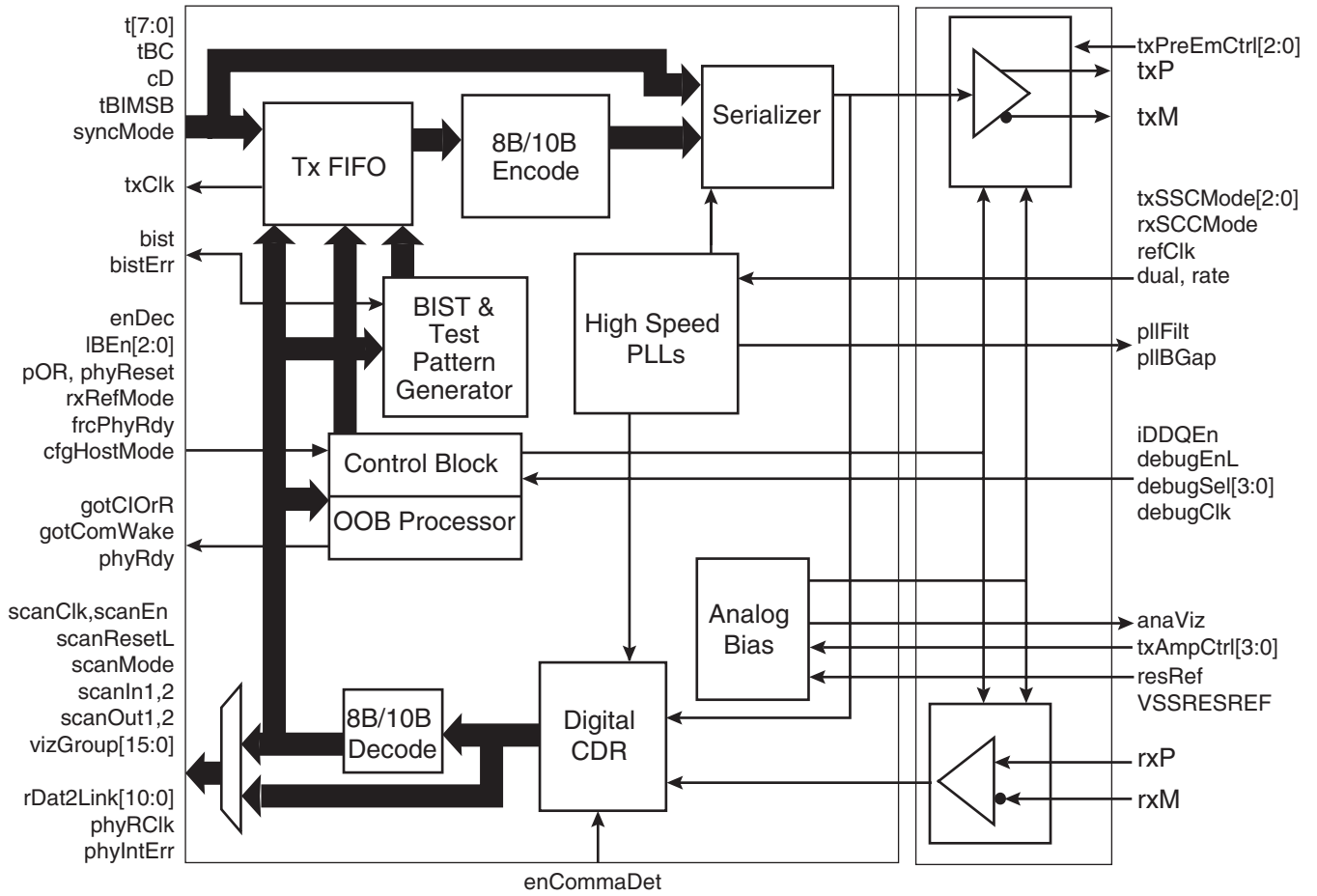
Summary

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Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Block Diagram





Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests

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