NCV4264

150 mA Low Dropout Linear Regulator

The NCV4264 is a wide input range, precision fixed output, low dropout integrated voltage regulator with a full load current rating of 150 mA.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 500 mV at 100 mA load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

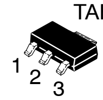
Features

- 5.0 V Fixed Output
- ±2.0% Output Accuracy, Over Full Temperature Range
- Quiescent Current 400 μA at I_{OUT} = 1.0 mA
- 500 mV Maximum Dropout Voltage at 100 mA Load Current
- Wide Input Voltage Operating Range of 5.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- AEC−Q100 Qualified
- This is a Pb−Free Device

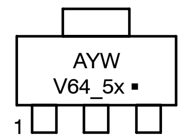
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

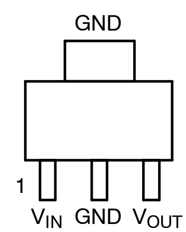


SOT−223
ST SUFFIX
CASE 318E



A	= Assembly Location
Y	= Year
W	= Work Week
V64_5x	= Specific Device Code
x	= 5 (5.0 V)
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

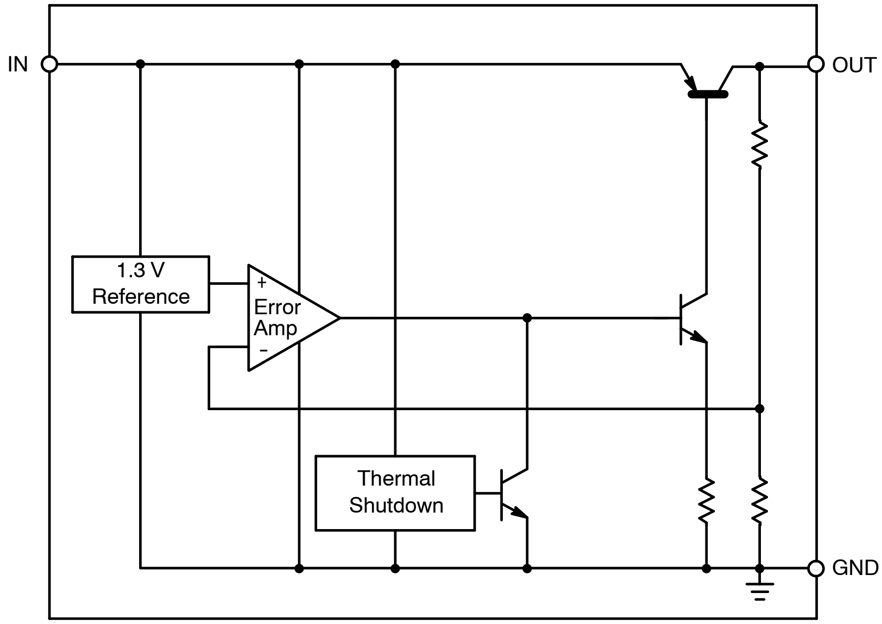


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function
1	V_{IN}	Unregulated input voltage; 5.5 V to 45 V.
2	GND	Ground; substrate.
3	V_{OUT}	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	GND	Ground; substrate and best thermal connection to the die.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Input Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+16	V
Storage Temperature	T_{stg}	−55	+150	°C
Moisture Sensitivity Level	MSL	1		–
ESD Capability, Human Body Model (Note 1)	V_{ESDHB}	4000	–	V
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	–	V
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 2)	T_{sld}	–	265 pk	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, DC Input Operating Voltage	V_{IN}	5.5	+45	V
Junction Temperature Operating Range	T_J	−40	+150	°C

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)
2. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction−to−Ambient	SOT−223	$R_{\theta JA}$		–	99 (Note 3)	°C/W
Junction−to−Case	SOT−223	$R_{\theta JC}$		–	17	

ELECTRICAL CHARACTERISTICS (V_{IN} = 13.5 V, Tj = −40°C to +150°C, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	5.0 mA ≤ I_{OUT} ≤ 100 mA (Note 4) 6.0 V ≤ V_{IN} ≤ 28 V	4.900	5.000	5.100	V
Line Regulation	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 6.0 V ≤ V_{IN} ≤ 28 V	−30	5.0	+30	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	5.0 mA ≤ I_{OUT} ≤ 100 mA (Note 4)	−40	5.0	+40	mV
Dropout Voltage	V_{IN}–V_{OUT}	I_{OUT} = 100 mA (Notes 4 & 5)	–	275	500	mV
Quiescent Current	I_q	I_{OUT} = 1.0 mA	–	83	400	μA
Active Ground Current	$I_{G(ON)}$	I_{OUT} = 50 mA (Note 4)	–	1.5	15	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 V_{P-P}, F = 100 Hz	–	67	–	dB
Output Capacitor for Stability	C_{OUT} ESR	I_{OUT} = 1.0 mA to 100 mA (Notes 4)	10	–	 9.0	μF Ω

PROTECTION

Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 4.5 V (Note 4)	150	–	500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 4)	40	–	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 6)	150	–	200	°C

3. 1 oz., 100 mm^2 copper area.
4. Use pulse loading to limit power dissipation.
5. Dropout voltage = (V_{IN}–V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.

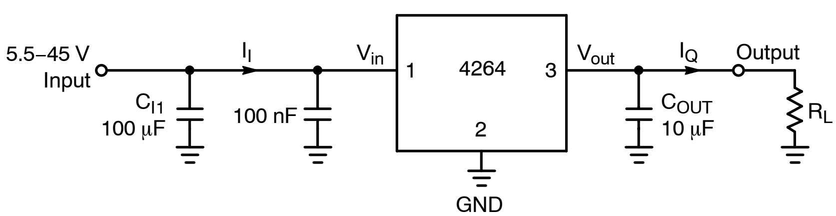


Figure 2. Measurement Circuit

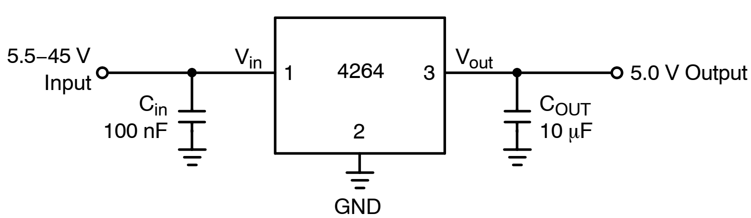


Figure 3. Applications Circuit

TYPICAL CHARACTERISTIC CURVES

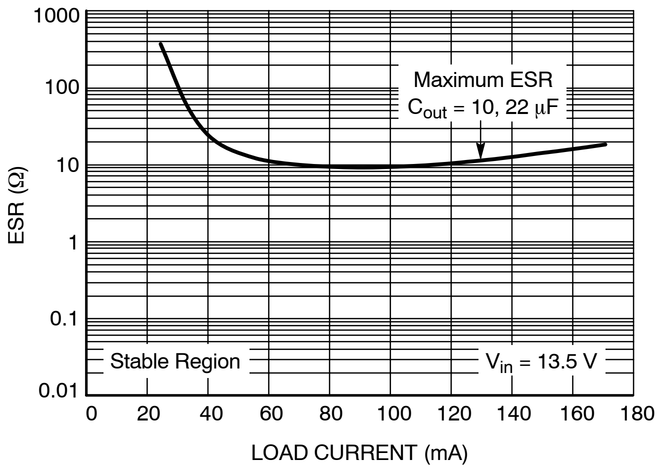


Figure 4. ESR Characterization

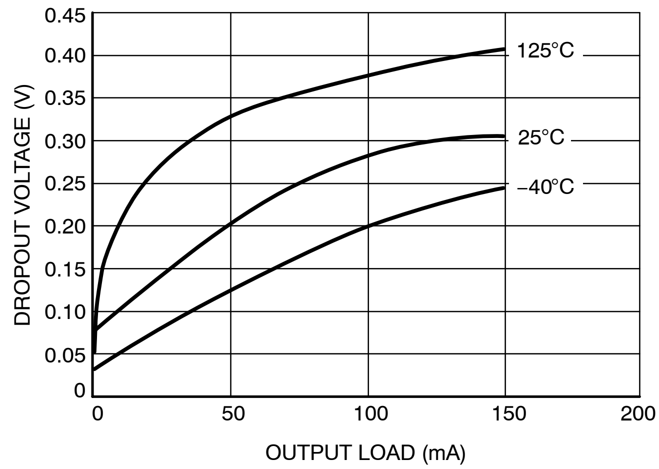


Figure 5. Dropout Voltage vs. Output Load

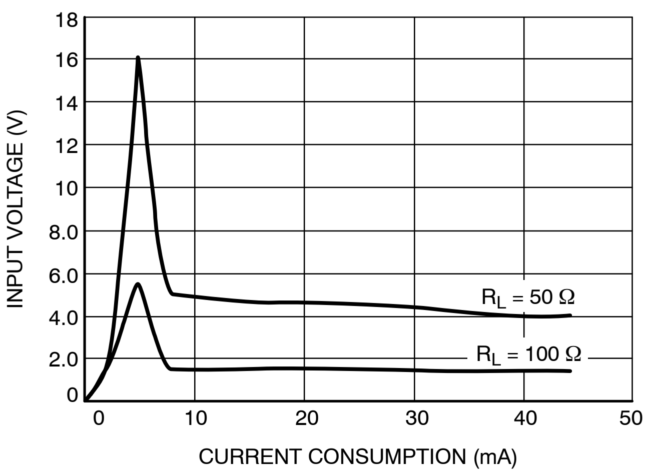


Figure 6. Current Consumption vs. Input Voltage

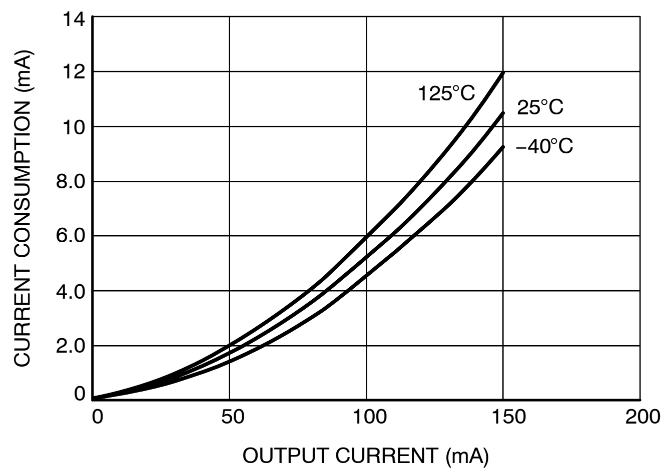


Figure 7. Current Consumption vs. Output Current

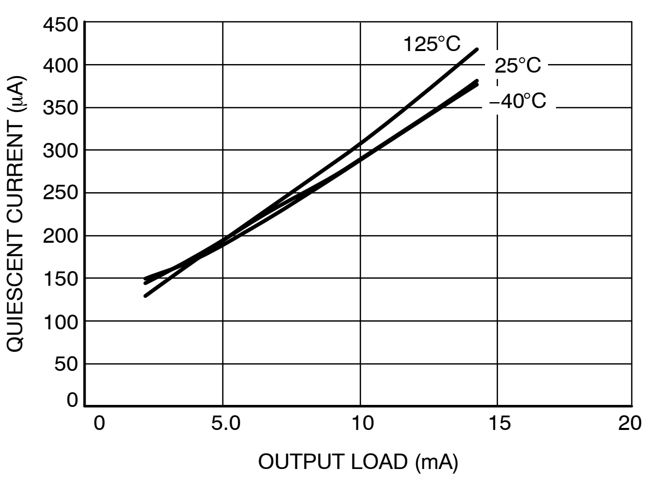


Figure 8. Quiescent Current vs. Output Load

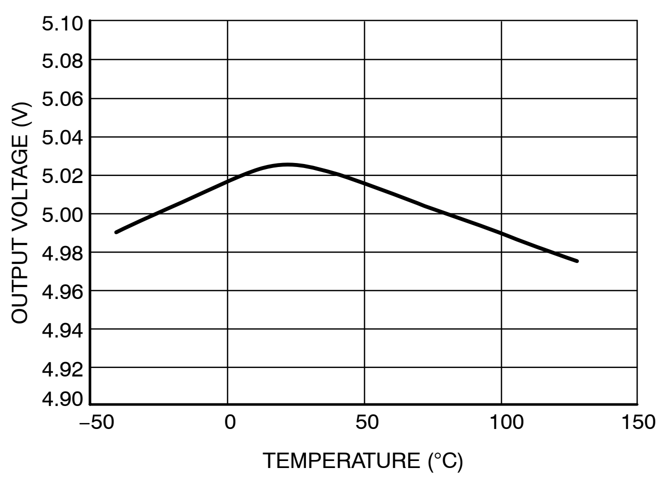


Figure 9. Output Voltage vs. Temperature

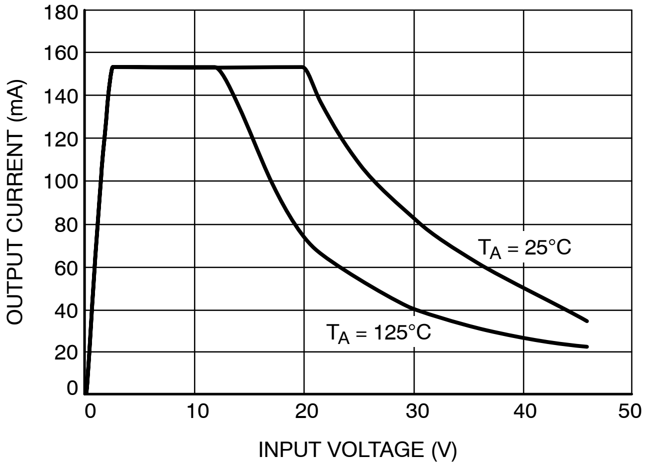


Figure 10. Output Current vs. Input Voltage

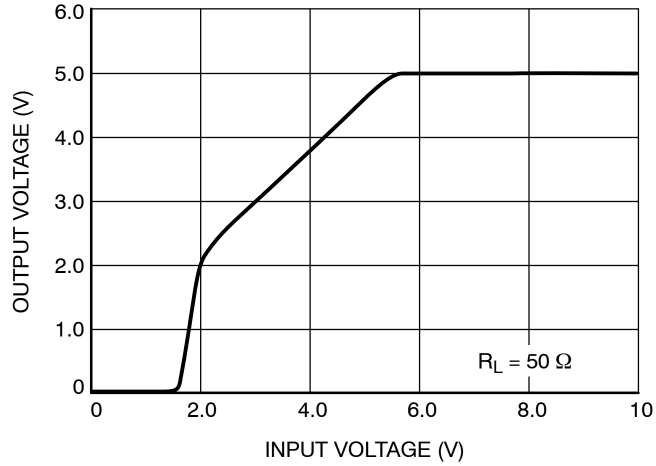


Figure 11. Input Voltage vs. Output Voltage

Circuit Description

The NCV4264 is a precision trimmed 5.0 V fixed output regulator. The device has current capability of 150 mA, with 500 mV of dropout voltage at 100 mA of current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor C_{IN1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN2}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values CQ = 10 μF and an ESR = 9 Ω within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \qquad \text{(eq. 1)}$$

Where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(Max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \qquad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JA}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

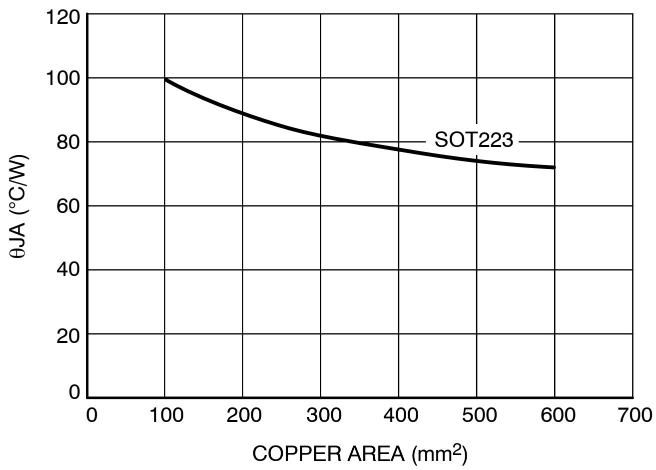


Figure 12.

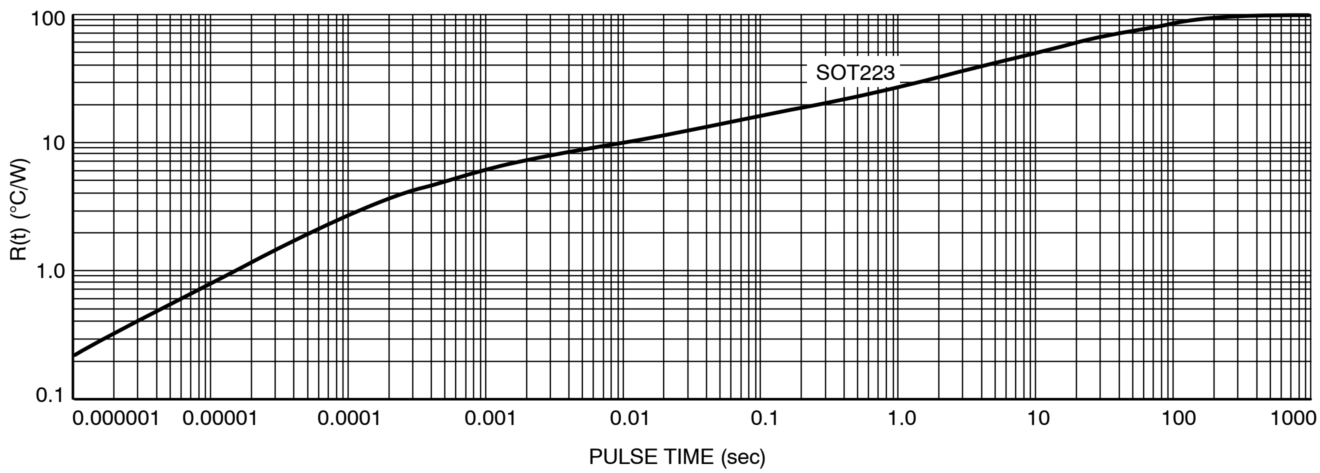


Figure 13.

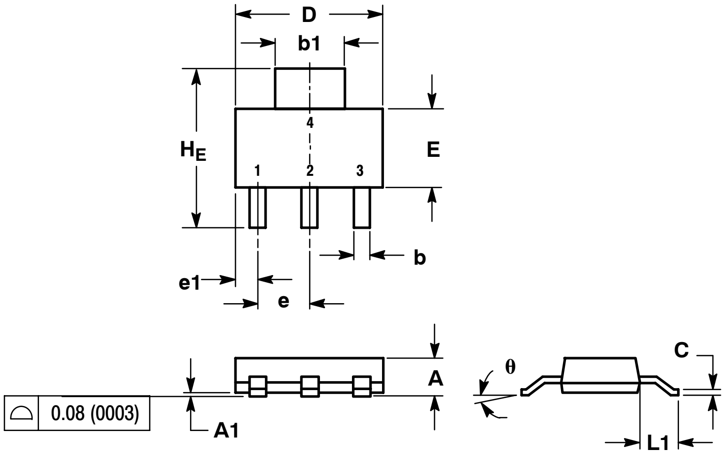
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV4264ST50T3G	V64_5	SOT−223	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

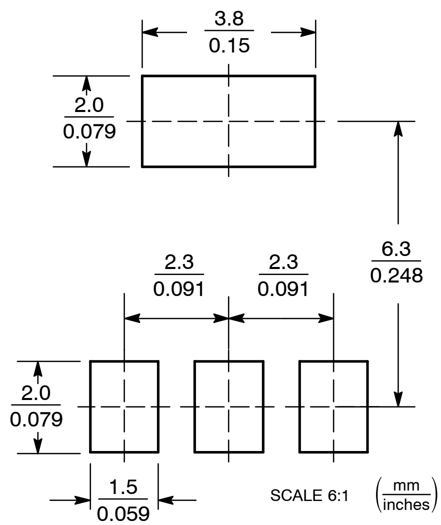
SOT−223 (TO−261)
ST SUFFIX
CASE 318E−04
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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