NCV8509 Series

Sequenced Linear Dual-Voltage Regulator

The NCV8509 Series are dual voltage regulators whose output voltages power up in such a manner as to protect the integrity of modern day microcontroller I/O and ESD input structures. Newer generation microcontrollers require two power supplies. One voltage is used for powering the core, while the other powers the I/O.

Features

- Power−Up Sequence
- Output Voltage Options:
  - V_{OUT1} 5 V (±2%) 115 mA, V_{OUT2} 2.6 V (2%) 100 mA
  - V_{OUT1} 5 V (±2%) 115 mA, V_{OUT2} 2.5 V (2%) 100 mA
  - V_{OUT1} 3.3 V (±2%) 115 mA, V_{OUT2} 1.8 V (2%) 100 mA
- Low 175 μA Quiescent Current
- Power Shunt
- Programmable $\overline{\text{RESET}}$ Time
- Dual Drive $\overline{\text{RESET}}$ Valid
- Programmable SLEW Rate Control
- Thermal Shutdown
- 16 Lead SOW Exposed Pad
- NCV Prefix, for Automotive and Other Applications Requiring Site and Change Control

Typical Applications

- Automotive Powertrain
- Telematics

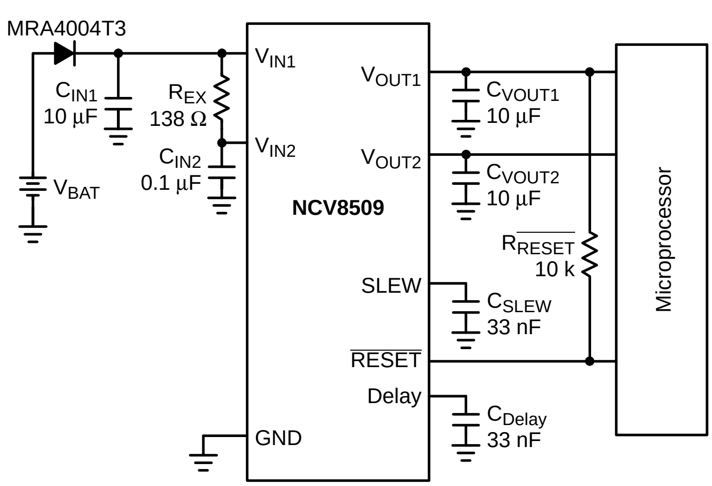

Figure 1. Application Diagram

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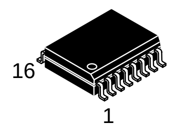
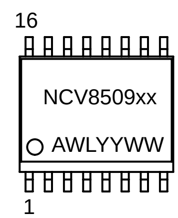


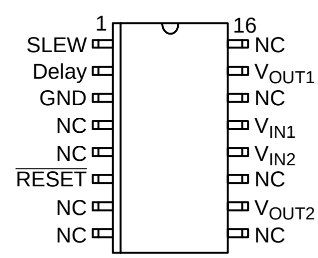
SOIC 16 LEAD WIDE BODY EXPOSED PAD PDW SUFFIX CASE 751R

MARKING DIAGRAM



xx = Voltage Ratings as Indicated Below:
26 = 5 V/2.6 V
25 = 5 V/2.5 V
18 = 3.3 V/1.8 V
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

MAXIMUM RATINGS*

Rating		Value	Unit
V_{IN1} (dc)		−0.3 to 50	V
V_{IN1} Peak Transient Voltage		50	V
V_{IN2} (dc)		50	V
V_{IN2} (Current out of pin)		10	mA
Operating Voltage		50	V
Input Voltage Range (SLEW, $\overline{RESET}$, Delay)		−0.3 to 10	V
V_{OUT1}		10	V
V_{OUT2}		10	V
ElectrosElectrostatic Discharge (Human Body Model) (Machine Model)		4.0 400	kV V
Package Thermal Resistance, SOW−16 E Pad:	Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	16 57	°C/W °C/W
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	240 peak (Note 2)	°C

*The maximum package power dissipation must be observed.
1. 60 second maximum above 183°C.
2. −5°C/+0°C allowable conditions.

ELECTRICAL CHARACTERISTICS (6.0 V < V_{IN1} < 18 V, I_{VOUT1} = 5.0 mA, I_{VOUT2} = 5.0 mA, −40°C < T_J < 125°C, C_{VOUT1} = C_{VOUT2} = 10 μF; unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{OUT1}					
Output Voltage 5 V Option 3.3 V Option	 1.0 mA < I_{VOUT1} < 100 mA 1.0 mA < I_{VOUT1} < 100 mA	 4.9 3.234	 5.0 3.3	 5.1 3.366	 V V
Dropout Voltage (V_{IN1} − V_{OUT1})	I_{OUT} = 100 mA I_{OUT} = 100 μA	− −	400 100	600 200	mV mV
Load Regulation	1.0 mA < I_{VOUT1} < 100 mA	−	10	50	mV
Line Regulation	6.0 V < V_{IN1} < 18 V	−	10	50	mV
Current Limit	V_{OUT1} = V_{OUT1} (typ) − 500 mV V_{OUT1} = 0 V	115 −	305 105	610 300	mA mA
V_{OUT2}					
Output Voltage 2.6 V Option 2.5 V Option 1.8 V Option	 1.0 mA < I_{VOUT2} < 100 mA 1.0 mA < I_{VOUT2} < 100 mA 1.0 mA < I_{VOUT2} < 100 mA	 2.548 2.450 1.764	 2.6 2.5 1.8	 2.652 2.550 1.836	 V V V
Load Regulation	1.0 mA < I_{VOUT2} < 100 mA	−	5.0	50	mV
Line Regulation	6.0 V < V_{IN1} = V_{IN2} < 18 V	−	10	50	mV
Current Limit	V_{OUT2} = V_{OUT2} (typ) − 500 mV V_{OUT2} = 0 V	105 −	305 105	610 300	mA mA
General					
Quiescent Current	I_{OUT1} = I_{OUT2} = 100 μA, V_{IN1} = 12 V I_{OUT1} = I_{OUT2} = 50 mA, V_{IN1} = 14 V	− −	75 5.0	175 10	μA mA
Thermal Shutdown (Note 3)	(Guaranteed by Design)	150	180	210	°C

3. Both outputs will turn off.

ELECTRICAL CHARACTERISTICS (continued) (6.0 V < V_{IN1} < 18 V, I_{VOUT1} = 5.0 mA, I_{VOUT2} = 5.0 mA, −40°C < T_J < 125°C, C_{VOUT1} = C_{VOUT2} = 10 μF; unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
SLEW					
SLEW Charging Current	SLEW = 1.0 V	4.0	6.0	8.0	μA
V_{OUT1} SLEW Rate (Note 4) 5 V Option 3.3 V Option	C_{SLEW} = 33 nF	 − −	 710 469	 − −	 V/s V/s
V_{OUT2} SLEW Rate 2.6 V Option 2.5 V Option 1.8 V Option	C_{SLEW} = 33 nF	 − − −	 370 355 256	 − − −	 V/s V/s V/s
SLEW Control Threshold	(See Figure 41)	1.5	1.8	2.1	V
$\overline{RESET}$					
$\overline{RESET}$ Threshold Increasing (Note 5)	−	94.5	96.5	98.5	%
$\overline{RESET}$ Threshold Decreasing 5 V Option 3.3 V Option 2.6 V Option 2.5 V Option 1.8 V Option	−	 4.5 2.97 2.34 2.25 1.62	 4.73 3.12 2.46 2.36 1.70	 0.965 × V_{OUT} 0.965 × V_{OUT} 0.965 × V_{OUT} 0.965 × V_{OUT} 0.965 × V_{OUT}	 V V V V V
$\overline{RESET}$ Output Low	$I_{\overline{RESET}}$ = 1.0 mA	−	0.1	0.4	V
$\overline{RESET}$ Output Peak	Power Down (See Figure 29)	−	0.6	1.0	V
$\overline{RESET}$ Threshold Hysteresis 5 V Option 3.3 V Option 2.6 V Option 2.5 V Option 1.8 V Option	−	 50 33 26 25 18	 100 66 52 50 36	 150 99 78 75 54	 mV mV mV mV mV
Delay					
Delay Switching Threshold	−	1.125	1.5	1.875	V
Delay Charge Current	Delay = 1.0 V	4.0	6.0	8.0	μA
Delay Saturation Voltage	V_{OUT1} Out of Regulation	−	−	0.1	V
Delay Discharge Current	Delay = 5.0 V V_{OUT1} out of Regulation	10	−	−	mA
Output Tracking					
Delta 1 [V_{OUT1} − V_{OUT2}] 5 V Option 3.3 V Option	 C_{OUT1} = C_{OUT2} , I_{OUT1} = I_{OUT2} C_{OUT1} = C_{OUT2} , I_{OUT1} = I_{OUT2}	 − −	 − −	 3.2 2.8	 V V
Delta 2 [V_{OUT2} − V_{OUT1}]	C_{OUT1} = C_{OUT2} , I_{OUT1} = I_{OUT2}	−	−	100	mV
Power Shunt					
Shunt Voltage 1 (V_{IN2})	V_{IN1} = 6.0 V, I_{OUT2} = 100 mA, No R_{EX}	3.3	−	4.6	V
Shunt Voltage 2 (V_{IN2})	V_{IN1} = 12 V, 1.0 mA < I_{OUT2} < 100 mA, No R_{EX}	3.25	4.5	5.75	V

4. Not a tested parameter.
5. $\overline{RESET}$ signal sensitive to V_{OUT1} and V_{OUT2}.

PIN DESCRIPTION

Pin No.	Symbol	Description
1	SLEW	Control for output rise time during power up. Requires capacitor to ground.
2	Delay	Timing capacitor for $\overline{RESET}$ function.
3	GND	Ground.
4, 5, 7−9, 11, 14, 16	NC	No connection.
6	$\overline{RESET}$	Active reset (accurate to V_{OUT} > 1.0 V).
10	V_{OUT2}	100 mA output (±2% output voltage) for powering microprocessor core.
12	V_{IN2}	Input voltage for V_{OUT2}.
13	V_{IN1}	Input voltage for V_{OUT1}, and internal circuitry.
15	V_{OUT1}	100 mA output (±2% output voltage) for powering microprocessor I/O.

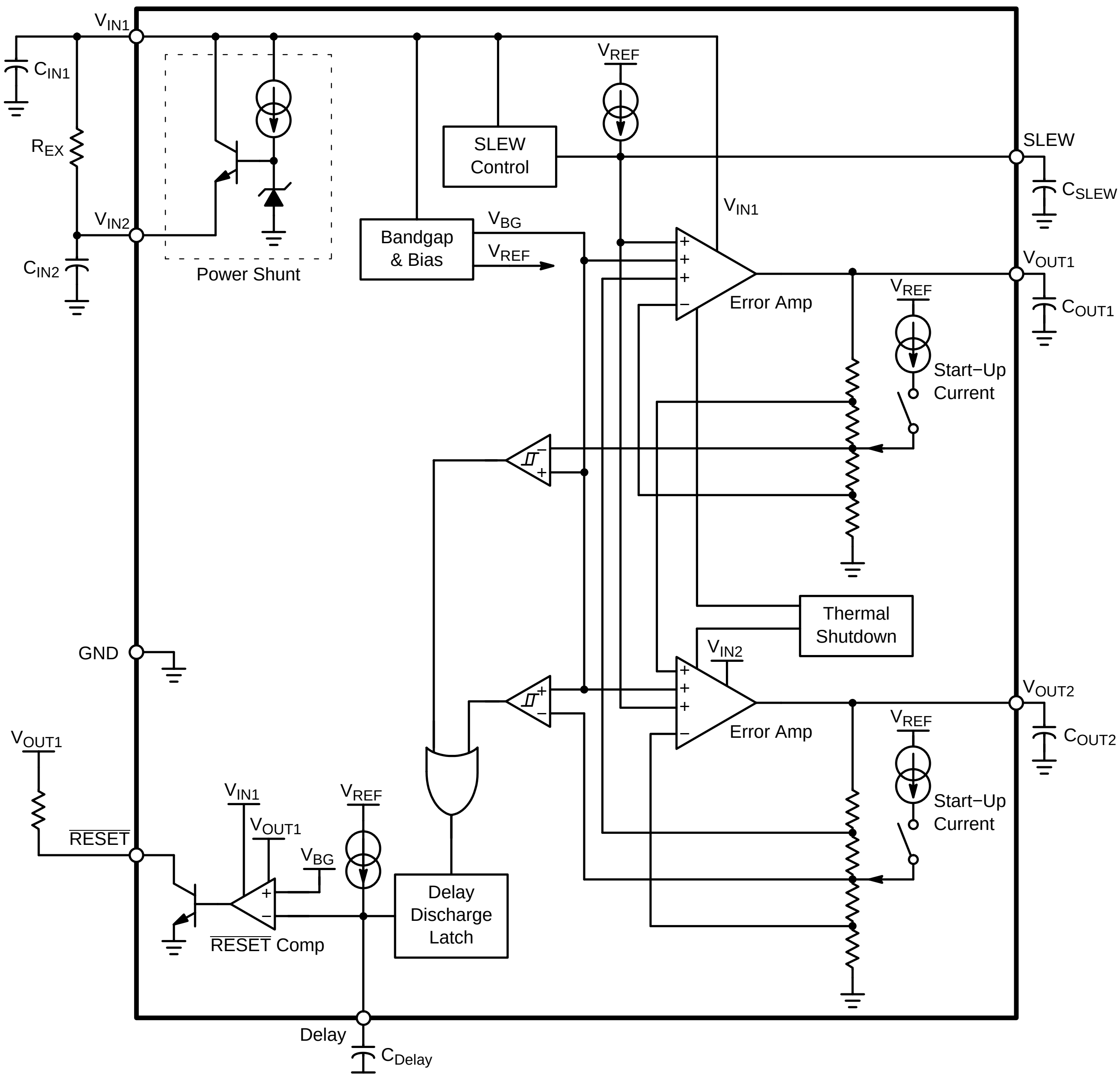


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

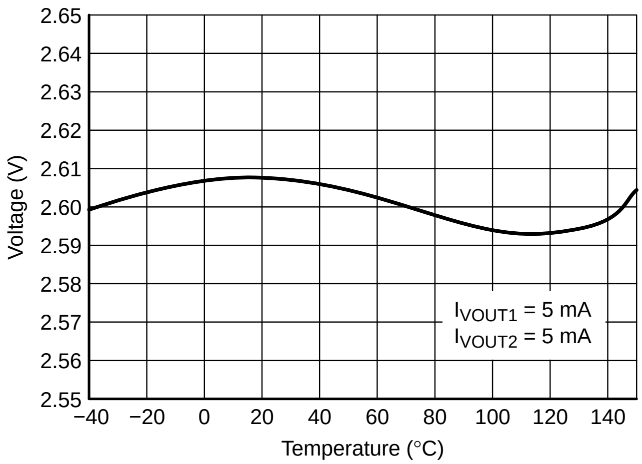


Figure 3. 2.6 V Output Voltage

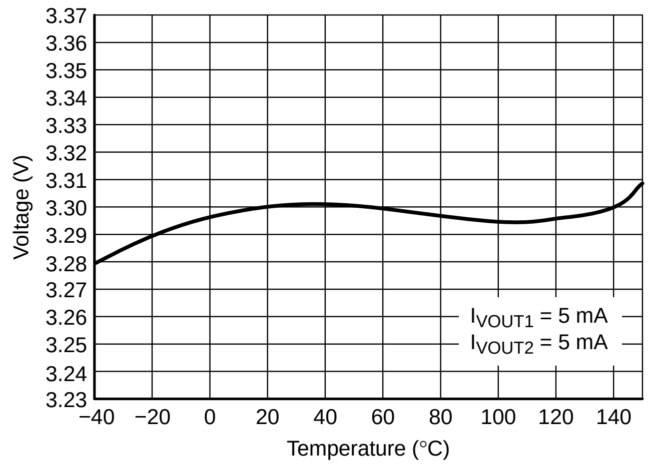


Figure 4. 3.3 V Output Voltage

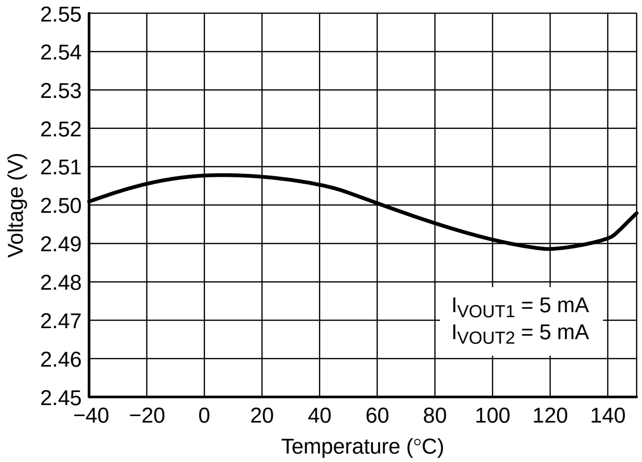


Figure 5. 2.5 V Output Voltage

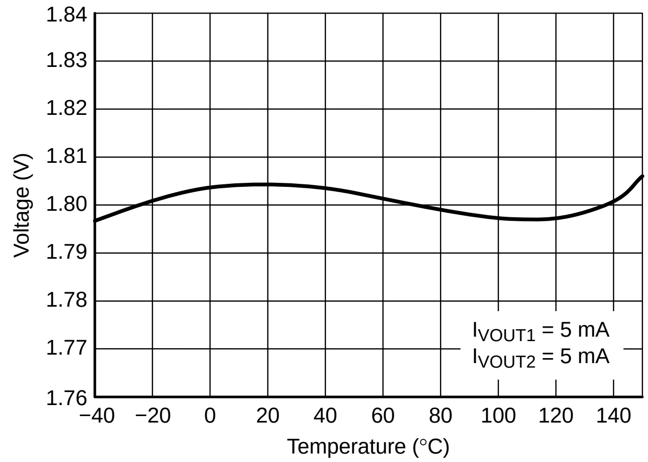


Figure 6. 1.8 V Output Voltage

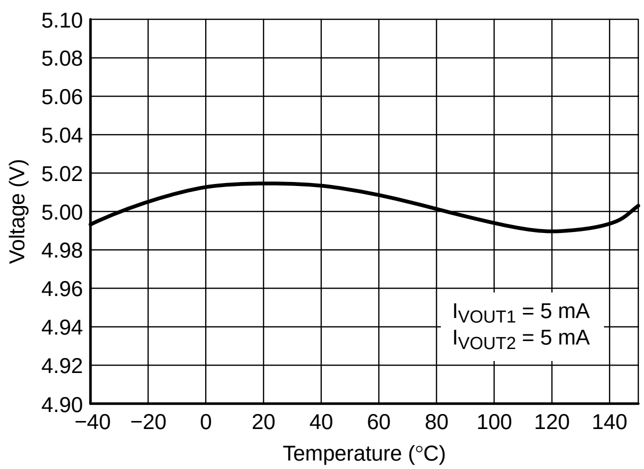


Figure 7. 5.0 V Output Voltage

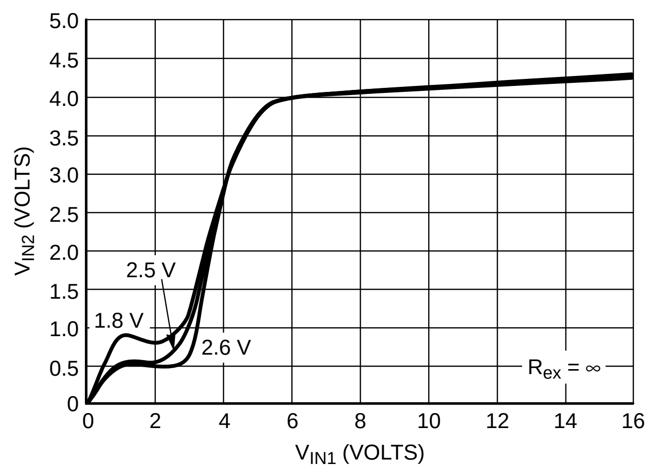


Figure 8. V_{IN2} versus V_{IN1}

TYPICAL PERFORMANCE CHARACTERISTICS

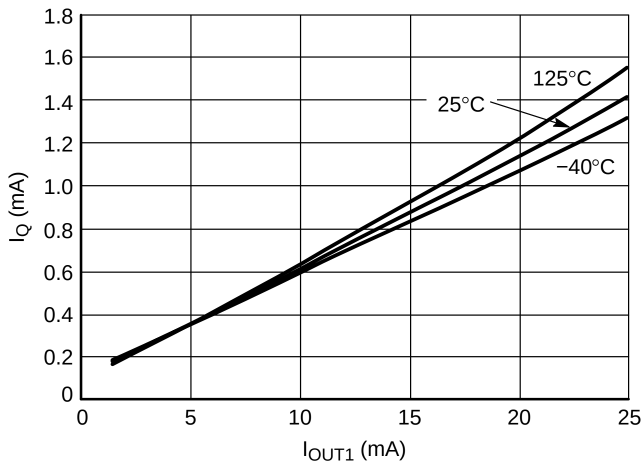


Figure 9. I_Q versus I_{OUT1}

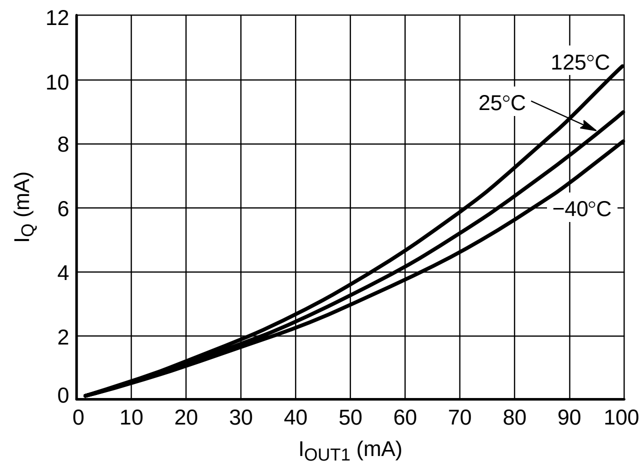


Figure 10. I_Q versus I_{OUT1}

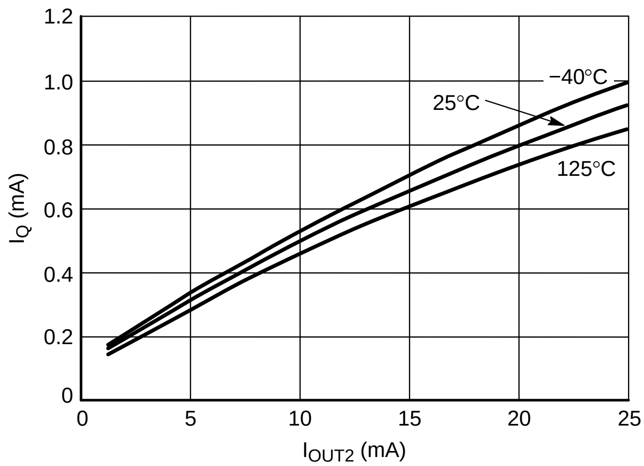


Figure 11. I_Q versus I_{OUT2}

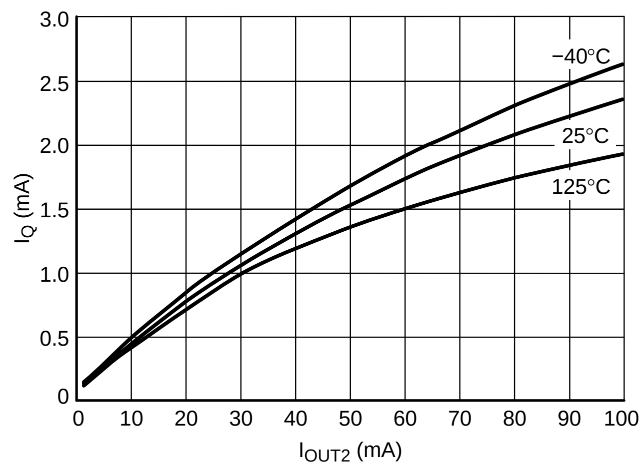


Figure 12. I_Q versus I_{OUT2}

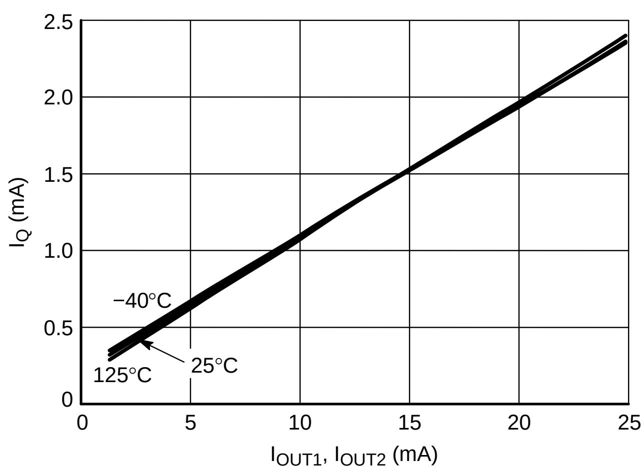


Figure 13. I_Q versus I_{OUT} (V_{OUT1} & V_{OUT2})

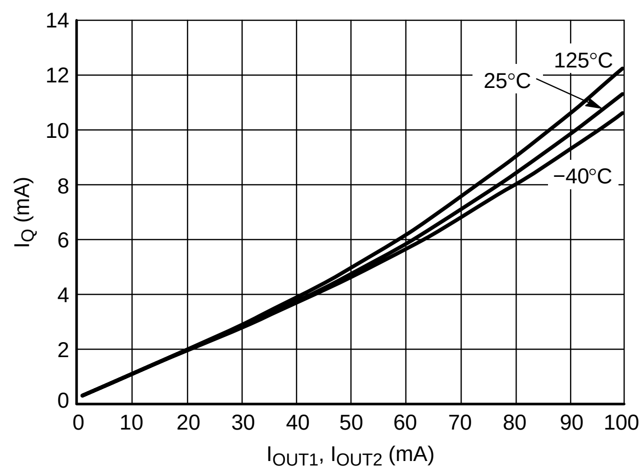


Figure 14. I_Q versus I_{OUT} (V_{OUT1} & V_{OUT2})

TYPICAL PERFORMANCE CHARACTERISTICS

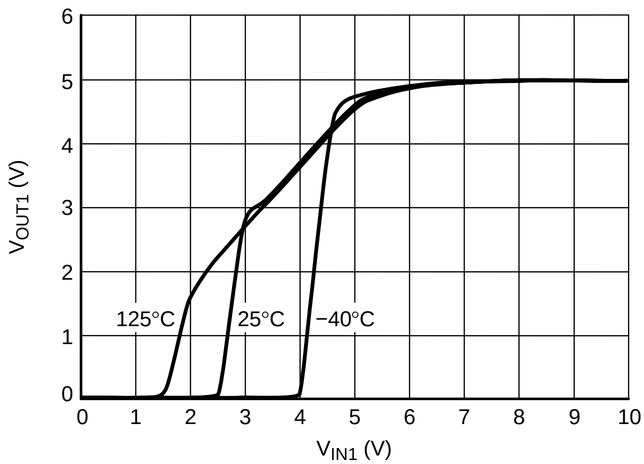


Figure 15. V_{OUT1} (5 V) versus V_{IN1}

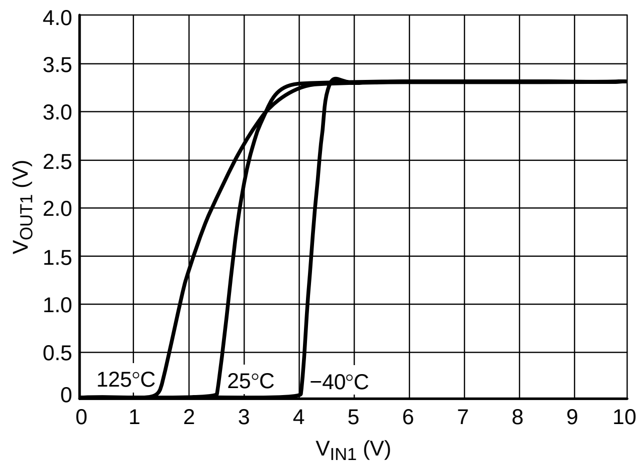


Figure 16. V_{OUT1} (3.3 V) versus V_{IN1}

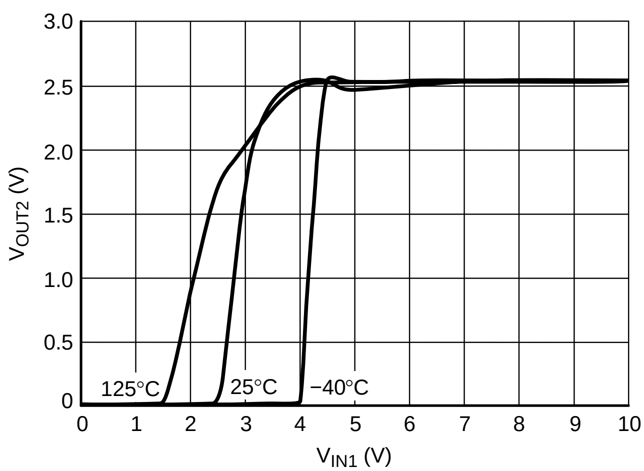


Figure 17. V_{OUT2} (2.6 V) versus V_{IN1}

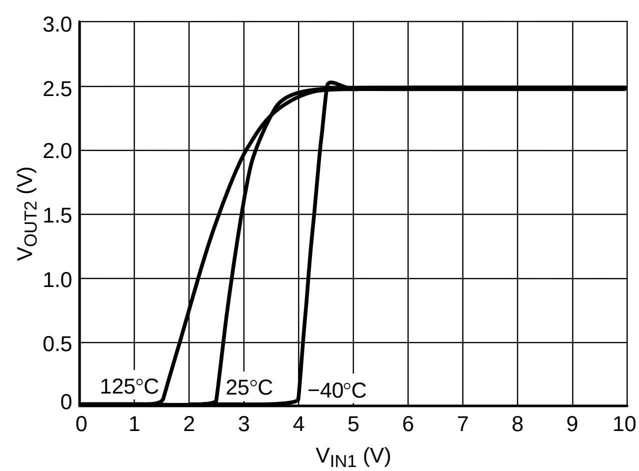


Figure 18. V_{OUT2} (2.5 V) versus V_{IN1}

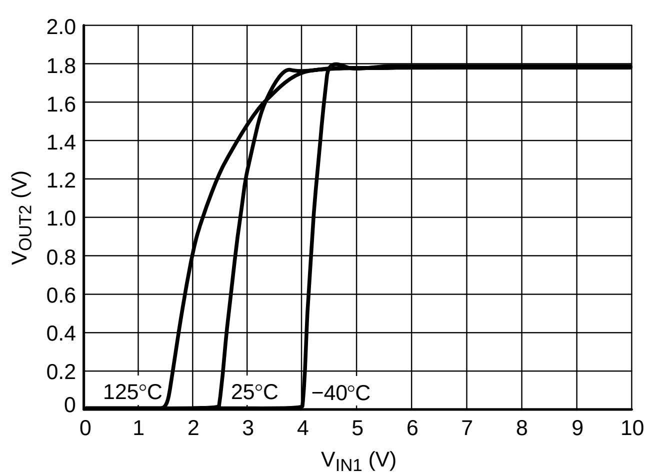


Figure 19. V_{OUT2} (1.8 V) versus V_{IN1}

TYPICAL PERFORMANCE CHARACTERISTICS

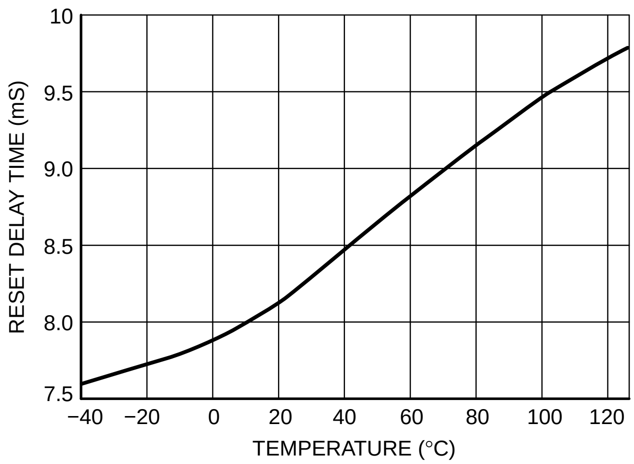


Figure 20. Reset Delay Time versus Temperature

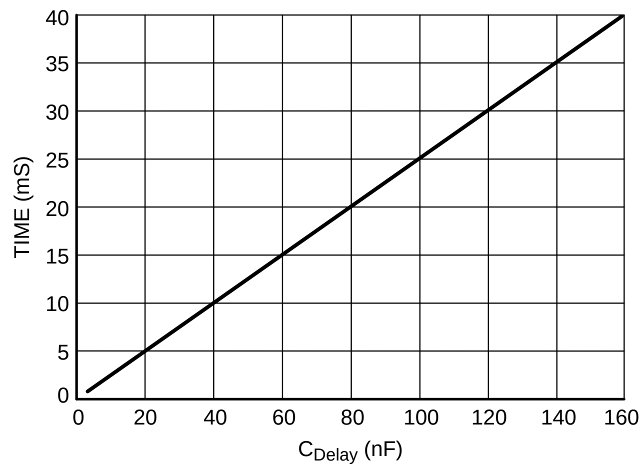


Figure 21. Reset Delay Time versus C_{Delay}

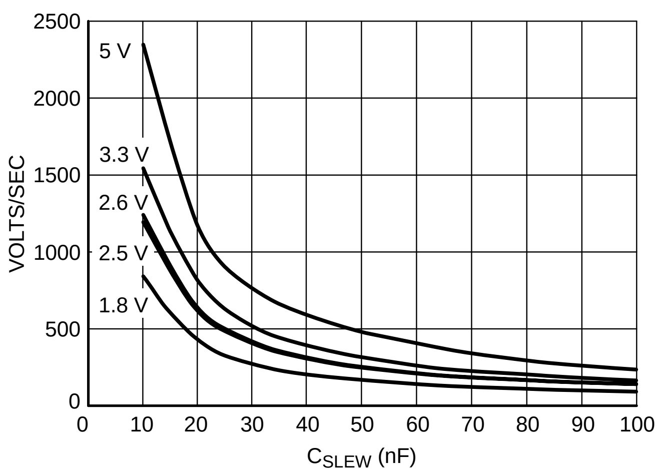


Figure 22. Slew Rate versus C_{Slew}

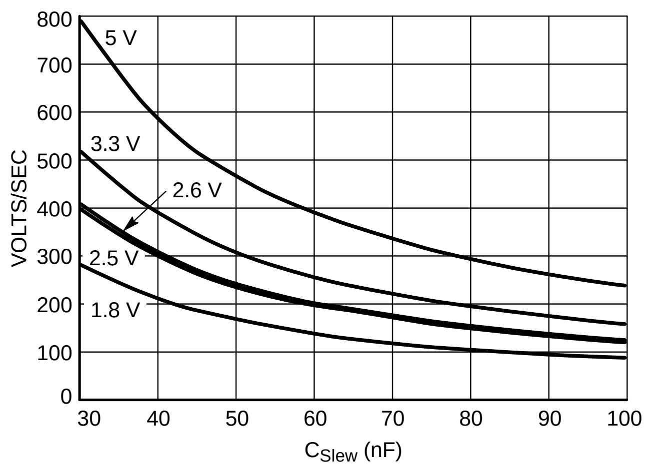


Figure 23. Slew Rate versus C_{Slew}

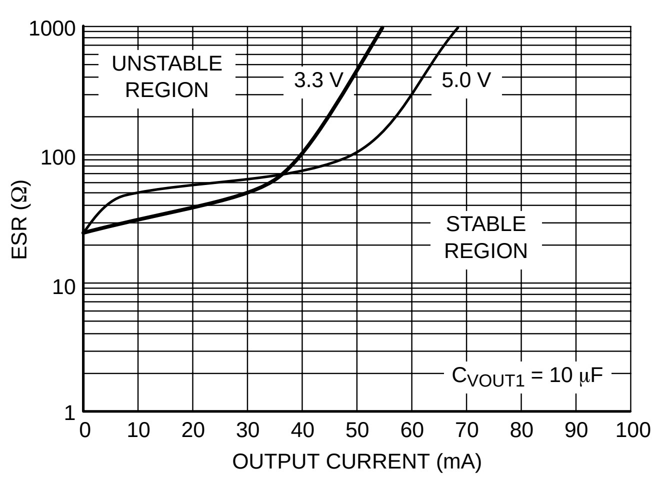


Figure 24. V_{OUT1} Output Capacitor ESR

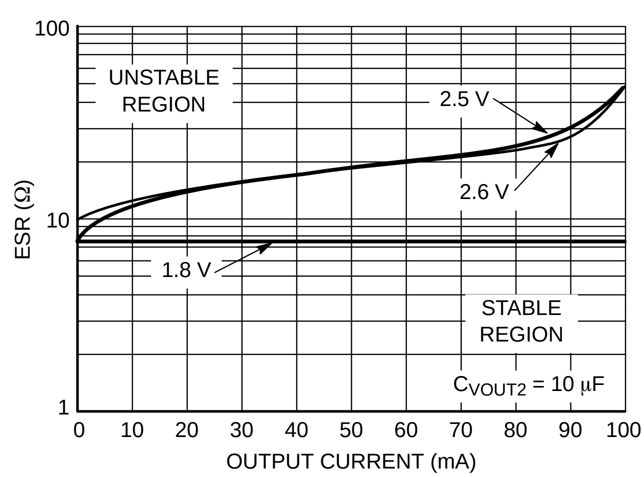


Figure 25. V_{OUT2} Output Capacitor ESR

TIMING DIAGRAMS

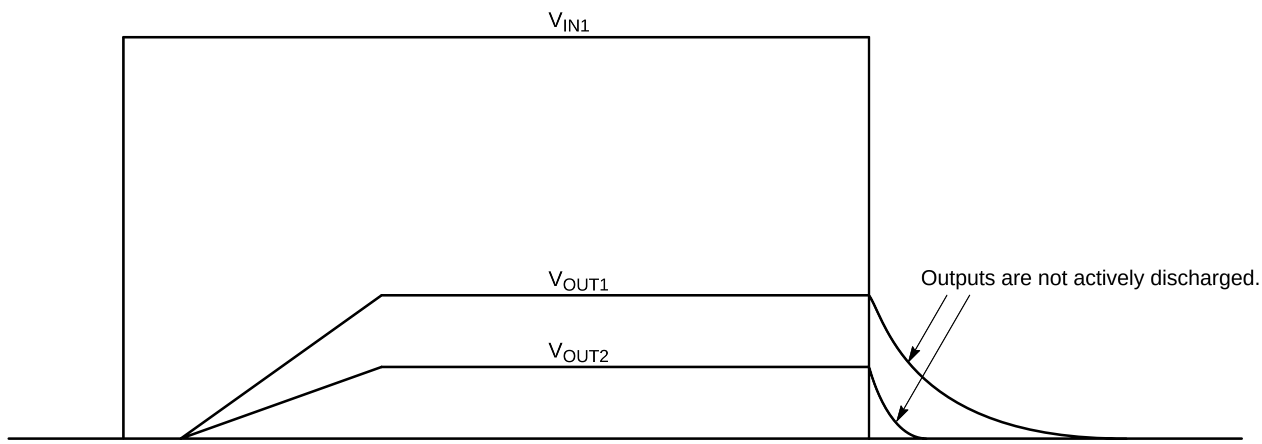


Figure 26. Response to Impulse

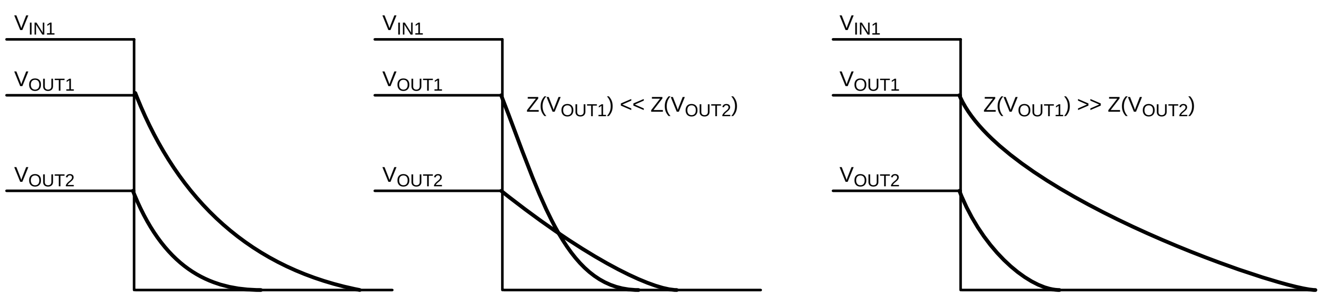


Figure 27. Output Decay vs. Load Impedance

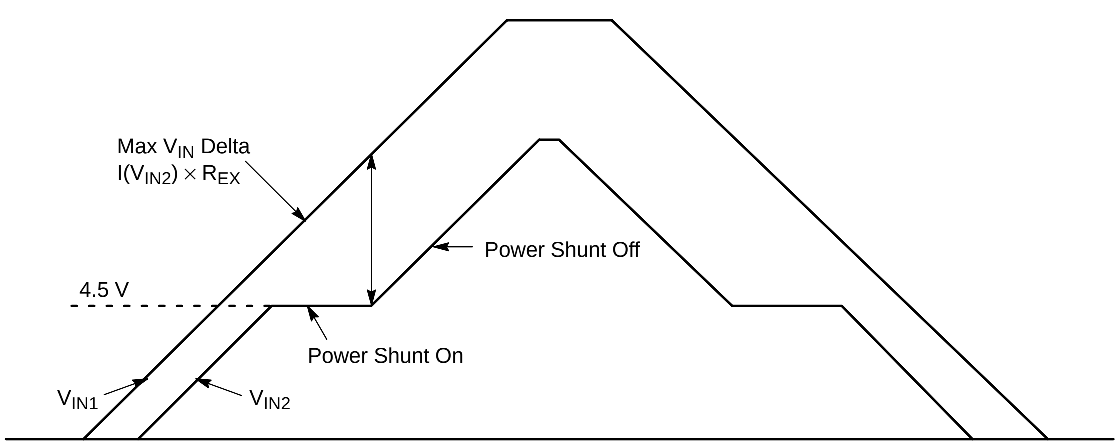


Figure 28. V_{IN} Power Shunt

CIRCUIT DESCRIPTION

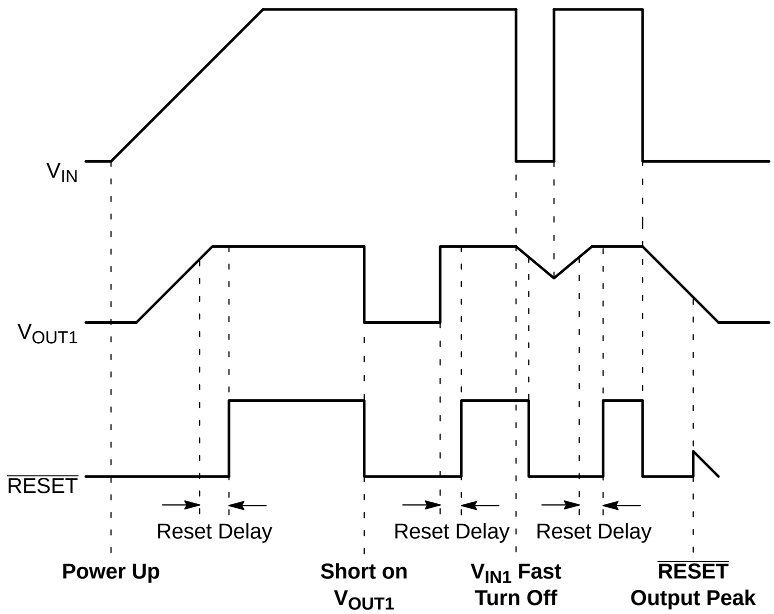


Figure 29. Dual Drive $\overline{\text{RESET}}$ Valid

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ function gets its drive from both the input (V_{IN1}) and the output (V_{OUT1}). Because of this, it is able to maintain a more reliable reset valid signal. Most regulators maintain a valid reset signal down to 1 V on the output voltage. The reset on the NCV8509 is valid down to 0 V on the output voltage V_{OUT1} (power is provided via V_{IN1}) and the reset on the NCV8509 is valid down to 0 V on the input voltage V_{IN1} (power is provided via V_{OUT1}). Refer to Figure 29 for operation timing diagrams.

Delay Function

The reset delay circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead.

The delay lead provides source current (typically 6.0 μA) to the external delay capacitor during the following proceedings:

1. During power up (once the regulation threshold has been verified);
2. After a reset event has occurred and the device is back in regulation.

The delay capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. This is a latched incident. The capacitor will fully discharge and wait for the device to regulate before going through the delay time event again.

Power Shunt

R_{EX} routes some of the current used in the V_{OUT2} to a second input pin (V_{IN2}). This is accomplished by using an internal shunt. A simplified version of this shunt is shown in Figure 30. This has the effect of reducing the amount of power dissipated on chip. The effects of choosing the external resistor value are shown in Figure 31.

Selection of the optimum Rex resistor value can be done using the following equation:

$$\frac{(V_{in(max)} - 4.5)}{I_{out2(max)}}$$

When not using the power shunt, short V_{IN1} to V_{IN2}.

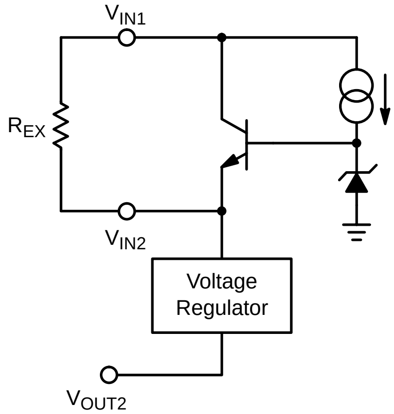


Figure 30. Power Shunt

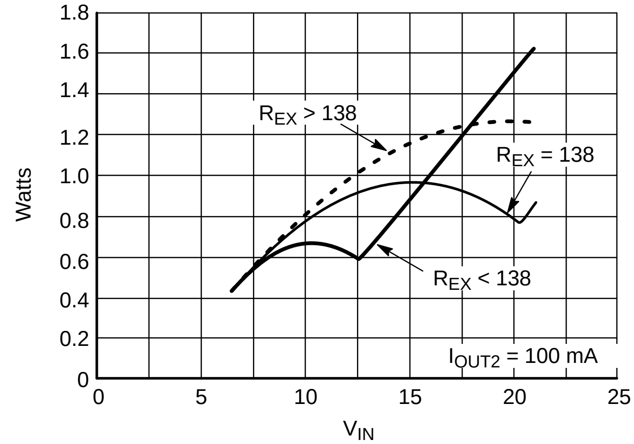


Figure 31. Power On Chip

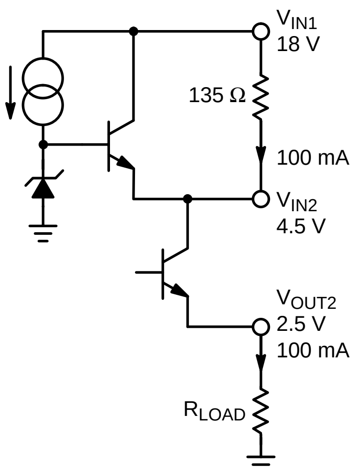


Figure 32.

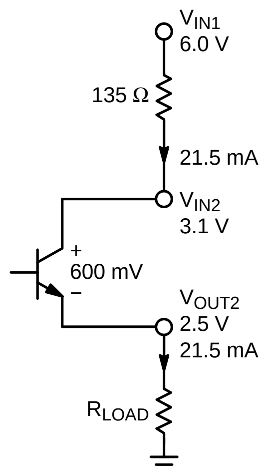


Figure 33.

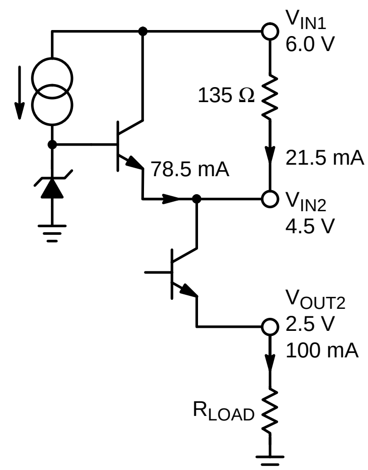


Figure 34.

Why Use a Power Shunt?

The power shunt circuitry helps manage and optimize power dissipation on the integrated circuit.

Figure 32 shows a 100 mA load. A 135 Ω resistor dissipates 1.35 W as shown.

Without the power shunt, the 135 Ω resistor would run into head room issues at 6.0 V and would only be able to drive 21.5 mA as shown in Figure 33 before causing the 2.5 V output to collapse.

Figure 34 shows the power shunt circuitry adding the current back in at low voltage operation. So the power is moved off chip at high voltage where it is needed most.

To further clarify, Figure 35 shows the maximum allowed resistor value (29 Ω) without the power shunt for 6.0 V operation.

Figure 36 shows the scenario at high voltage. Only 290 mW of power is dissipated off chip compared to Figure 32 with 1.35 W.

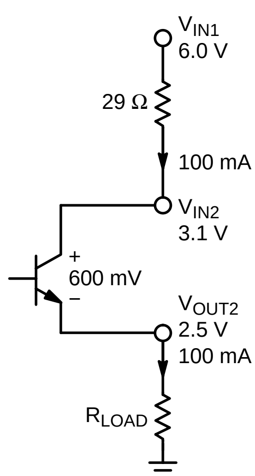


Figure 35.

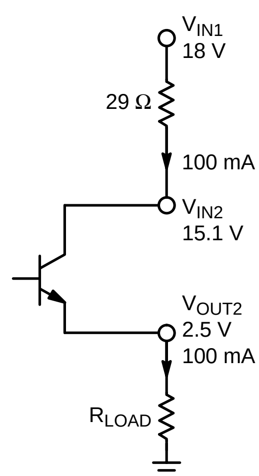


Figure 36.

Power Dissipation

NCV8509 has a power shunt circuit which reduces the power on chip by utilizing an external resistor, R_{EX}. Thus the power on chip, P_{IC}, is equal to the total power, P_T, minus the power dissipated in the resistor P_{REX}. Refer to Figure 37.

$$P_{IC} = P_{TOTAL} - P_{REX} \quad (1)$$

where

$$P_{TOTAL} = (V_{IN1} - V_{OUT1})\, I_{OUT1} + (V_{IN1} - V_{OUT2})\, I_{OUT2} + (V_{IN1} \times Iq) \quad (2)$$

and

$$P_{REX} = (V_{IN1} - V_{IN2})\, I_{OUT2} \quad (3)$$

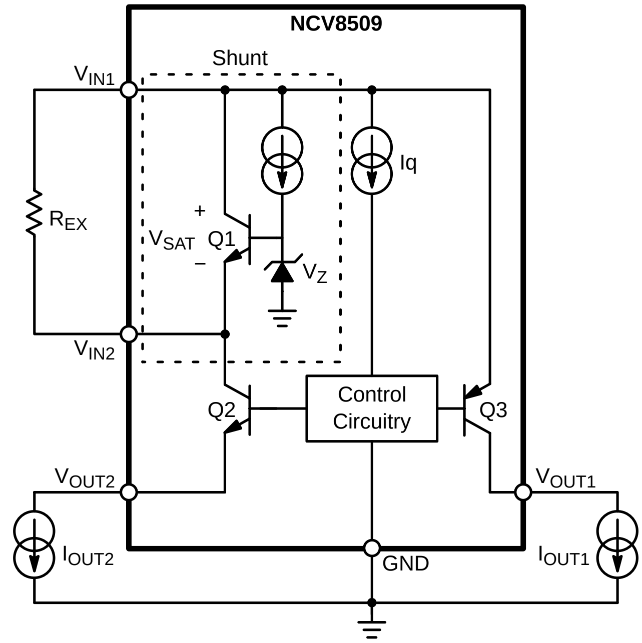


Figure 37.

$$V_{IN2} = \begin{cases} V_{IN1} - V_{SAT} & \text{for } V_{IN1} < (V_{REF} + V_{SAT}) \\ V_{REF} & \text{for } (V_{REF} + V_{SAT}) < V_{IN1} < (V_{REF} + (I_{OUT2} \times R_{EX})) \\ V_{IN1} - (I_{OUT2} \times R_{EX}) & \text{for } (V_{REF} + (I_{OUT2} \times I_{OUT})) < V_{IN1} \end{cases} \quad (4)$$

where $V_{REF} = V_Z - V_{BE}$ when Q1 is normally conducting.

Based on equation 3, the power in R_{EX} is dependent on V_{IN2}. The voltage on V_{IN2} is controlled by the shunt circuit, which has three modes of operation, as seen in Figure 38.

Mode 1. At low battery V_{IN2} is equal to V_{IN1} minus the saturation voltage of the shunt output NPN.

Mode 2. Once V_{IN1} rises above the reference voltage of the shunt circuit, V_{IN2} will regulate at the V_{REF}.

Mode 3. V_{IN2} would continue to regulate at V_{REF}, but since I_{OUT2} is not infinite, when V_{IN1} rises higher than the reference voltage plus the voltage drop across the external resistor R_{EX}, it will force V_{IN2} to be $V_{IN1} - (I_{OUT2} \times R_{EX})$.

Equation 4 provides a summary for V_{IN2}.

Combining equations 3 and 4 gives three different equations for power across R_{EX}.

$$P_{MODE1} = (V_{SAT} \times I_{OUT2}) \quad (5)$$

$$P_{MODE2} = (V_{IN1} - V_{REF}) \times I_{OUT2} \quad (6)$$

$$P_{MODE3} = I_{OUT2}{}^2 \times R_{EX} \quad (7)$$

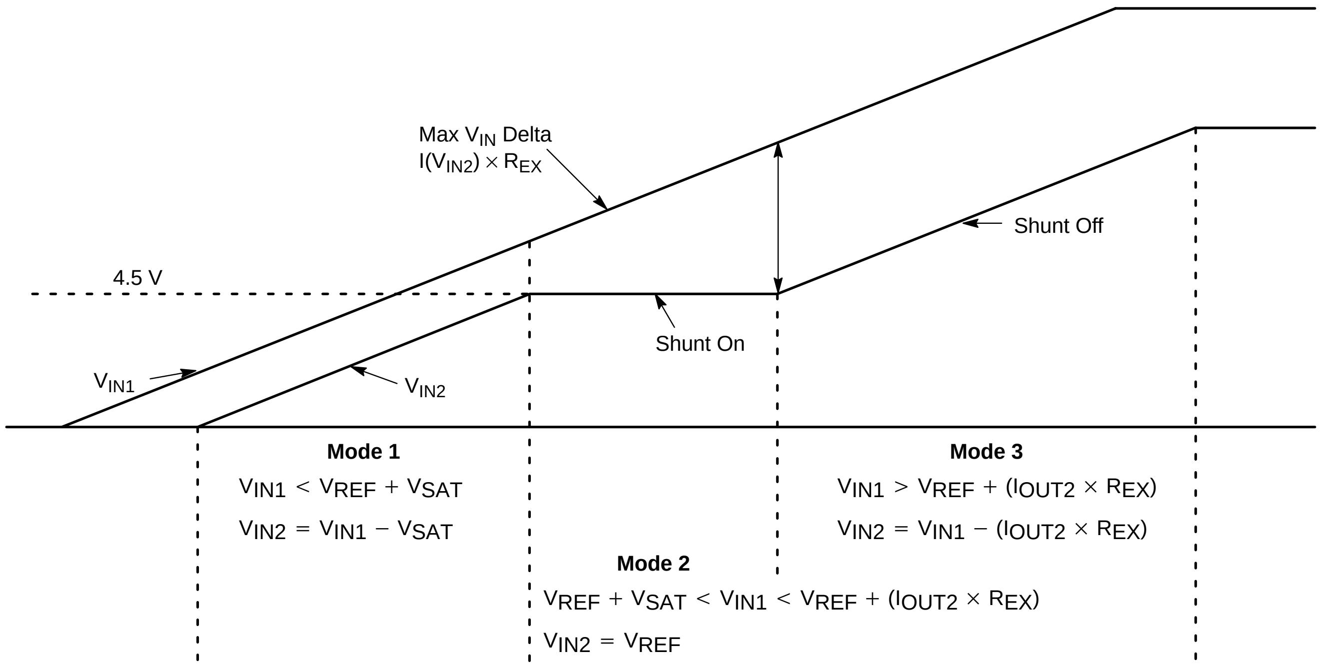


Figure 38. V_{IN} Shunt

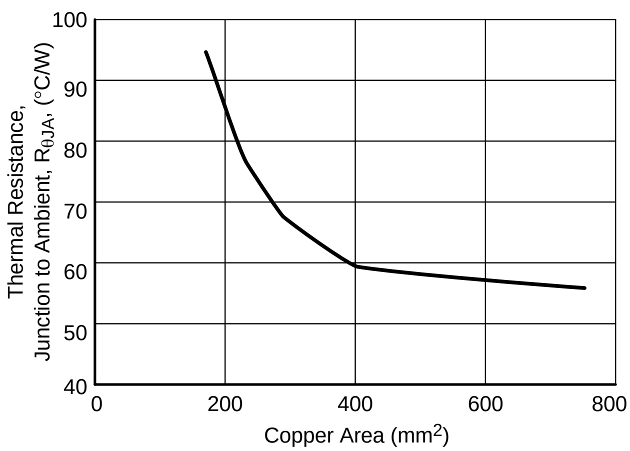


Figure 39. 16 Lead SOW (Exposed Pad), θJA as a Function of the Pad Copper Area (2 oz. Cu Thickness), Board Material = 0.0625″ G−10/R−4

Once the value of $P_{IC(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_{IC}} \quad (8)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (9)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

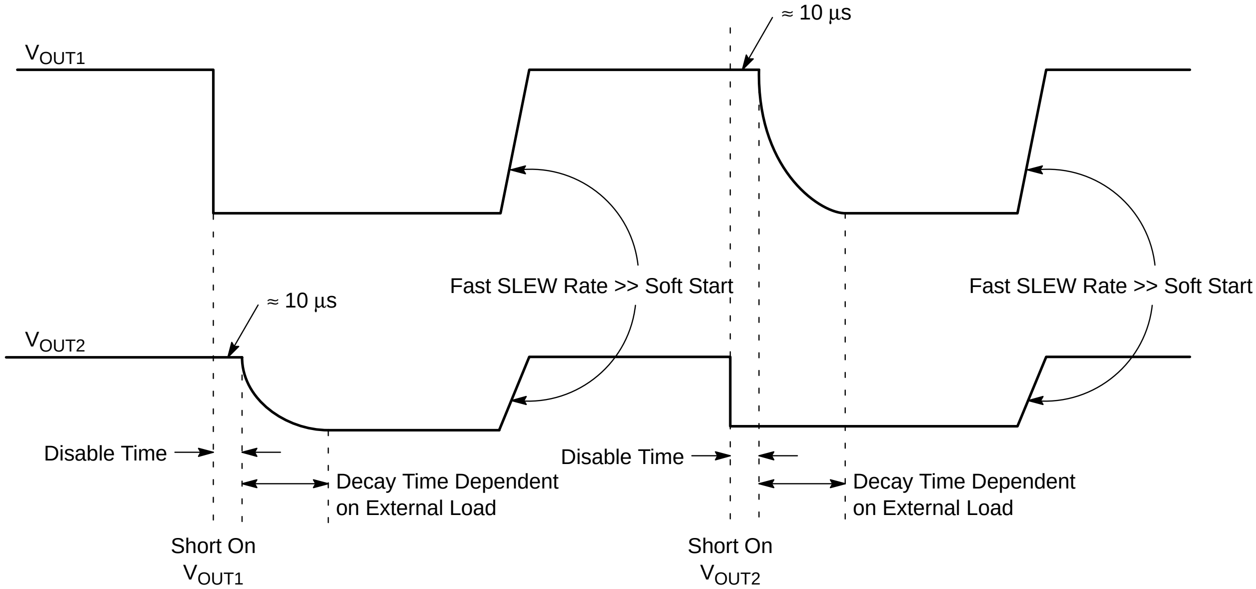


Figure 40. Fault Response. Note the High SLEW Rate Coming Out of Fault Conditions. Soft Start Only Applies to a Power Up Sequence.

Slew Rate Control

Figure 41 shows the circuitry associated with Slew Rate Control. The diagram highlights the control of one output for simplicity. V_{OUT1} and V_{OUT2} are both controlled on the IC.

The slew rate capacitor (C_{SLEW}) is charged with an on−chip current source runing at 6.0 µA (typ.). Charging a capacitor with a current source creates a linear voltage ramp as shown in Figure 42.

The lowest voltage to the positive terminals of the comparator (Error Amp) dominates the output voltage (V_{OUT}). Consequently, when C_{SLEW} is fully discharged on power up, it is the dominant factor on the positive terminal and disables the output. The output (V_{OUT}) follows the linear ramp on the SLEW pin (after being gained up with R1 and R2) until V_{BG} becomes the dominant voltage. This occurs when SLEW = V_{BG} + V_{D1} or approximately 1.8 V.

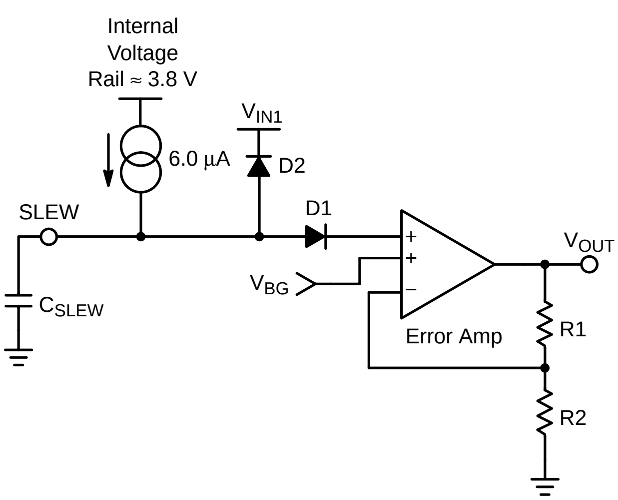


Figure 41. Slew Control Circuitry

Slew time can be calculated using the standard capacitor equation.

$$I = C\frac{dv}{dt}, \quad t = \frac{C(\Delta V)}{I}$$

Using a 33 nF capacitor, the slew time is:

$$t = \frac{(33\ nF)(1.8\ V)}{6\ \mu A} = 9.9\ ms$$

The corresponding slew rate for this is 1.8 V/9.9 ms = 182 V/s ON THE SLEW PIN.

To calculate the slew rate on outputs, you must multiply by the gain set up by R1 and R2.

$$A_V = \frac{V_{OUT}}{1.28\ V}$$

For a 5 V output, the gain would be:

$$A_V = \frac{5\ V}{1.28\ V} = 3.9\ V/V$$

assuming V_{BG} = 1.28 V.

The resultant slew rate on the output is the slew rate on the SLEW pin multiplied by the gain, or:

$$(182\ V/s) \times (3.9\ V/V) = 710\ V/s$$

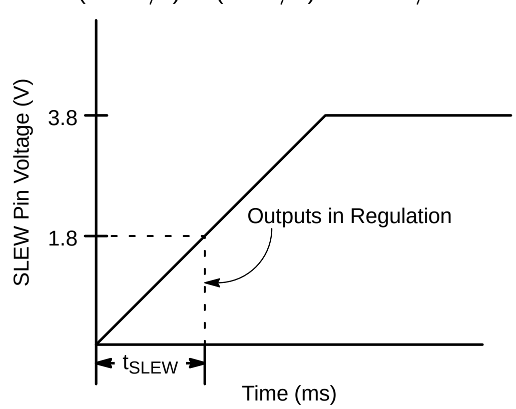


Figure 42.

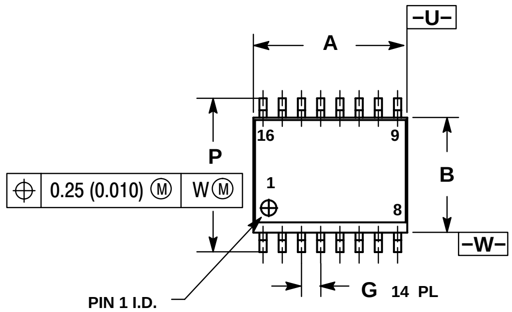
ORDERING INFORMATION

Device	Output Voltage	Package	Shipping
NCV8509PDW26	5 V/2.6 V	SOIC 16 Lead Wide Body Exposed Pad	47 Units/Rail
NCV8509PDW26R2			1000 Tape & Reel
NCV8509PDW25	5 V/2.5 V		47 Units/Rail
NCV8509PDW25R2			1000 Tape & Reel
NCV8509PDW18	3.3 V/1.8 V		47 Units/Rail
NCV8509PDW18R2			1000 Tape & Reel

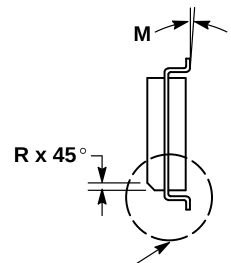
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

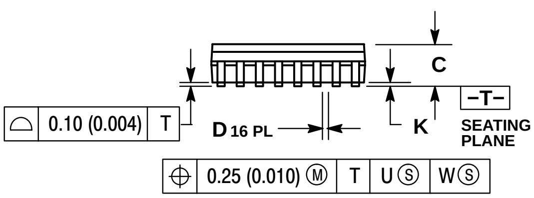
SOIC 16 LEAD WIDE BODY
EXPOSED PAD
PDW SUFFIX
CASE 751R−02
ISSUE A

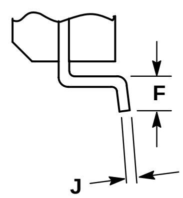


TOP SIDE

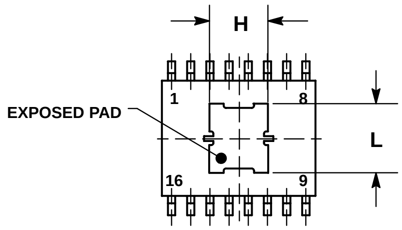


DETAIL E





DETAIL E



BACK SIDE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R−01 OBSOLETE, NEW STANDARD 751R−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.76	3.86	0.148	0.152
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
L	4.58	4.78	0.180	0.188
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PUBLICATION ORDERING INFORMATION

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