



AO4418

N-Channel Enhancement Mode Field Effect Transistor

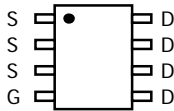


General Description

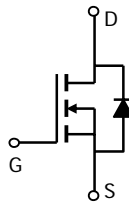
The AO4418 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard Product AO4418 is Pb-free (meets ROHS & Sony 259 specifications). AO4418L is a Green Product ordering option. AO4418 and AO4418L are electrically identical.*

Features

- V_{DS} (V) = 30V
- I_D = 11.5A (V_{GS} = 20V)
- $R_{DS(ON)} < 14m\Omega$ (V_{GS} = 20V)
- $R_{DS(ON)} < 17m\Omega$ (V_{GS} = 10V)
- $R_{DS(ON)} < 40m\Omega$ (V_{GS} = 4.5V)



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ\text{C}$	11.5
		$T_A=70^\circ\text{C}$	9.7
Pulsed Drain Current ^B	I_{DM}	40	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3
		$T_A=70^\circ\text{C}$	2.1
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	31	40
		Steady-State	59	75
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±25V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.5	2.4	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =20V, I _D =11.5A T _J =125°C		9.8 14.2	14 18	mΩ
		V _{GS} =10V, I _D =10A		12.3	17	mΩ
		V _{GS} =4.5V, I _D =5A		32	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A	14	22		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				4.3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			758		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		180		pF
C _{rss}	Reverse Transfer Capacitance			128		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.7		Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge			16.6		nC
Q _g (4.5V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =11.5A		8.6		nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			4.9		nC
t _{D(on)}	Turn-On Delay Time			5.4		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =15V, R _L =1.3Ω, R _{GEN} =3Ω		5.1		ns
t _{D(off)}	Turn-Off Delay Time			14.4		ns
t _f	Turn-Off Fall Time			3.7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =11.5A, dI/dt=100A/μs		16.9		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =11.5A, dI/dt=100A/μs		6.6		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

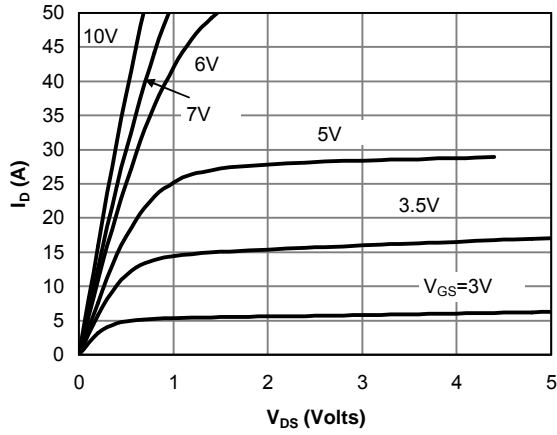


Fig 1: On-Region Characteristics

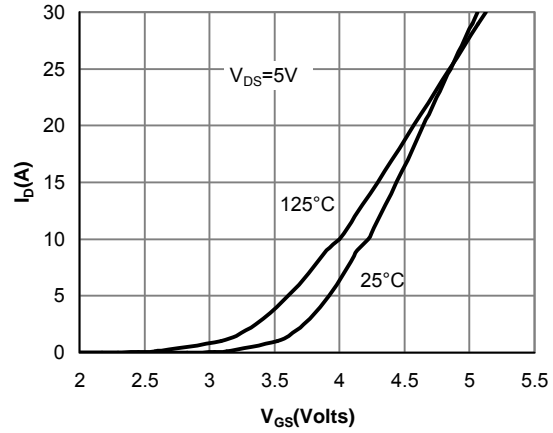


Figure 2: Transfer Characteristics

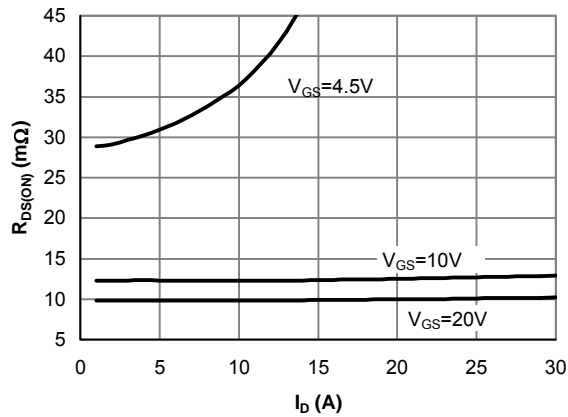


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

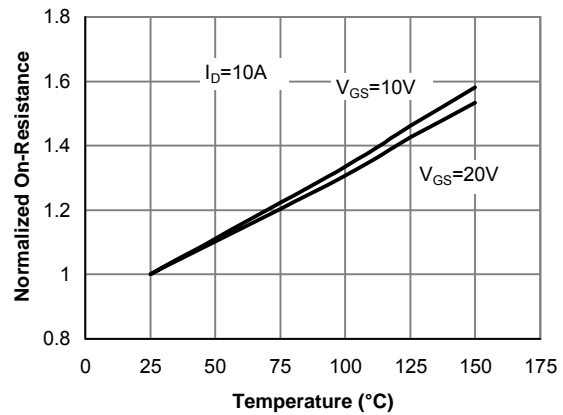


Figure 4: On-Resistance vs. Junction Temperature

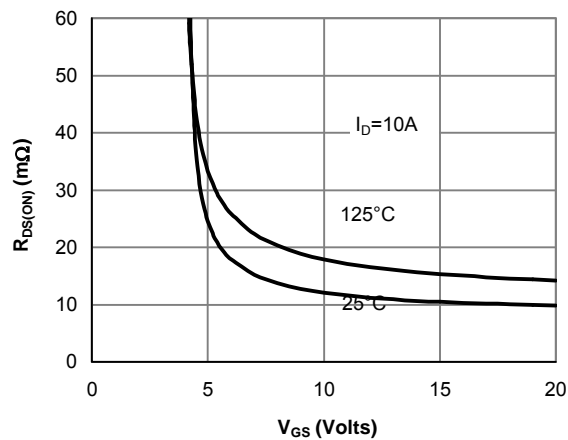


Figure 5: On-Resistance vs. Gate-Source Voltage

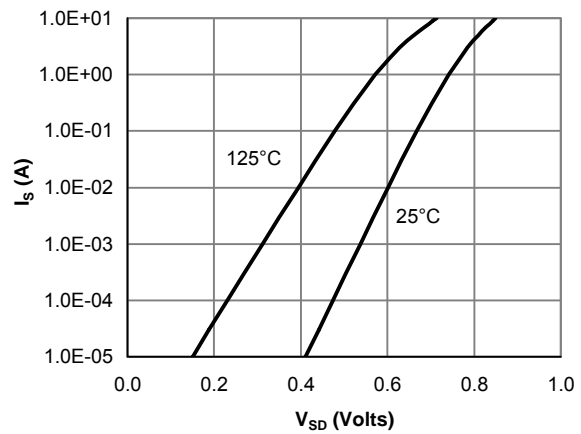


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

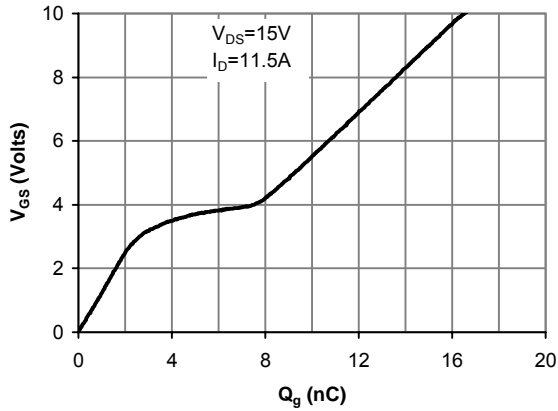


Figure 7: Gate-Charge Characteristics

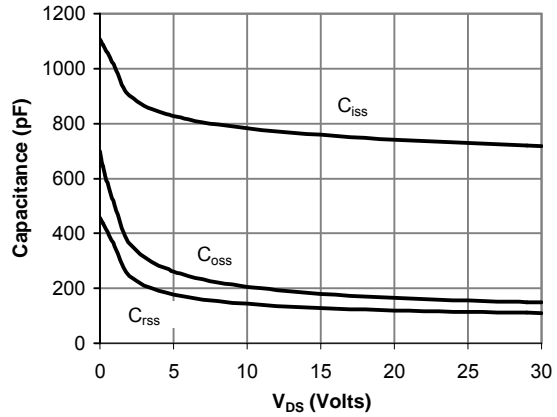


Figure 8: Capacitance Characteristics

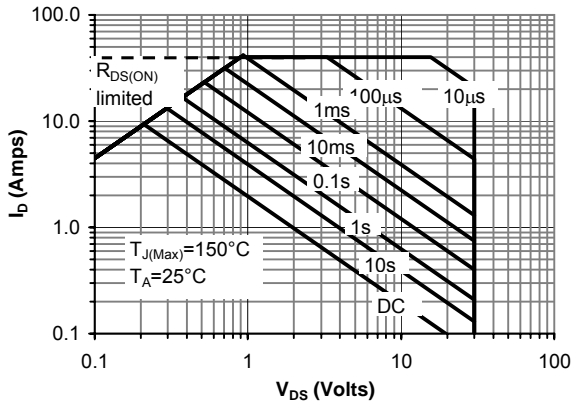


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

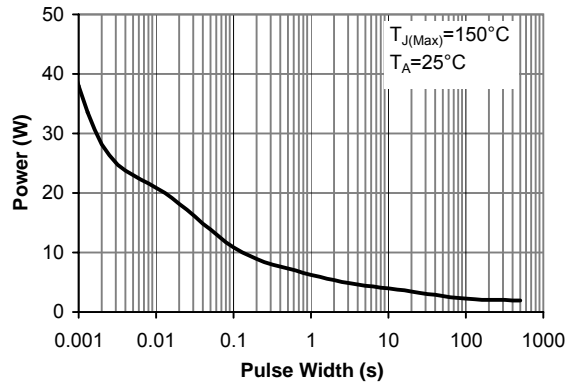


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

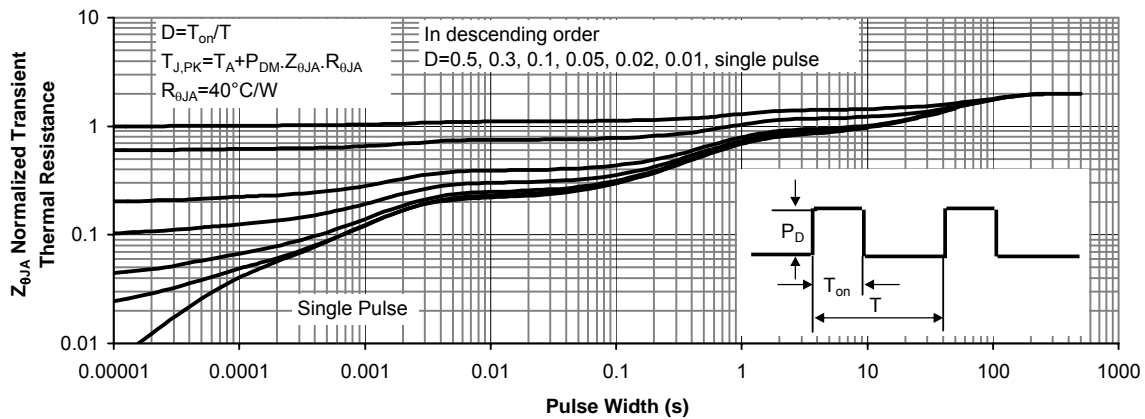


Figure 11: Normalized Maximum Transient Thermal Impedance