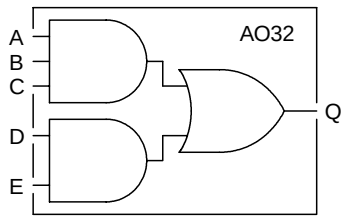
AO32 is an AND/OR circuit providing the logical function Q = (A.B.C+D.E).

Truth Table

A	B	C	D	E	Q
L	X	X	L	X	L
L	X	X	X	L	L
X	L	X	X	L	L
X	L	X	L	X	L
X	X	L	L	X	L
X	X	L	X	L	L
X	X	X	H	H	H
H	H	H	X	X	H



Capacitance

	Ci (pF)
A	0.051
B	0.052
C	0.057
D	0.052
E	0.055

Area

0.95 mils^2

Power

3.46 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.67	2.07	2.76	0.67	2.00	2.70
	tpdaf	0.74	1.86	2.43	0.97	2.09	2.59
Delay B to Q	tpdbr	0.67	2.06	2.72	0.75	2.10	2.78
	tpdbf	0.70	1.80	2.37	0.91	2.02	2.57
Delay C to Q	tpdcr	0.63	2.03	2.69	0.78	2.16	2.82
	tpdcf	0.65	1.73	2.30	0.82	1.93	2.45
Delay D to Q	tpddr	0.58	1.97	2.61	0.64	2.00	2.68
	tpddf	0.66	1.79	2.33	0.97	2.06	2.60
Delay E to Q	tpder	0.56	1.90	2.65	0.72	2.07	2.74
	tpdef	0.62	1.72	2.29	0.90	2.01	2.55
Output Slope A to Q	op_slar	0.98	5.31	7.51	0.95	5.26	7.51
	op_slaf	0.75	3.61	5.08	0.72	3.78	5.02
Output Slope B to Q	op_slbr	0.96	5.26	7.57	0.95	5.27	7.48
	op_slbf	0.72	3.56	5.30	0.72	3.60	5.31
Output Slope C to Q	op_slcr	1.00	5.28	7.55	0.93	5.28	7.51
	op_slcf	0.68	3.56	5.01	0.71	3.61	5.08

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Output Slope D to Q	op_sldr	0.95	5.33	7.58	0.96	5.23	7.47
	op_sldf	0.73	3.71	5.23	0.73	3.73	5.08
Output Slope E to Q	op_sler	0.97	5.27	7.56	0.96	5.25	7.45
	op_slef	0.72	3.53	5.16	0.71	3.62	5.31