

## AOU401

### P-Channel Enhancement Mode Field Effect Transistor

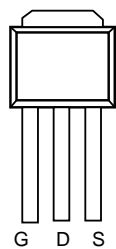
#### General Description

The AOU401 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. *Standard Product AOU401 is Pb-free (meets ROHS & Sony 259 specifications). AOU401L is a Green Product ordering option. AOU401 and AOU401L are electrically identical.*

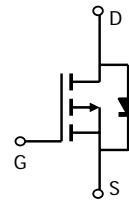
#### Features

$V_{DS} (V) = -60V$   
 $I_D = -26 A (V_{GS} = -10V)$   
 $R_{DS(ON)} < 40 m\Omega (V_{GS} = -10V) @ 20A$   
 $R_{DS(ON)} < 55 m\Omega (V_{GS} = -4.5V)$

TO-251



Top View  
 Drain Connected  
 to Tab



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ C$	A
		$T_C=100^\circ C$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-60	
Avalanche Current <sup>C</sup>	$I_{AR}$	-26	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	134	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	W
		$T_C=100^\circ C$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	100	125	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	1.9	2.5	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250uA, V <sub>GS</sub> =0V	-60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		-0.003	-1	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.9	-2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A		32	40	mΩ
		T <sub>J</sub> =125°C		53		
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A		43	55	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		32		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.73	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-30	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-30V, f=1MHz		2977	3600	pF
C <sub>oss</sub>	Output Capacitance			241		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			153		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		2	2.4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, I <sub>D</sub> =-20A		44	54	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			22.2	28	nC
Q <sub>gs</sub>	Gate Source Charge			9		nC
Q <sub>gd</sub>	Gate Drain Charge			10		nC
t <sub>D(on)</sub>	Turn-On DelayTime			12		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, R <sub>L</sub> =1.5Ω,		14.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime	R <sub>GEN</sub> =3Ω		38		ns
t <sub>f</sub>	Turn-Off Fall Time			15		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-20A, di/dt=100A/μs		40	50	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, di/dt=100A/μs		59		nC

- A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.
  - B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
  - C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.
  - D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
  - E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
  - F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.
  - G: The maximum current rating is limited by bond-wires.
- Rev3: August 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

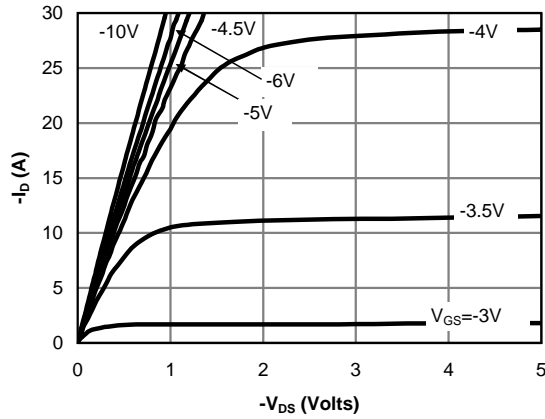


Fig 1: On-Region Characteristics

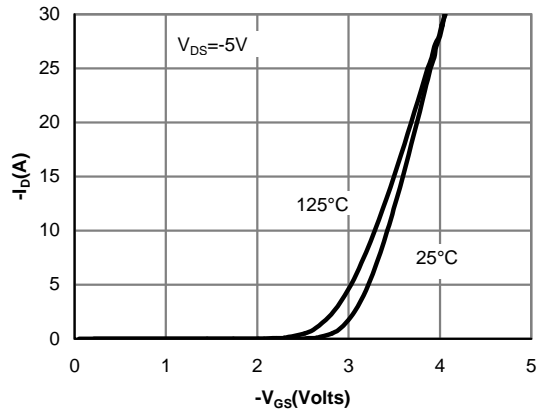


Figure 2: Transfer Characteristics

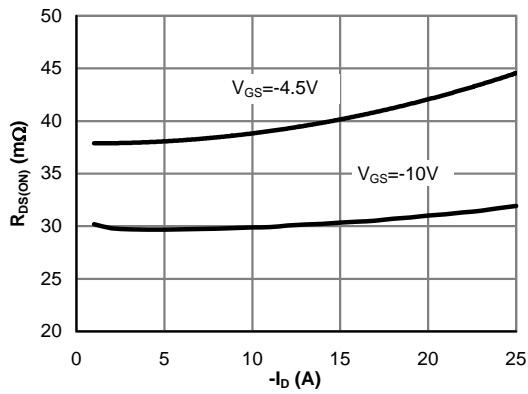


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

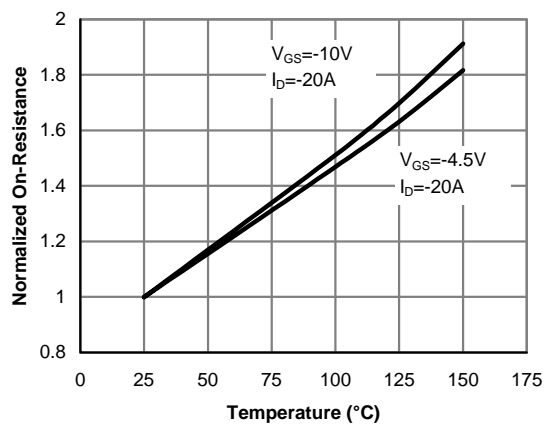


Figure 4: On-Resistance vs. Junction Temperature

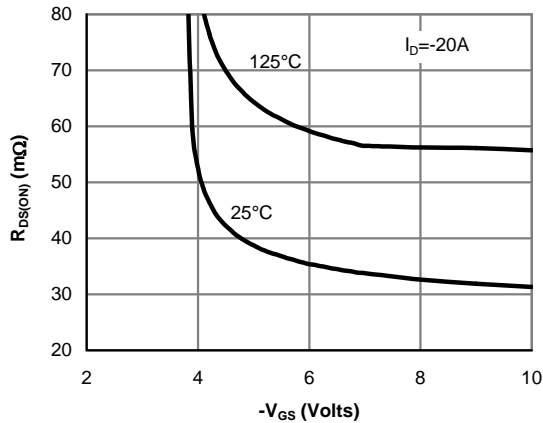


Figure 5: On-Resistance vs. Gate-Source Voltage

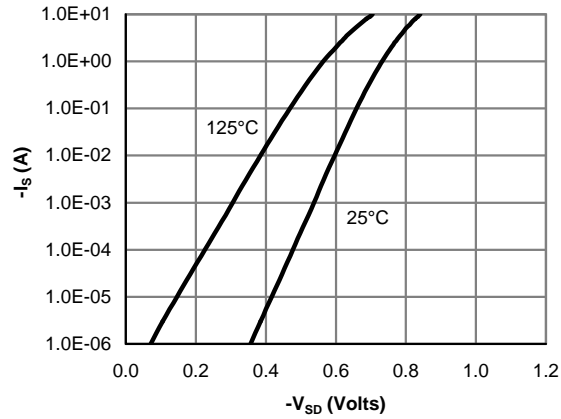


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

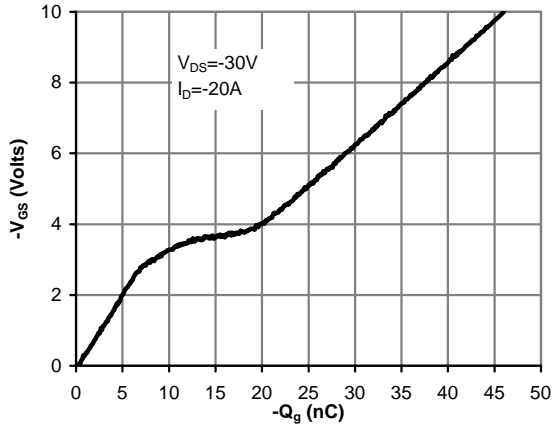


Figure 7: Gate-Charge Characteristics

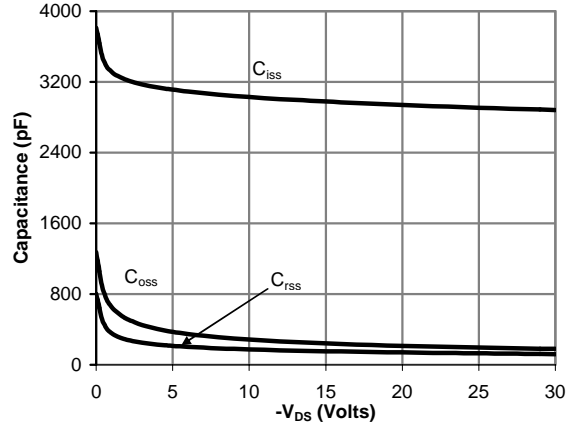


Figure 8: Capacitance Characteristics

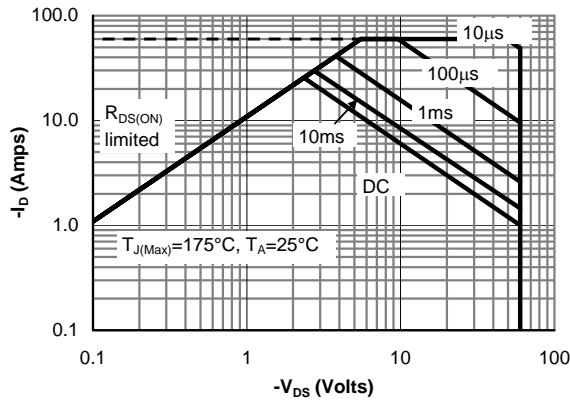


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

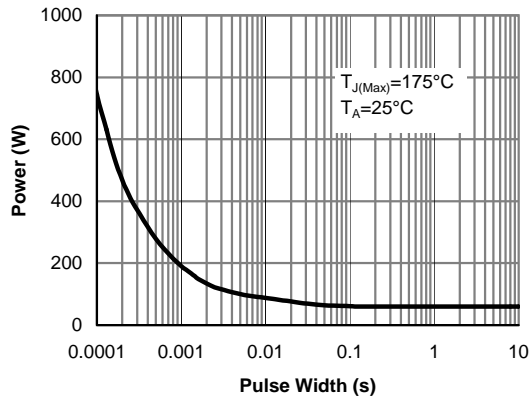


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

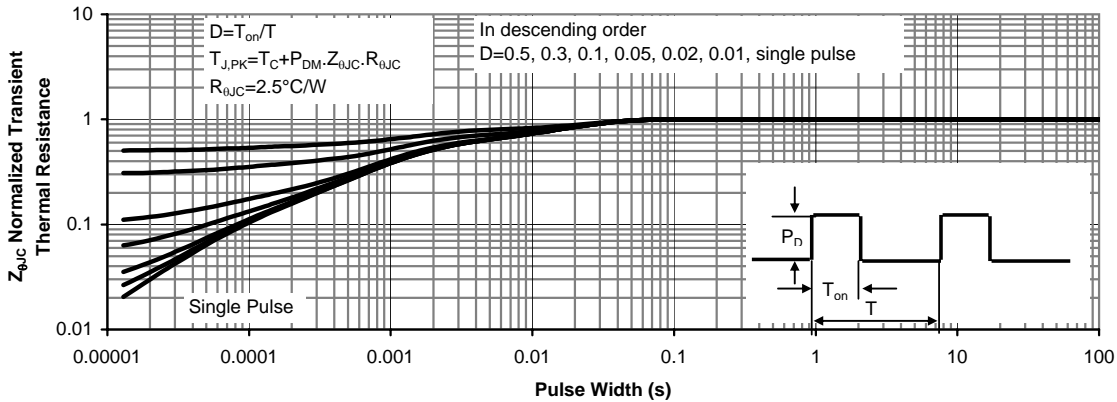


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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