STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCTSERIES 2-ch Switching Regulator Controller

TYPE **BA9741F, BA9741FS**

FEATURES

1. Built-in timer-latch type short prevention circuit
2. Built-in high-accuracy reference voltage output pin 2.5V±4%
3. Rest period adjustable over the whole range of duty ratio

○ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Limits	Unit
Power supply voltage		Vcc	36	V
Power dissipation	BA9741F	Pd	500*1	mW
	BA9741FS		650*2	mW
Output pin current		Io	120*3	mA
Output pin voltage		Vo	36	V
Operating temperature		Topr	-40～+85	℃
Storage temperature		Tstg	-55～+125	℃
Junction temperature		Tjmax	125	℃

*1: Reduced by 5.0 mW/°C over Ta = 25°C or more. (When mounted on 70 mm × 70 mm × 1.6 mm, glass epoxy)
*2: Reduced by 6.5 mW/°C over Ta = 25°C or more. (When mounted on 70 mm × 70 mm × 1.6 mm, glass epoxy)
*3: Should not exceed Pd-or ASO-value.

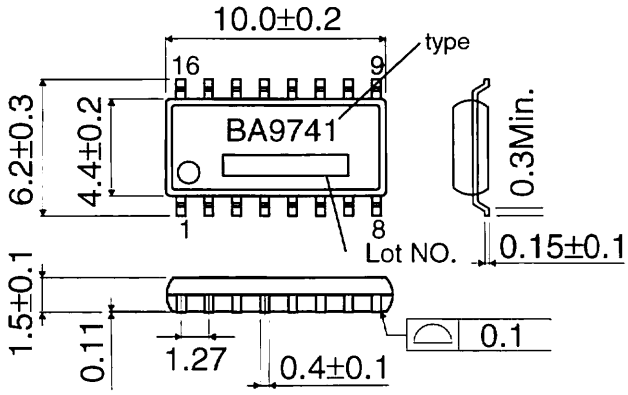
○ Recommendable operation range (Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	3.6	6.0	35	V
Output pin current	Io	-	-	100	mA
Output pin voltage	Vo	-	-	35	V
Error amplifier input voltage	VOM	0.3	-	1.6	V
Timing capacitance	CCT	100	-	15000	pF
Timing resistance	RRT	5.1	-	50	kΩ
Oscillation frequency	Fosc	10	-	800	kHz

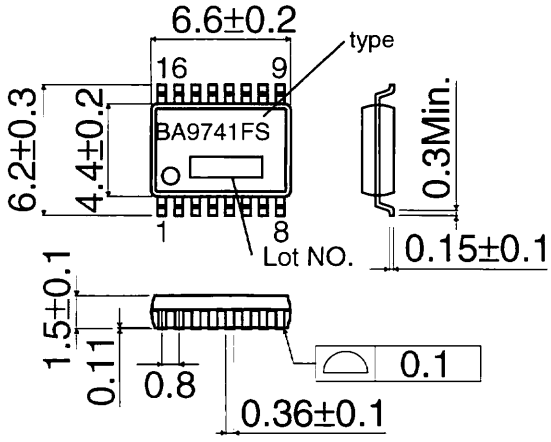
○ Electrical Characteristics (Ta=25℃, VCC=6.0V)

Item	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【Reference voltage section]】						
Output voltage	V_{REF}	2.4	2.5	2.6	V	I_{REF}=1mA
Input stability	V_{DLI}	−	1	10	mV	Vcc=3.6～35V
Load stability	V_{DLO}	−	1	10	mV	I_{REF}=0～5mA
【Triangular wave oscillator section】						
Oscillation frequency	F_{OSC}	320	400	480	KHz	R_{RT}=10kΩ,CCT=220pF
Frequency variation	F_{DV}	−	1	−	%	Vcc=3.6～35V
【Protection circuit section】						
Threshold voltage	V_{IT}	1.48	1.64	1.80	V	
Standby voltage	V_{STB}	−	50	100	mV	No pull-up
Latch voltage	V_{LT}	−	30	100	mV	No pull-up
Source current	I_{SCP}	1.5	2.5	3.5	μA	
Comparator threshold voltage	V_{CT}	0.9	1.05	1.2	V	5pin, 12pin
【Rest period adjustment circuit section】						
Input threshold voltage (fosc=10kHz)	V_{t0}	1.79	1.97	2.15	V	Duty cycle =0%
	V_{t100}	1.32	1.48	1.64	V	Duty cycle =100%
ON duty cycle	D_{ON}	45	55	65	%	VREF is divided by13kΩ and27kΩ resistors.
Input bias current	I_{BDT}	−	0.1	1	μA	DTC=2.0V
Latch mode source current	I_{DT}	200	560	−	μA	DTC=0V
Latch input voltage	V_{DT}	2.28	2.48	−	V	I_{DT}=40μA
【Low-input-voltage malfunction prevention circuit section】						
Threshold voltage	V_{UT}	−	2.53	−	V	
【Error amplifier section】						
Input offset voltage	V_{IO}	−	−	6	mV	
Input offset current	I_{IO}	−	−	30	nA	
Input bias current	I_{IB}	−	15	100	nA	
Open loop gain	AV	70	85	−	dB	
Common-mode input voltage	V_{CM}	0.3	−	1.6	V	Vcc=3.6～35V
Common-mode rejection ratio	CMRR	60	80	−	dB	
Maximum output voltage	V_{OM}	2.3	2.5	−	V	
Minimum output current	V_{OL}	−	0.7	0.9	V	
Output sink current	I_{OI}	3	20	−	mA	FB=1.25V
Output source current	I_{OO}	45	75	−	μA	FB=1.25V
【PWM comparator section】						
Input threshold voltage (fosc=10kHz)	V_{t0}	1.79	1.97	2.15	V	Duty cycle =0%
	V_{t100}	1.32	1.48	1.64	V	Duty cycle=100%
【Output section】						
Saturation voltage	V_{SAT}	−	0.8	1.2	V	Io=75mA
Leak current	I_{LEAK}	−	−	5	μA	Vo=35V
【Total device】						
Standby current	I_{CCS}	−	1.3	1.8	mA	When output is OFF
Average current dissipation	I_{CCA}	−	1.6	2.3	mA	R_{RT}=10kΩ

○ Outline figure

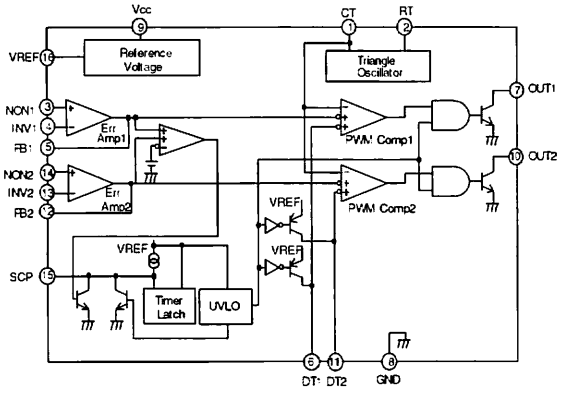


SOP－16 (Unit : mm)



SSOP－A16(Unit : mm)

○ Block Diagram



○ PIN No./ name / function

Pin No.	Pin name	Function
1	CT	External timing capacitance
2	RT	External timing resistance
3	NON1	Positive input for error amplifier 1
4	INV1	Negative input for error amplifier 1
5	FB1	Output for error amplifier 1
6	DT1	Output 1 dead time/soft start setting
7	OUT1	Output 1
8	GND	GROUND
9	Vcc	Power Supply
10	OUT2	Output 2
11	DT2	Output 2 dead time/soft start setting
12	FB2	Output for error amplifier 2
13	INV2	Negative input for error amplifier 2
14	NON2	Positive input for error amplifier 2
15	SCP	Timer latch setting
16	VREF	Reference voltage output

○ Cautions on use

1. Absolute maximum ratings
An excess in the absolute maximum ratings, such as applied voltage, operating temperature range, etc., can degrade or break down devices, thus making impossible to identify breaking mode such as short circuit mode or an open mode. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including use of fuses, etc.

2. GND potential
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins other than the GND pin fall below the GND voltage, including an actual electric transient.

3. Thermal design
With consideration given to power dissipation(Pd) in the actual use state, provide the thermal design with an adequate margin.

4. Short circuit between pins and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the GND pin, the ICs can break down.

5. Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

6. Inspection with set printed circuit board
On the inspection with the set printed circuit board, if a capacitor is connected to a low-impedance pin, the IC can suffer stress. Therefore, be sure to discharge from the set printed circuit board by each process. For protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set printed circuit board. Furthermore, in older to connect the jig for the inspection process, be sure to turn OFF the power supply and then mount the set printed circuit board to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount the set printed circuit board from the jig.

7. Common impedance
For power supply and GND wirings, thorough consideration should be given, for example, to reduce common impedance, minimize ripple currents(in other words, to provide as thick and short wirings as possible or reduce ripple currents according to L and C values), etc.

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