BUK71/794R1-40BT

TrenchMOS™ standard level FET

Rev. 01 — 4 November 2004 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology. The devices include TrenchPLUS diodes for over-temperature protection.

Product availability:

BUK714R1-40BT in SOT426 (D^2-PAK)

BUK794R1-40BT in SOT263B (TO-220AB).

1.2 Features

- Integrated temperature sensor
- Very low on-state resistance
- Q101 compliant
- 175 °C rated.

1.3 Applications

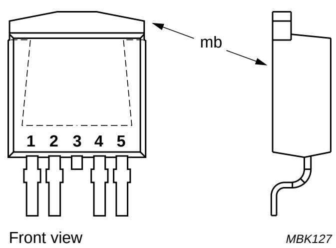
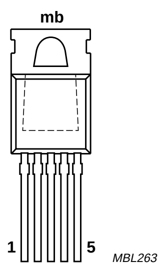
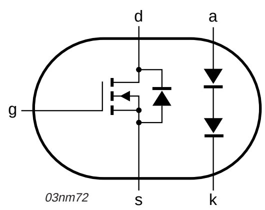
- Electrical Power Assisted Steering
- Motors, lamps and solenoids
- 12 V loads
- General purpose power switching.

1.4 Quick reference data

- R_{DSon} = 3.4 mΩ (typ)
- $V_{DS} \leq 40$ V
- $I_D \leq 75$ A
- $P_{tot} \leq 272$ W.

2. Pinning information

Table 1: Pinning - SOT426 and SOT263B, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT426 (D^2-PAK)  SOT263B (TO-220AB)	
2	anode (a)		
3	drain (d)		
4	cathode (k)		
5	source (s)		
mb	mounting base; connected to drain (d)		

PHILIPS

3. Limiting values

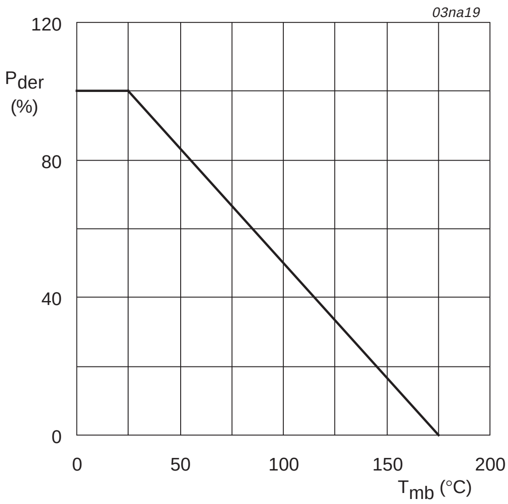
Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	40	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	[1]	-	187	A
			[2]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	[2]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10$ µs; Figure 3		-	748	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	272	W
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[1]	-	187	A
			[2]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10$ µs		-	748	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \le 40$ V; V_{GS} = 10 V; R_{GS} = 50 Ω; starting T_{mb} = 25 °C		-	1.5	J
Electrostatic discharge						
V_{esd}	Electrostatic discharge voltage; pins 1,3,5	Human Body Model; C = 100 pF; R = 1.5 kΩ		-	4	kV

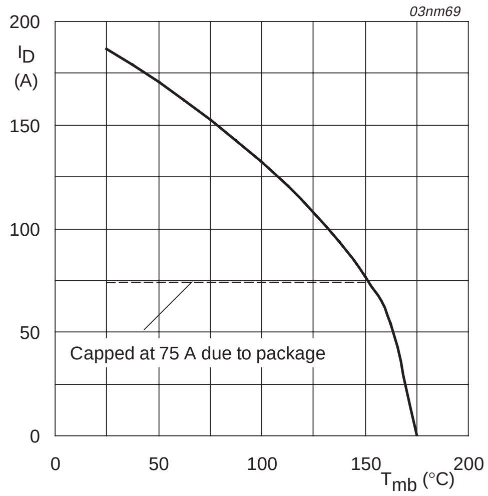
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



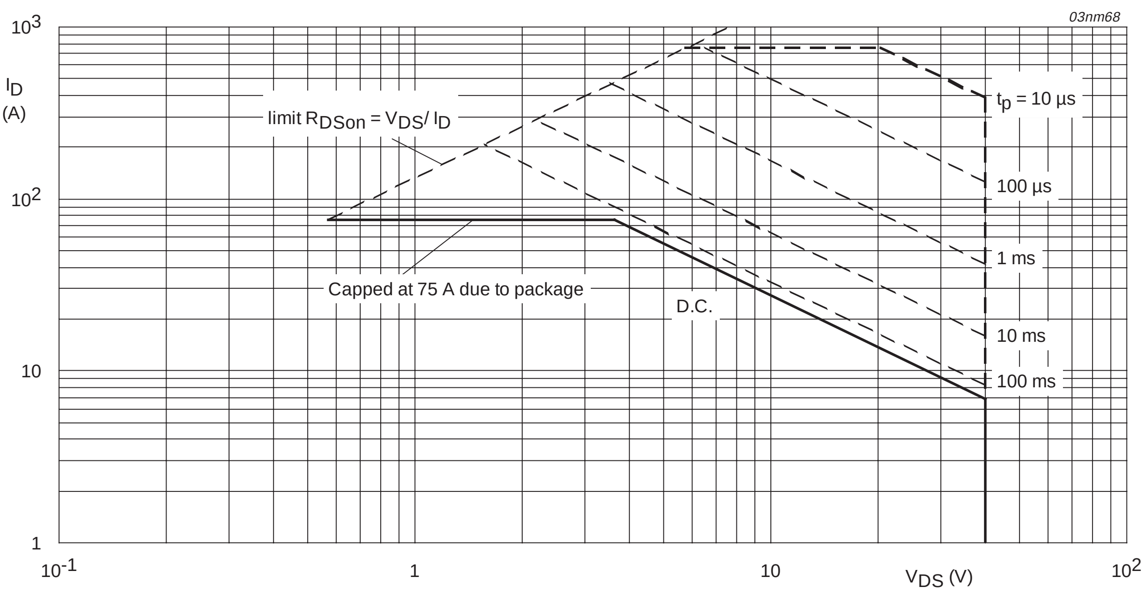
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT263B (TO-220AB)	vertical in still air	-	-	60	K/W
	SOT426 (D^2-PAK)	minimum footprint; mounted on a PCB	-	-	50	K/W

4.1 Transient thermal impedance

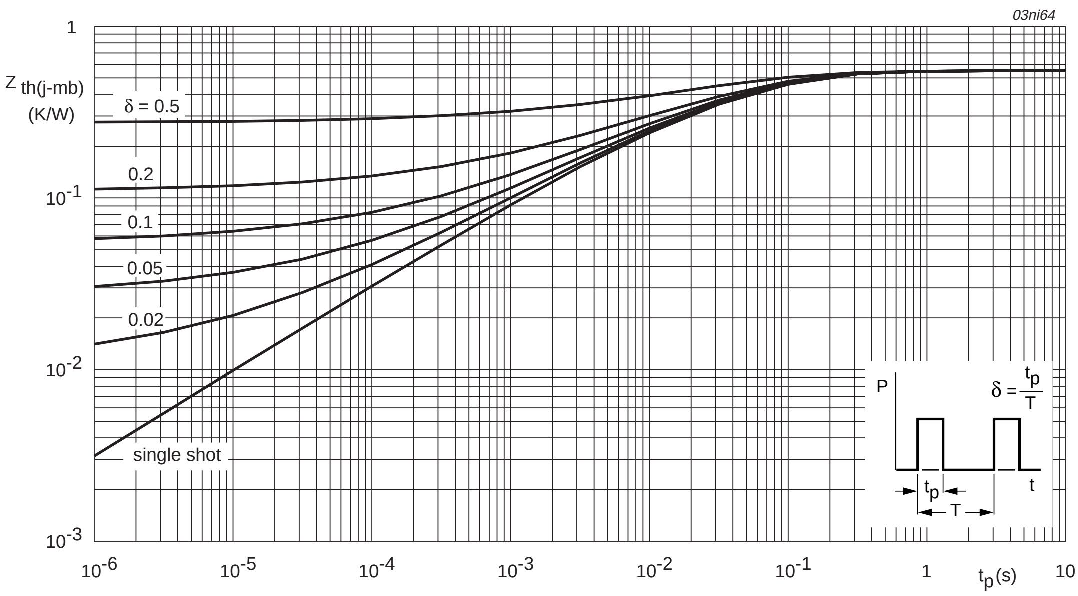


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

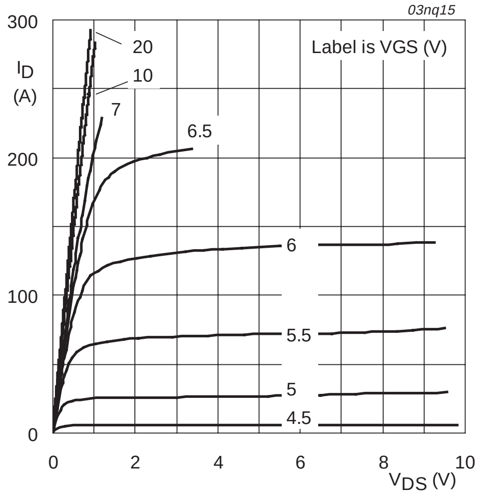
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	40	-	-	V
		T_j = –55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 50 A; Figure 7 and 8				
		T_j = 25 °C	-	3.4	4.1	mΩ
		T_j = 175 °C	-	-	7.8	mΩ
V_F	temperature sense diode forward voltage	I_F = 1 mA	1.58	1.60	1.63	V
S_F	temperature sense diode temperature coefficient	I_F = 1 mA; –55 °C < T_j < 175 °C	–2.55	–2.83	–3.11	mV/K
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	V_{GS} = 10 V; V_{DD} = 32 V; I_D = 25 A; Figure 14	-	83	-	nC
Q_{gs}	gate-to-source charge		-	18	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	29	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	5106	6808	pF
C_{oss}	output capacitance		-	1389	1667	pF
C_{rss}	reverse transfer capacitance		-	527	721	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	38	-	ns
t_r	rise time		-	82	-	ns
$t_{d(off)}$	turn-off delay time		-	141	-	ns
t_f	fall time		-	90	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die SOT263B	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT426	-	2.5	-	nH

Table 4: Characteristics…*continued*

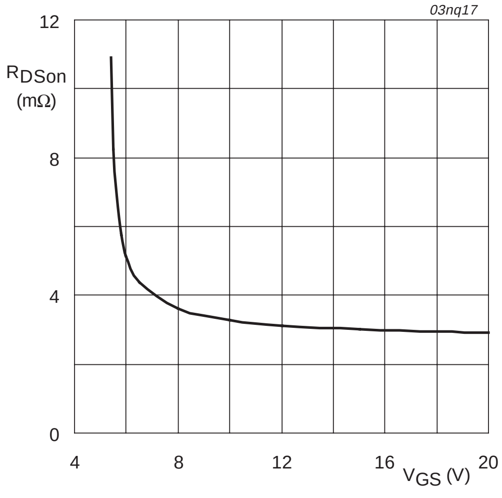
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_s	internal source inductance	from source lead to source bond pad; lead length 6 mm	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 30 V	-	70	-	ns
Q_r	recovered charge		-	55	-	nC



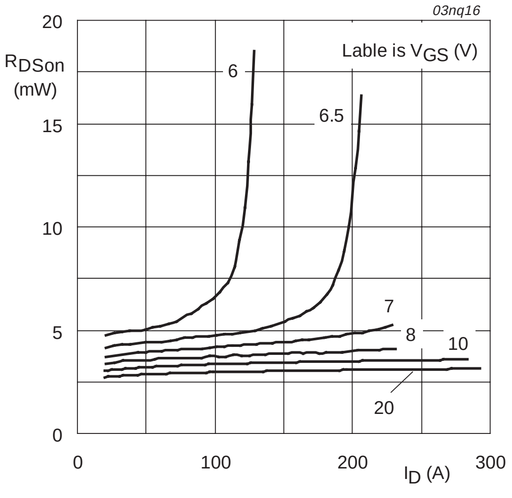
T_j = 25 °C; t_p = 300 µs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



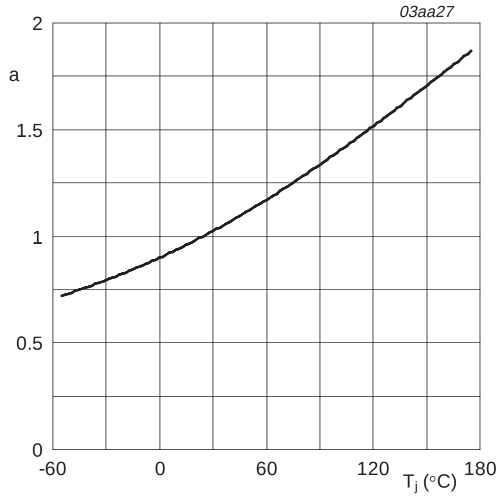
T_j = 25 °C; I_D = 50 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



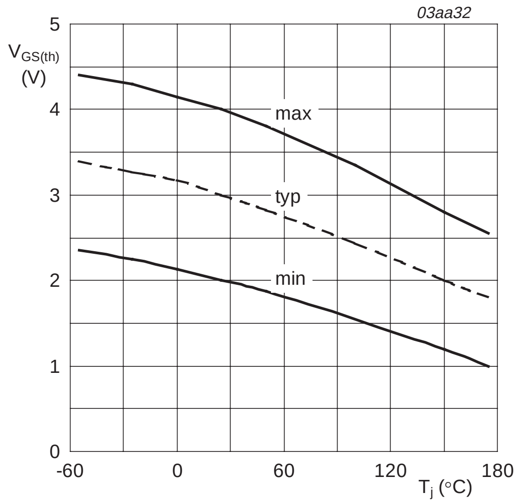
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



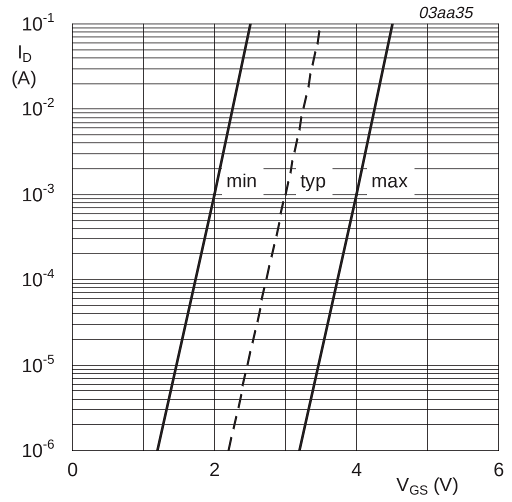
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



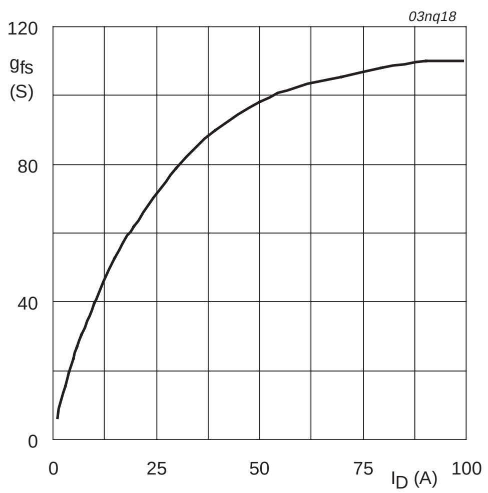
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



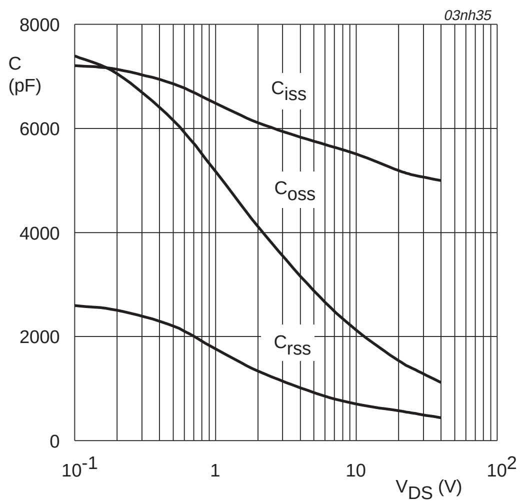
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



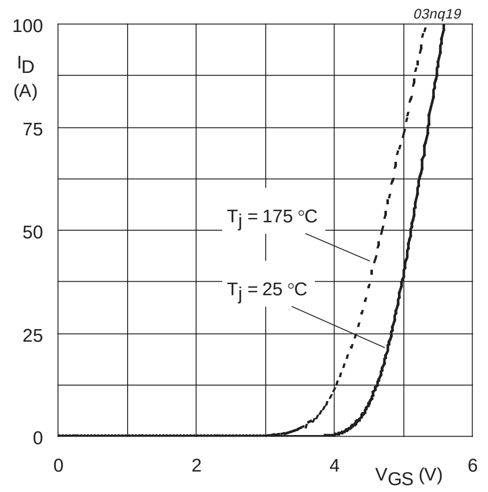
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



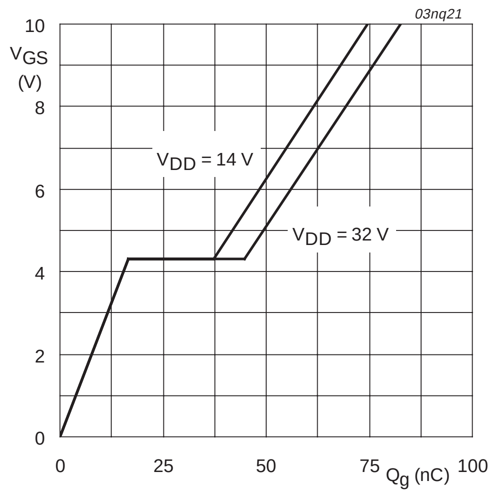
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



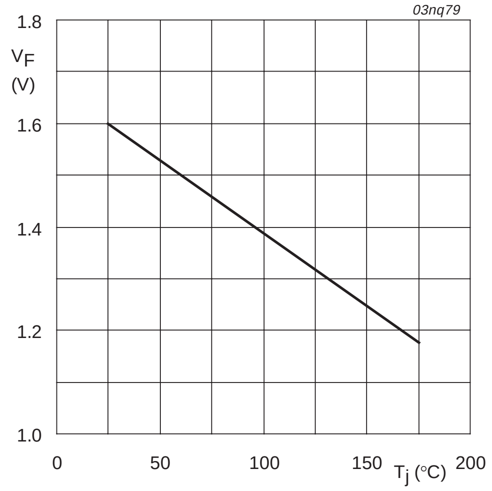
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



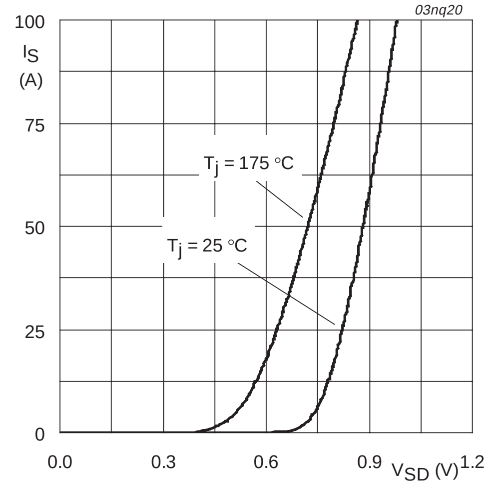
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



I_F = 1 mA

Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values.

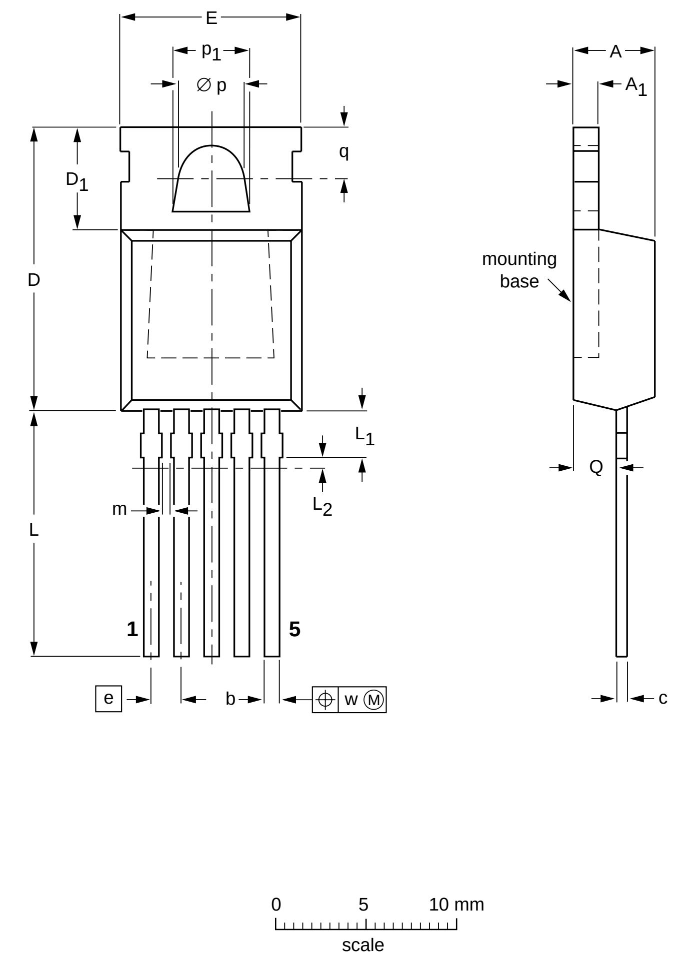


V_{GS} = 0 V

Fig 16. Reverse diode current as a function of reverse diode voltage; typical values.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220 **SOT263B**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	e	L	$L_1^{(1)}$	$L_2^{(2)}$	m	∅ p	p_1	q	Q	w
mm	4.5 4.1	1.39 1.27	0.85 0.70	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	1.7	15.0 13.5	2.4 1.6	0.5	0.8 0.6	3.8 3.6	4.3 4.1	3.0 2.7	2.6 2.2	0.4

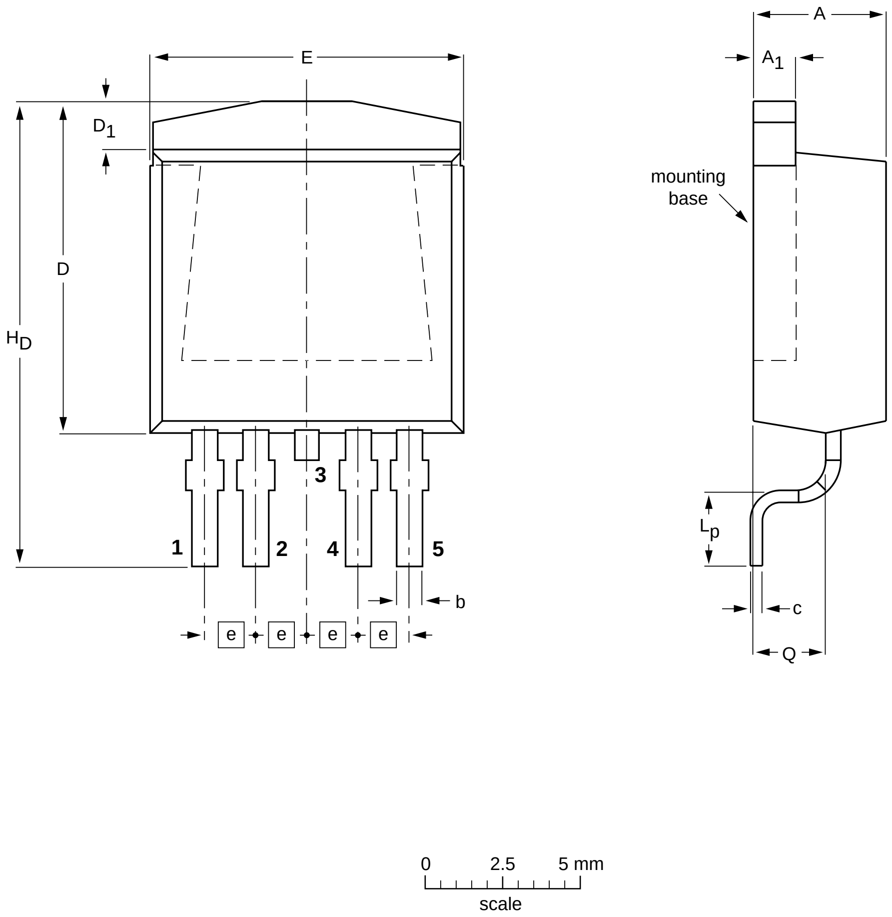
Notes

1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT263B		5-lead TO-220				01-01-11

Fig 17. SOT263B (TO-220AB).

Plastic single-ended surface mounted package (D^2-PAK); 5 leads (one lead cropped) **SOT426**



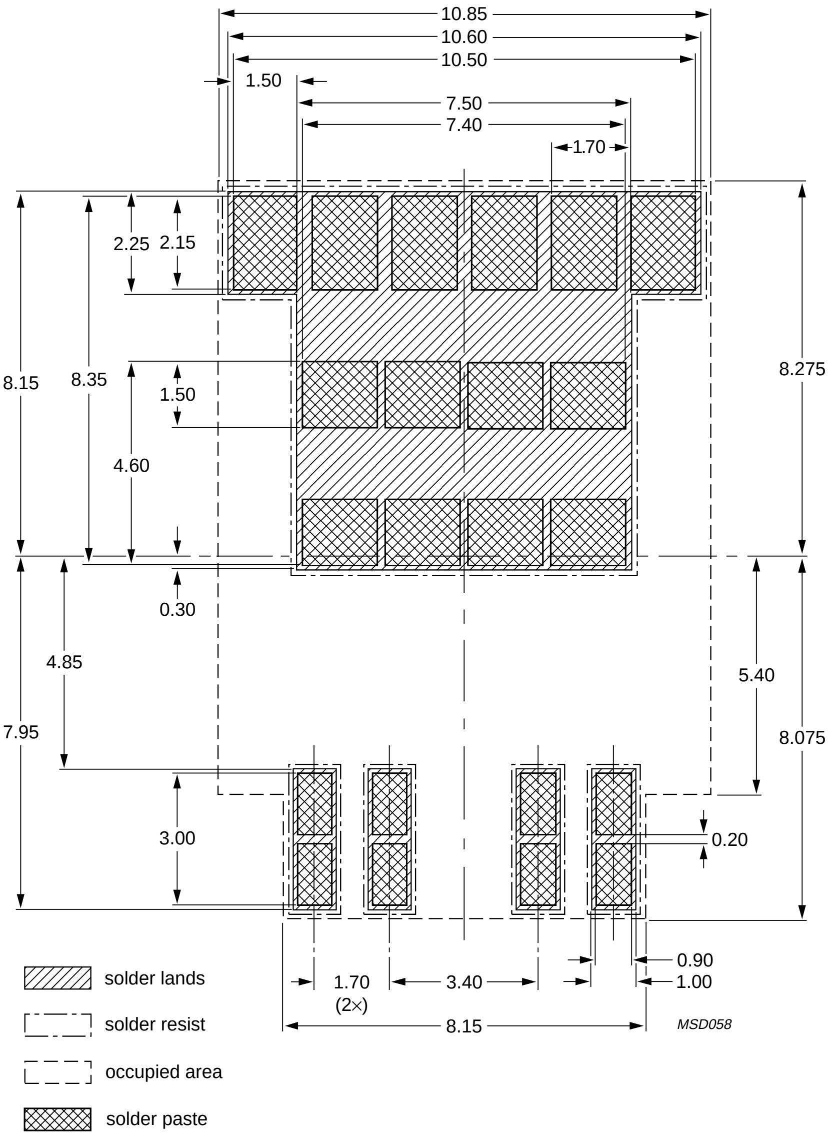
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.70	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT426						~~99-06-25~~ 04-10-13

Fig 18. SOT426 (D^2-PAK)

7. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT426.

8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20041104	-	Product data; initial version.

9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

11. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

12. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Fax: +31 40 27 24825

Contents

Date of release: 4 November 2004 **Document order number: 9397 750 13954**

PHILIPS

Let's make things better.