EK22

INTRODUCTION

The EK22 evaluation kit is designed to provide a convenient way to breadboard design ideas for the SA56 PWM amplifiers. The EVAL25 evaluation board is pre-wired for all required and recommended external components. The EVAL25 also includes a breadboard area for constructing your application circuit including provisions for an output filter. Please refer to applications note 32 in the Apex catalog for guidance in filter component selection. The 1µF ceramic capacitors supplied with the kit are for high frequency bypassing of the VS and VDD supplies (C1 – C3 on the EVAL25 board). An additional user supplied low ESR capacitor of at least 10uF per amp of output current is required for adequate bypass of the VS supply (C4 on the EVAL25 board). Please refer to applications note 30 for help with power supply bypassing and other useful information.

SA56 PROTOTYPE BETA SAMPLES

This evaluation kit is supplied for evaluation of SA56 prototype beta samples. There are some limitations to the SA56 prototypes that must be noted. Suggestions to minimize the effect of these limitations are included.

The SA56 combines both high speed high power switching and low level analog signals on a single silicon chip. The difficulty in achieving clean noise free operation is much greater then that of discrete or hybrid microcircuit designs. Though much care and attention has been given to these considerations in the design and layout of the SA56, there is still some work to be done and these prototypes do not switch as cleanly as necessary for completely trouble free operation.

Grounding for the SA56 is critical. The EVAL25 board has separate ground paths for signal ground (SGND) and power ground (PGND). The signal and power grounds are common at one point on the SA56. Ground loops can be formed if these two grounds are tied together externally. These two grounds are not tied together on the EVAL25 board through trace routing. When building your evaluation circuit, insure that each component referenced to ground is tied to the proper ground path. External components at the high speed, high current output of the SA56 must be returned to PGND.

Analog Mode Operation of the SA56 prototype is affected by switching noise through non-linear operation towards the PWM duty cycle extremes. This limits the useable duty cycle range of the SA56 prototype. The use of external flyback diodes and the use of RC snubbers from each output to ground reduces switching noise, increasing the usable duty cycle range. However the duty cycle should be limited within the range of 5% to 95%.

This kit is supplied with four schottky diodes, p/n SB5100, for use as external flyback diodes (D1 – D4). It is recommended that diodes D1 – D4 be used regardless of the mode of operation.

In addition four 20 ohm, 5W resistors, and two 15nF, 100V capacitors are supplied for use as an RC snubber for each output (C9, R3a, R3b and C10, R4a, R4b). The snubbers are especially useful in reducing the noise generated by the high dv/dt during output switching. The power dissipated in the snubber components can be estimated by;

$P = V^2 * C * FSW$

Where:
P is the power dissipated
V is the VS supply voltage
C is the snubber capacitor value (15nF)
FSW is the switching frequency.

It also is recommended that a low pass RC filter be included on the PWM_IN line for analog mode operation (R2 and C8). A 100 ohm resistor and 2.7nF capacitor worked well for R2 and C8 value during design verification testing. However these may not be the best choice for switching frequency and load configurations other then that used during design verification testing. It is up to the user to determine the best values to use for a given application.

Start-up Faults of the SA56 protection circuits due to noise generated by high current transient pulses at start-up may occur. The SA56 has an internal start-up reset pulse to handle these transients, but the duration of these transients is often longer then the reset pulse.

These transient current pulses will trip the short circuit and over current protection if a high current output is commanded at start-up. It is best if the SA56 can be started up with low output current demand. Examples are starting with the PWM input at mid-range in analog mode, or starting with reduced VS supply voltage.

If a “soft start” is not practical, a start-up reset pulse can be generated on the EVAL25 board with a few external components. Figure 1 is an example of this reset pulse generator. When VDD is applied, the disable pin will be pulled high by capacitor C11 until C11 is discharged by R1. This generates a reset pulse on the disable pin. After the reset pulse is discharged, R1 holds disable at logic low for normal operation. The time constant of C11 and R1 must be a couple of milliseconds longer then the rise time of the VDD supply. A good choice for R1 is 10K - 20K ohms. The VS supply must be turned on before the VDD supply.

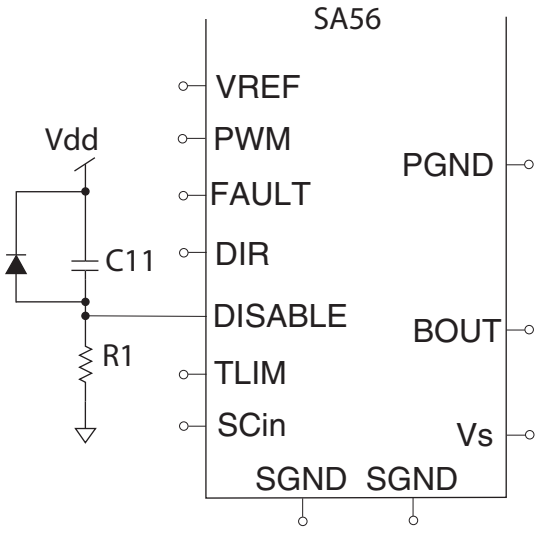


Figure 1. Start-up Reset

It also maybe necessary to bypass the SCin line with a 22pF - 50pF ceramic capacitor. This bypass capacitor will add a time delay to the short circuit protection. However this additional time delay has not resulted in failure during design verification testing of the short circuit protection. The short circuit protection may be disabled entirely by grounding the SCin pin to SGND. Cycle by cycle current limiting will still be active if a current limit resistor is connected from ISEN to SGND. Please refer to the SA56 data sheet for selection of the current limit resistor.

The SA56 prototypes have an extended blocking period in the ISEN output. This blocking period can be several hundreds of nano-seconds. This is a limitation of this feature for the SA56 prototypes that will be corrected in the production SA56 when released.

In 2 quadrant mode of operation, one half bridge of the SA56 is held low while the other half bridge is modulated. This means that no current is sensed at the ISEN pin during the low portion of the output modulation. The ISEN output is not useful for configuring a transconductance amplifier in 2 quadrant operation.

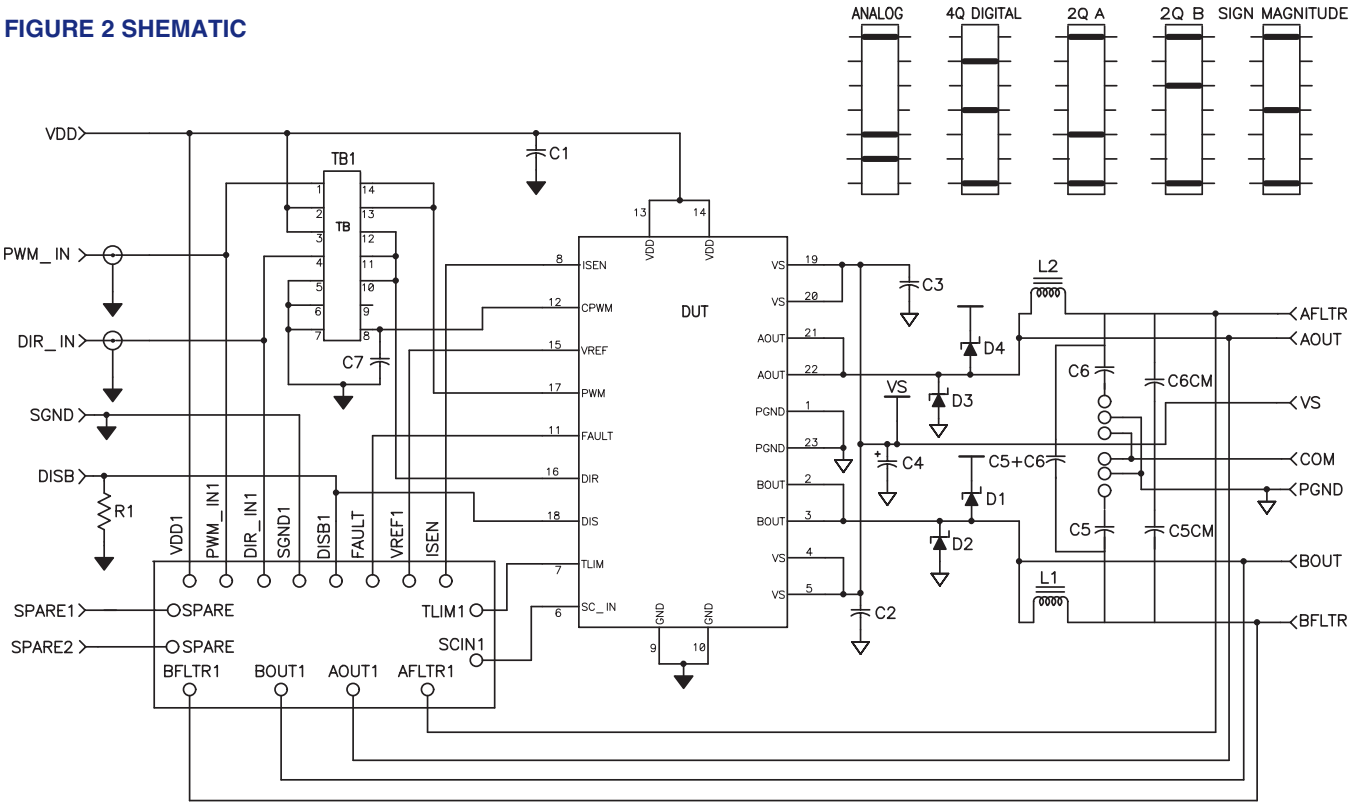
BEFORE YOU GET STARTED

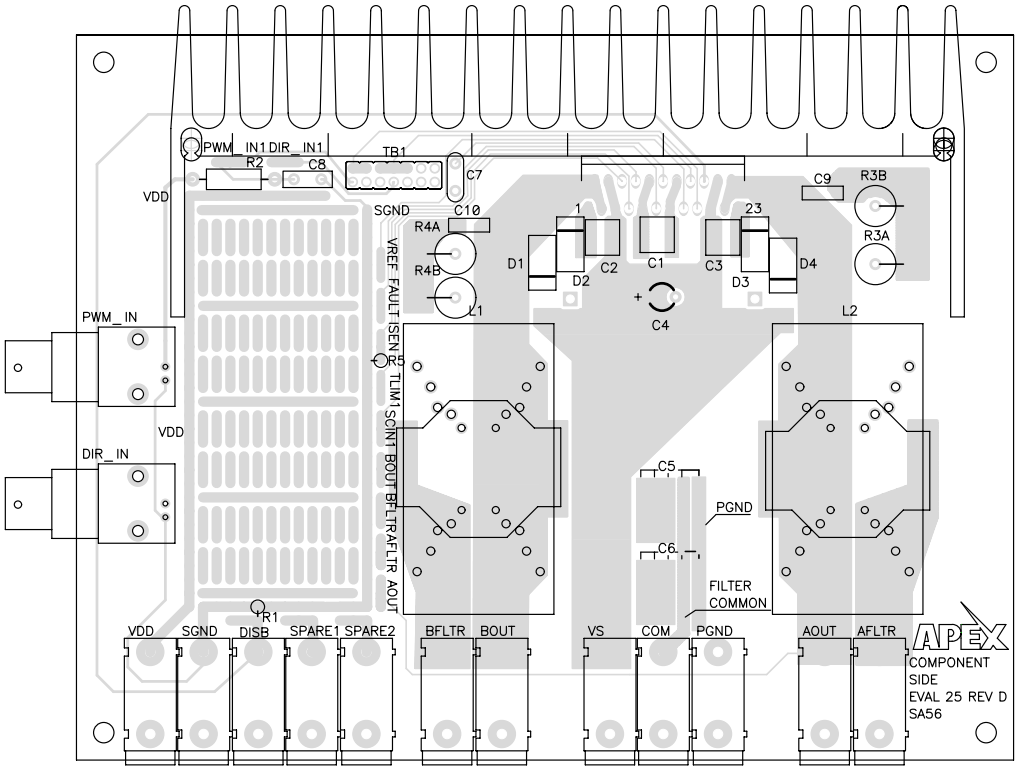
- All Apex amplifiers should be handled using proper ESD precautions.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating voltage allowed in the device data sheet.
- The power supply turn on sequence for the SA56 is VS supply on first followed by the VDD supply. If VDD is turned on before VS, the SA56 will start up in a fault condition that can not be reset until VS is greater then 12V.

PARTS LIST

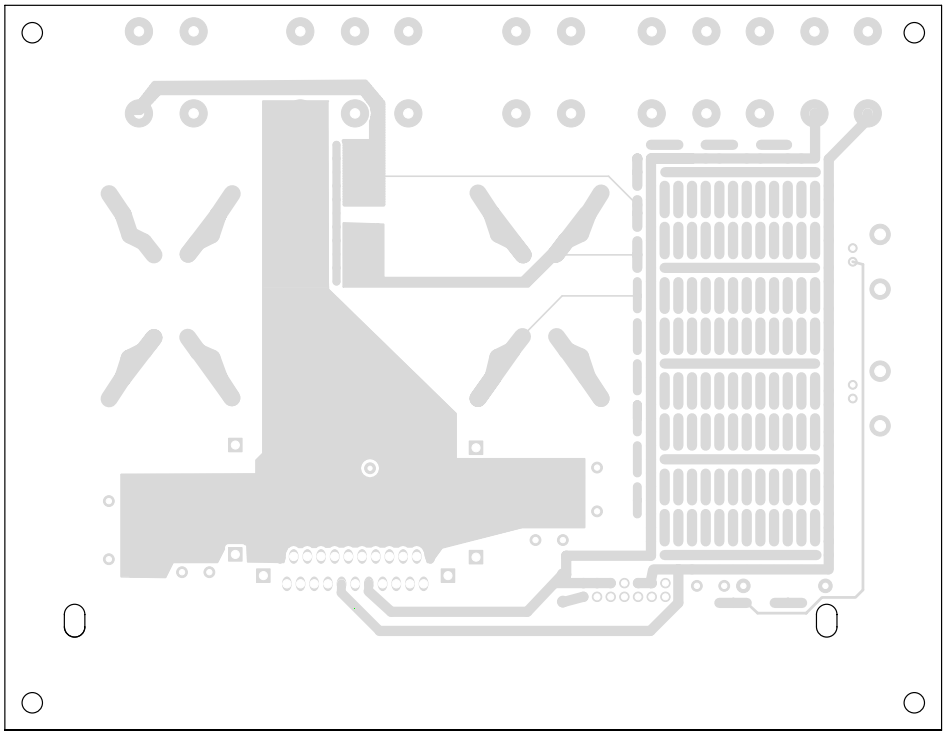
--Ref.	Apex P/N	Description/Vendor	Qty.
NA	HS20	Heat Sink	1
NA	MS11	Strip of 30 Cage Jacks	1
NA	EVAL25	PC board	1
BJ1-12	BJ1	Banana Jack/ Deltron 571-0100	12
BN1, 2	146510CJ	BNC, PCB mount R/A Jameco 146510CJ	2
C1-3	OX7R105KWN	1 µF cap Novacap 1825B105K201N	3
C9, 10	C062K153K1X5CA	15 nF cap	2
D1-4	SB5100	Diode, 100V, 5A	4
R3a-4b	286-20	Resistor, 20 ohm, 5W	4
TB1	PTC07DAAN	Header 2x7 pin	1
J1-3	STC02SYAN	Jumper, shorting	3
NA	TW12	Thermal Washer	1 box

FIGURE 2 SHEMATIC





COMPONENT SIDE



CIRCUIT SIDE

FIGURE 3 PCB

ASSEMBLY

During assembly, refer to Figure 2, 3 and the SA56 data sheet.

1. Note that each side of the circuit board is identified as either the “component side” or “bottom side”. The component side is labeled on the silk screen side of the board.
2. Cut the MS11 into strips of 12 and 11. Discard the remaining small strip. Insert the two strips into the two rows of holes for the DUT from the component side of the PCB. From the bottom side, solder all cage jacks to the circuit board pads. Be sure that the cage jacks are fully seated before soldering. Be careful that the solder does not flow into the cage jack. Remove the plastic carrier strips.
3. Solder the surface mount capacitors at C1 – C3, on the component side of the PCB. The carrier strips removed from the cage jacks in step 2 are convenient as a tool to hold the capacitors in place while soldering. The carrier strips can be discarded when no longer needed for this purpose. Though not required, it is a good idea to fill in the vias on the PGND side of C2 and C3 with solder.
4. From the component side, insert the 4 diodes D1 – D4 into the PCB at the locations marked on the board. Solder the diodes to the PCB from the bottom side.
5. Insert the 14 pin header TB1 into the PCB from the component side. Solder TB1 from the bottom side. Install shorting jumpers J1 – J3 on TB1 to configure the mode of operation for the SA56. Refer to the schematic in figure 2 for jumper positions. The top pair of pins in the schematic diagram for TB1 correspond to the left most pair of pins when TB1 is viewed on the PCB in figure 3.
6. Mount the banana jacks and the BNC connectors to the PCB at locations marked on the PCB as needed or as desired. Solder these from the bottom side of the board.
7. Mount an electrolytic bypass capacitor (not supplied) at C4 from the component side of the PCB. Match the polarity markings on the PCB. Solder the capacitor to the PCB from the bottom side.
8. The SA56 will not function with the ISEN pin open. Select a resistor value and install on the component side of the PCB between ISEN and SGND at the R5 position marked on the PCB. Solder from the bottom side. If a current limit resistor is not used, short the ISEN pads to SGND in place of R5.
9. It is recommended that a 10K to 20K pull down resistor be installed between the disable line and SGND at the location labeled R1. For reliable start-up it is recommended to include a capacitor and diode to VDD as shown in figure 1.
10. For analog mode operation, a PWM timing capacitor is required. Refer to the SA56 datasheet for timing capacitor calculation. Install the timing capacitor in the C7 location.
11. Install the snubber components C9, R3a, R3b and C10, R4a, R4b at the locations labeled on the PCB.
12. If the prototype SA56 will be used in an analog application it is recommended to include an input RC filter in series with the PWM_IN input (R2 and C8). The PWM_IN BNC connector is not routed to the DUT unless a resistor or a shorting wire is installed at the R2 location.
13. Mount other components to complete your application circuit, using the pads and holes provided. Trim all excess leads.
14. The PCB has provisions for a 2 pole output filter. The locations for the inductors L1 and L2 are designed to accept a wide range of sizes for either a through hole or surface mount style of inductor. J.W. Miller series 6700 through hole inductors or series PM2110 surface mount inductors will fit in these locations and include a wide range of inductors suitable for many SA56 applications. These inductors are readily available from Digikey Corp.
15. Partially insert the SA56 device into the cage jacks from the Component side of the PCB.
16. Install the HS20 on the component side of the board, securing the HS20 to the board with two 6-32 self tapping screws (Not supplied) through the elongated holes in the PCB from the bottom side. Place a TW12 thermal washer between the DVT and heatsink. Align the holes in the TW12 to the mounting holes of the DUT.
17. Mount the device to the heat sink with a 4-40 x 1/4“ screw. Make the screw snug but do not over tighten as this provides no benefit and may break the screw.
18. Hook up power and signals as necessary. The amplifier is now ready for testing.