

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

**IDT54/74FCT861A/B
IDT54/74FCT863A/B**

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT861A/863A equivalent to FAST™ speed
- **IDT54/74FCT861B/863B 25% faster than FAST**
- High-speed symmetrical bidirectional transceivers
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

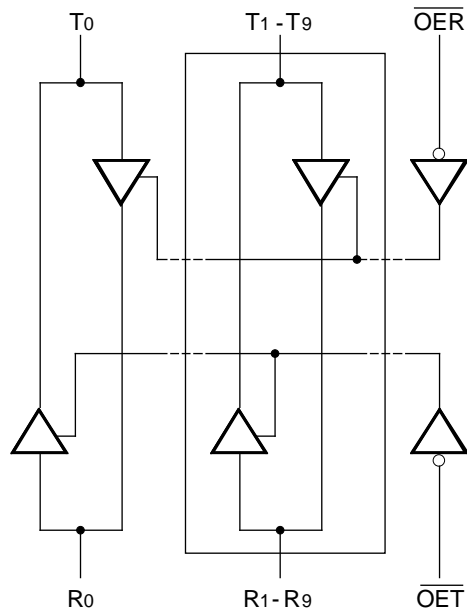
The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT860 series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863 9-bit transceivers have NAND-ed output enables for maximum control flexibility.

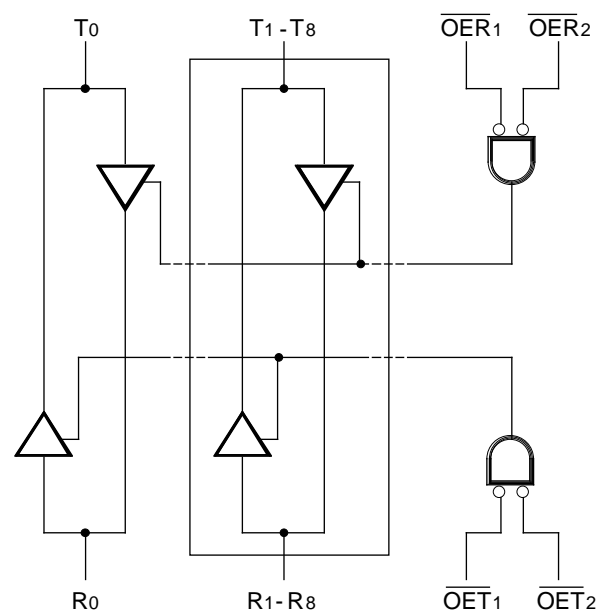
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT861



IDT54/74FCT863



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PRODUCT SELECTOR GUIDE

	Device	
	10-Bit	9-Bit
Non-inverting	IDT54/74FCT861	IDT54/74FCT863

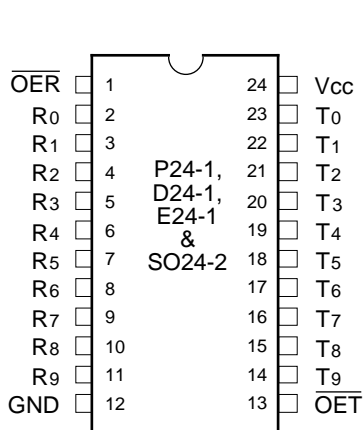
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FAST is a trademark of National Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

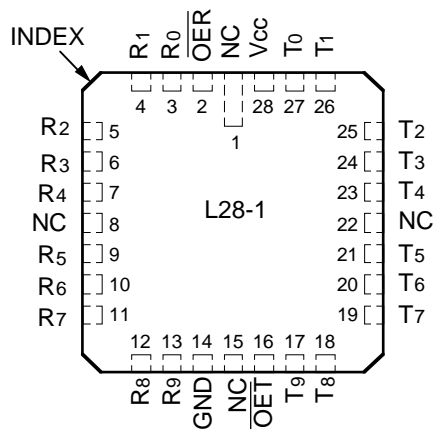
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PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVERS

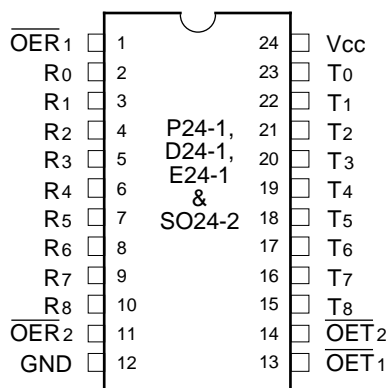


DIP/CERPACK/SOIC
TOP VIEW

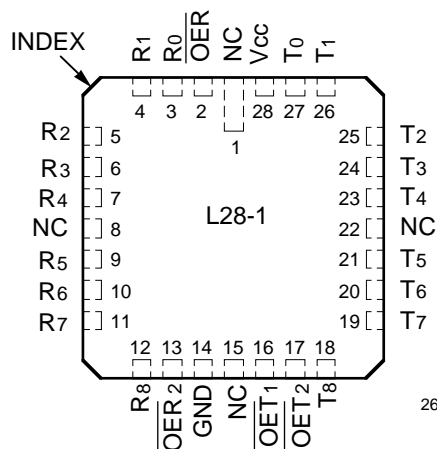


LCC
TOP VIEW

IDT54/74FCT863 9-BIT TRANSCEIVERS



DIP/CERPACK/SOIC
TOP VIEW

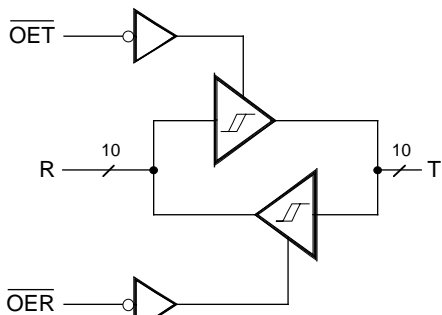


LCC
TOP VIEW

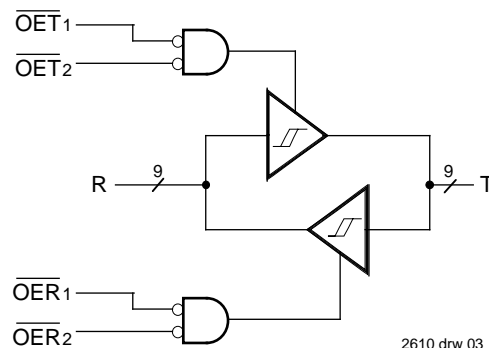
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LOGIC SYMBOLS

IDT54/74FCT861



IDT54/74FCT863



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PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT861		
$\overline{\text{OER}}$	I	When LOW in conjunction with $\overline{\text{OET}}$ HIGH activates the RECEIVE mode.
$\overline{\text{OET}}$	I	When LOW in conjunction with $\overline{\text{OER}}$ HIGH activates the TRANSMIT mode.
Ri	I/O	10-bit RECEIVE input/output.
Ti	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863		
$\overline{\text{OER}}_i$	I	When LOW in conjunction with $\overline{\text{OET}}_i$ HIGH activates the RECEIVE mode.
$\overline{\text{OET}}_i$	I	When LOW in conjunction with $\overline{\text{OER}}_i$ HIGH activates the TRANSMIT mode.
Ri	I/O	9-bit RECEIVE input/output.
Ti	I/O	9-bit TRANSMIT input/output.

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FUNCTION TABLE⁽¹⁾

IDT54/74FCT861/863 (Non-inverting)

Inputs				Outputs		Function
$\overline{\text{OET}}$	$\overline{\text{OER}}$	Ri	Ti	Ri	Ti	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:

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1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{\text{TERM}}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{\text{TERM}}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Inputs and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	$5^{(4)}$	
I_{IL}	Input LOW Current (Except I/O pins)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	$-5^{(4)}$	μA
			$V_I = GND$	—	—	-5	
I_{IH}	Input HIGH Current (I/O pins Only)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	15	μA
			$V_I = 2.7V$	—	—	$15^{(4)}$	
I_{IL}	Input LOW Current (I/O pins Only)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	$-15^{(4)}$	μA
			$V_I = GND$	—	—	-15	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -15mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -24mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
			$I_{OL} = 32mA \text{ MIL.}^{(5)}$	—	0.3	0.5	
			$I_{OL} = 48mA \text{ COM'L.}^{(5)}$	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- These are maximum I_{OL} values per output, for 10 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 480mA for commercial and 320mA for military. Derate I_{OL} for number of outputs exceeding 10 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open \overline{OER} or $\overline{OET} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle \overline{OER} or $\overline{OET} = \text{GND}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.0	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle \overline{OER} or $\overline{OET} = \text{GND}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.2	14.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

2610 tbl 06

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT861A/863A				FCT861B/863B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay RI to TI or TI to RI FCT861/863	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $\overline{\text{OET}}$ to TI or $\overline{\text{OER}}$ to RI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	22.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{\text{OET}}$ to TI or $\overline{\text{OER}}$ to RI	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

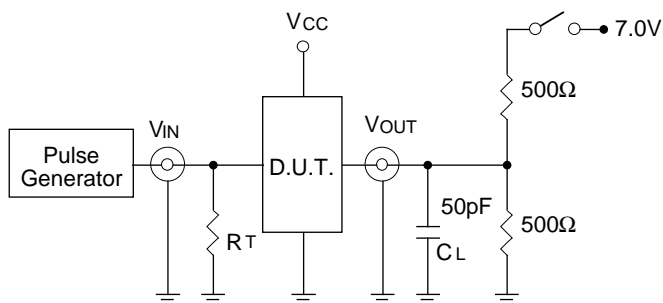
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition guaranteed but not tested.

2610 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

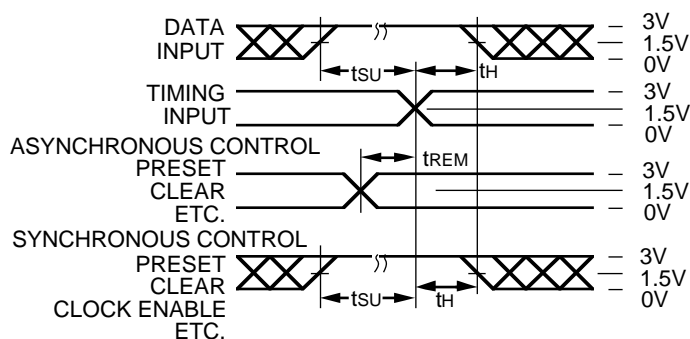
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

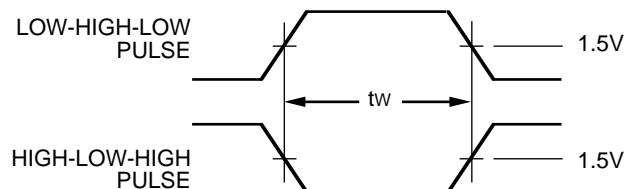
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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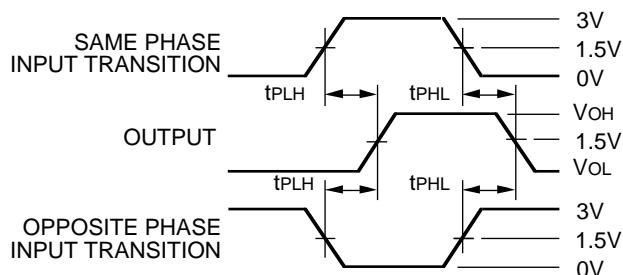
SET-UP, HOLD AND RELEASE TIMES



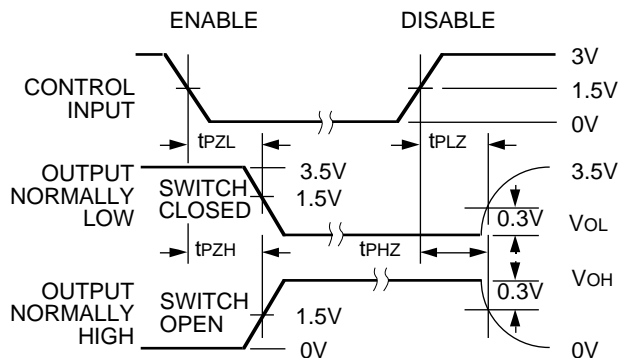
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

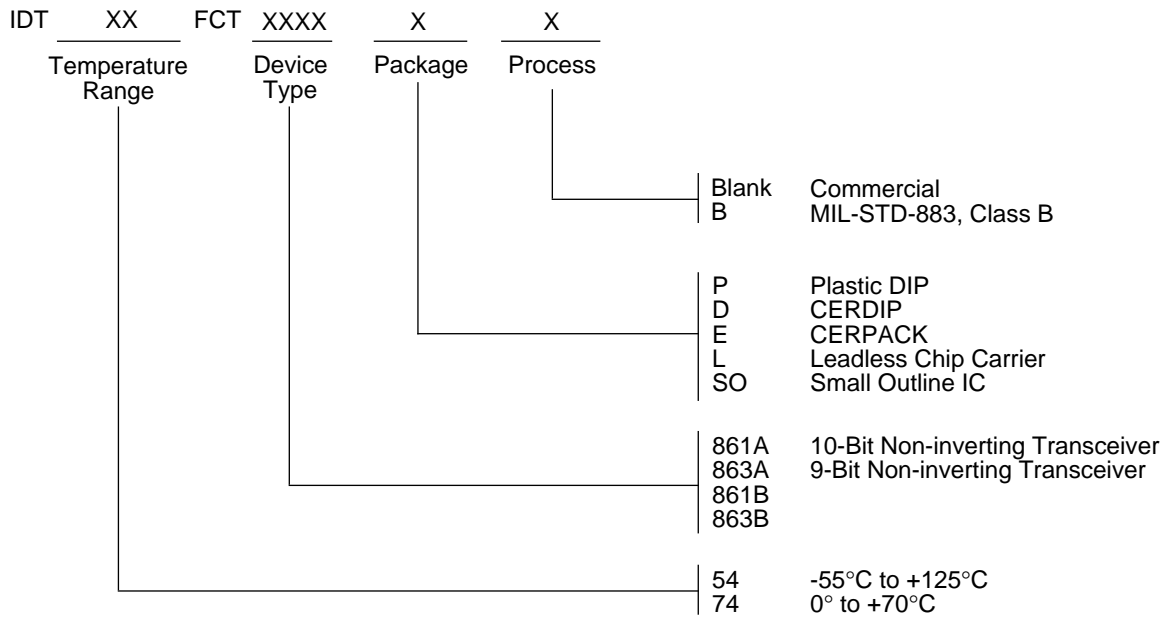


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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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