

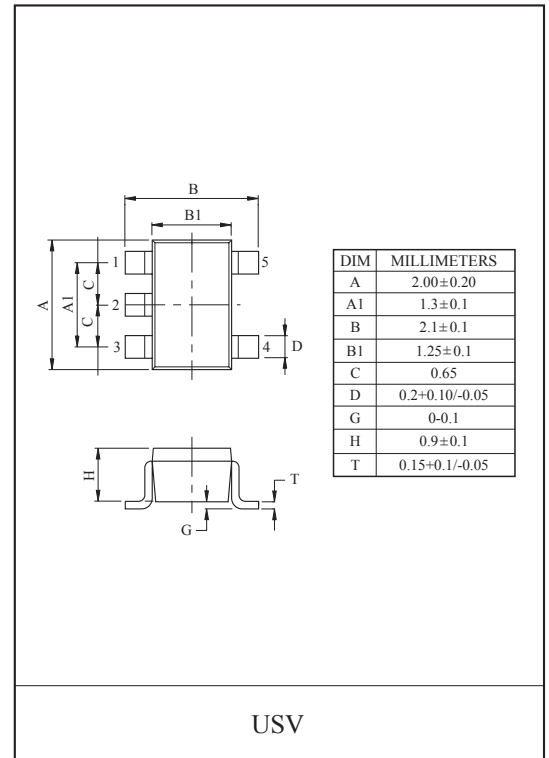
#### 2 INPUT NAND GATE (Open Drain Output)

#### FEATURES

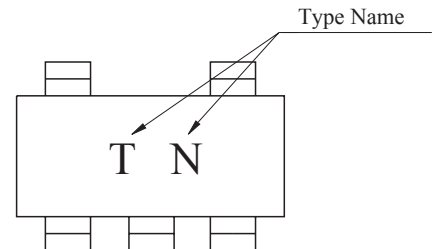
- Open Drain Output Stage for OR tied application.
- Super High Speed : 2.4ns(Typ.) 50pF at  $V_{CC}=5V$ .
- High Output Sink Drive : 24mA at  $V_{CC}=3V$ .
- Operating Voltage Range :  $V_{CC(opr)}=1.65\sim 5.5V$ .
- Power Down High Impedance Inputs/Outputs.

#### MAXIMUM RATINGS (Ta=25°C)

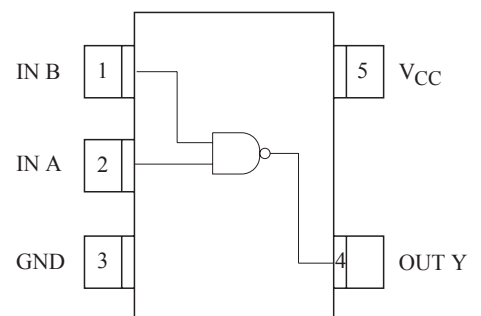
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage Range	$V_{CC}$	-0.5~6	V
DC Input Voltage	$V_{IN}$	-0.5~6	V
DC Output Voltage	$V_{OUT}$	-0.5~6	V
Input Diode Current	$I_{IK}$	-50~20	mA
Output Diode Current	$I_{OK}$	-50~20	mA
DC Output Current	$I_{OUT}$	50	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	200	mW
Storage Temperature Range	$T_{stg}$	-65 ~ 150	°C
Lead Temperature (10s)	$T_L$	260	°C



#### MARKING



#### PIN CONNECTION(TOP VIEW)



# KIC7SZ38FU

## Logic Diagram



## ELECTRICAL CHARACTERISTICS

### DC Characteristics

CHARACTERISTIC		SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT	
					V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Input Voltage	High Level	V <sub>IH</sub>	-	1.65~1.95	0.75 × V <sub>CC</sub>	-	-	0.75 × V <sub>CC</sub>	-	V	
				2.3~5.5	0.7 × V <sub>CC</sub>	-	-	0.7 × V <sub>CC</sub>	-		
	Low Level	V <sub>IL</sub>	-	1.65~1.95	-	-	0.25 × V <sub>CC</sub>	-	0.25 × V <sub>CC</sub>		
				2.3~5.5	-	-	0.3 × V <sub>CC</sub>	-	0.3 × V <sub>CC</sub>		
Output Leakage Voltage	High Level	I <sub>LKG</sub>	V <sub>IN</sub> =V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND	5.5	-	-	±5	-	±10	μA	
	Low Level	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub>	I <sub>OL</sub> =100μA	1.65	-	0	0.1	-	0.1	V
					1.8	-	0	0.1	-	0.1	
					2.3	-	0	0.1	-	0.1	
					3.0	-	0	0.1	-	0.1	
					4.5	-	0	0.1	-	0.1	
				I <sub>OL</sub> =4mA	1.65	-	0.08	0.24	-	0.24	
				I <sub>OL</sub> =8mA	2.3	-	0.10	0.3	-	0.3	
				I <sub>OL</sub> =16mA	3.0	-	0.15	0.4	-	0.4	
				I <sub>OL</sub> =24mA	3.0	-	0.22	0.55	-	0.55	
I <sub>OL</sub> =32mA	4.5	-	0.22	0.55	-	0.55					
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> =5.5V or GND	0~5.5	-	-	±1	-	±10	μA	
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> or V <sub>OUT</sub> =5.5V	0.0	-	-	1	-	10	μA	
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> =5.5V or GND	5.5	-	-	2.0	-	20	μA	

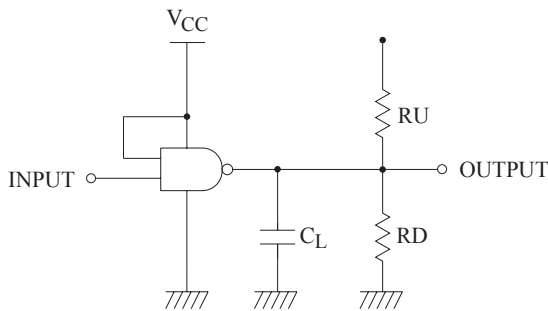
# KIC7SZ38FU

AC Characteristics (unless otherwise specified, Input :  $t_r=t_f=3ns$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation delay time	t <sub>pZL</sub>	C <sub>L</sub> =50pF, R <sub>U</sub> =500Ω R <sub>D</sub> =500Ω V <sub>I</sub> =2×V <sub>CC</sub> (Figures 1,3)	1.65	1.5	6.5	12.7	1.5	13.2	ns
			1.8	1.5	5.4	10.5	1.5	11.0	
			2.5±0.2	0.8	3.5	7.0	0.8	7.5	
			3.3±0.3	0.8	2.8	5.0	0.8	5.2	
			5.0±0.5	0.5	2.2	4.3	0.5	4.5	
	t <sub>pLZ</sub>	C <sub>L</sub> =50pF, R <sub>U</sub> =500Ω R <sub>D</sub> =500Ω V <sub>I</sub> =2×V <sub>CC</sub> (Figures 1,3)	1.65	1.5	5.5	12.7	1.5	13.2	ns
			1.8	1.5	4.6	10.5	1.5	11.0	
			2.5±0.2	0.8	3.0	7.0	0.8	7.5	
			3.3±0.3	0.8	2.1	5.0	0.8	5.2	
			5.0±0.5	0.5	1.3	4.3	0.5	4.5	
Input Capacitance	C <sub>IN</sub>	-	0	-	4	-	-	pF	
Output Capacitance	C <sub>OUT</sub>	-	0	-	5	-	-	pF	
Power Dissipation Capacitance	C <sub>PD</sub>	(Note) (Figures 2)	3.3	-	5.1	-	-	-	pF
			5.0	-	7.3	-	-	-	

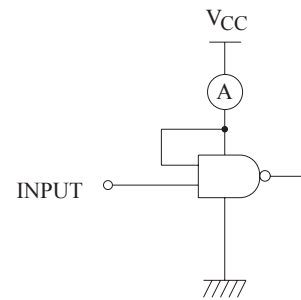
Note : C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression :  $I_{CCD}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC} \text{ Static}$

## AC Loading and Waveforms



C<sub>L</sub> includes load and stray capacitance  
Input PRR=1.0MHz ; t<sub>w</sub>=500ns

FIGURE 1. AC Test Circuit



Input=AC Waveform ; t<sub>r</sub>=t<sub>f</sub>=1.8ns  
PRR=10MHz ; Duty Cycle=50%

FIGURE 2. I<sub>CCD</sub> Test Circuit

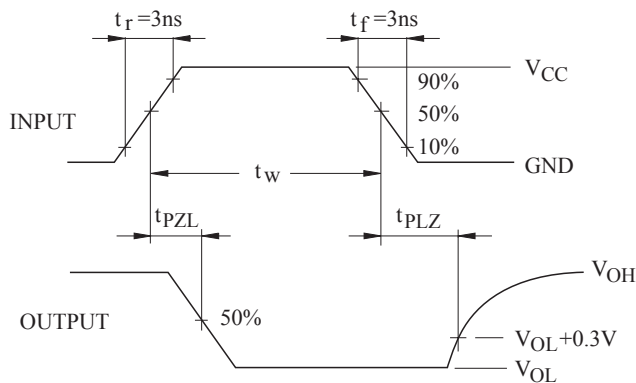


FIGURE 3. AC Waveforms