Description

The M16C/62M (80-pin version) group (low voltage version) of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office, communications, industrial equipment, and other high-speed processing applications.
The M16C/62M (80-pin version) group (low voltage version) includes a wide range of products with different internal memory types and sizes and various package types.

Features

- Memory capacity ..... ROM (See Figure 1.1.3. ROM Expansion)
  RAM 10K to 20K bytes
- Shortest instruction execution time ..... 100ns ($f(X_{IN})$=10MHz, V_{CC}=2.7V to 3.6V)
  142.9ns ($f(X_{IN})$=7MHz, V_{CC}=2.2V to 3.6V, with software one-wait)
- Supply voltage ..... 2.7V to 3.6V ($f(X_{IN})$=10MHz, without software wait)
  2.4V to 2.7V ($f(X_{IN})$= 7MHz, without software wait)
  2.2V to 2.4V ($f(X_{IN})$= 7MHz, with software one-wait)
- Low power consumption ..... 28.5mW ($f(X_{IN})$=10MHz, with software one-wait, V_{CC} = 3V)
- Interrupts ..... 25 internal and 5 external interrupt sources, 4 software interrupt sources; 7 levels (including key input interrupt)
- Multifunction 16-bit timer ..... 5 output timers + 6 input timers (3 for timer function only)
- Serial I/O ..... 5 channels (2 for UART or clock synchronous, 1 for UART, 2 for clock synchronous)
- DMAC ..... 2 channels (trigger: 24 sources)
- A-D converter ..... 10 bits X 8 channels (Expandable up to 10 channels)
- D-A converter ..... 8 bits X 2 channels
- CRC calculation circuit ..... 1 circuit
- Watchdog timer ..... 1 line
- Programmable I/O ..... 70 lines
- Input port ..... 1 line ($P8_5$ shared with $\overline{NMI}$ pin)
- Clock generating circuit ..... 2 built-in clock generation circuits
  (built-in feedback resistor, and external ceramic or quartz oscillator)

Note: Memory expansion mode and microprocessor mode are not supported.

Applications

Audio, cameras, office equipment, communications equipment, portable equipment

Pin Configuration

Figures 1.1.1 show the pin configurations (top view).

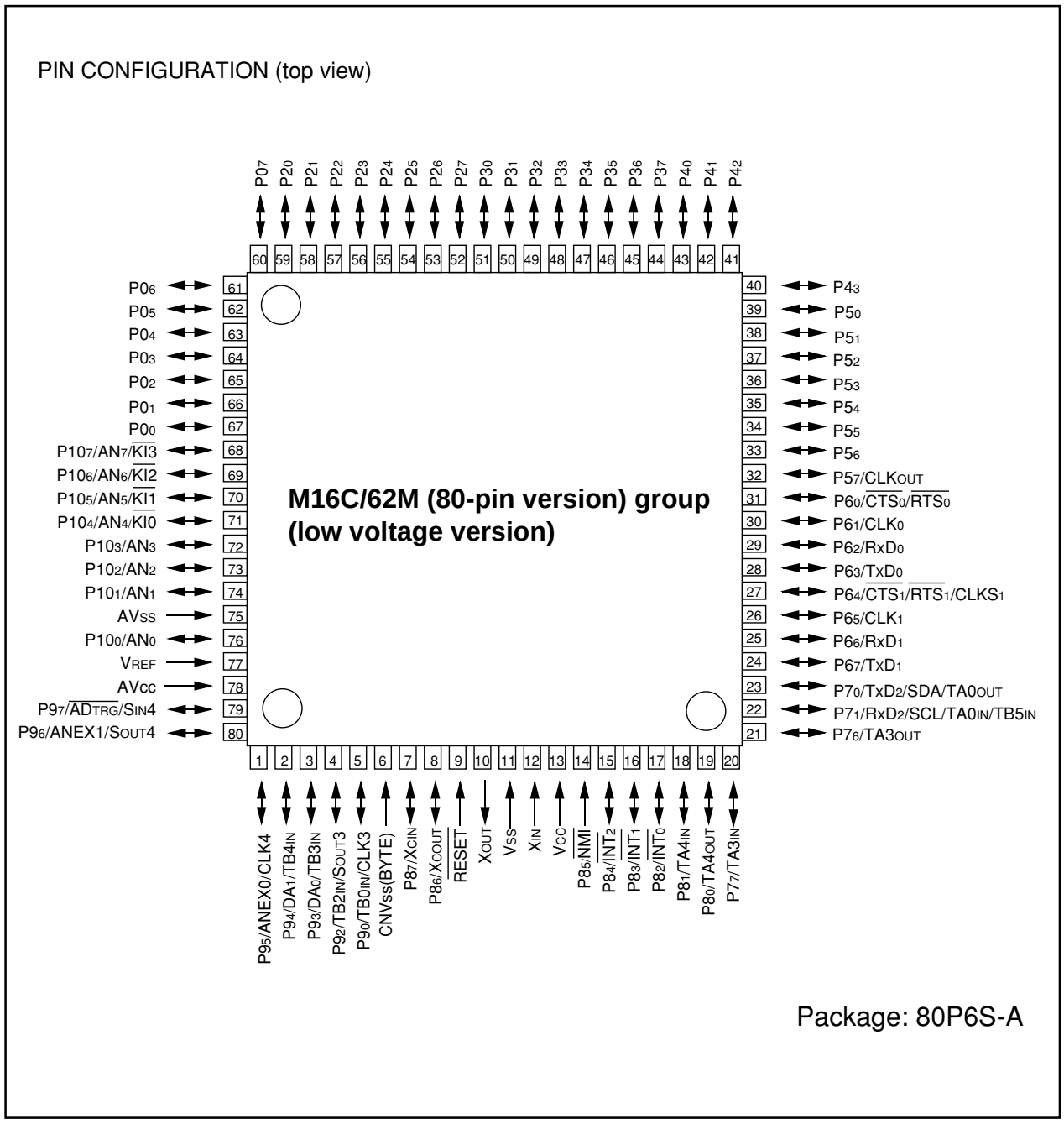


Figure 1.1.1. Pin configuration (top view)

Block Diagram

Figure 1.1.2 is a block diagram of the M16C/62M (80-pin version) group (low voltage version).

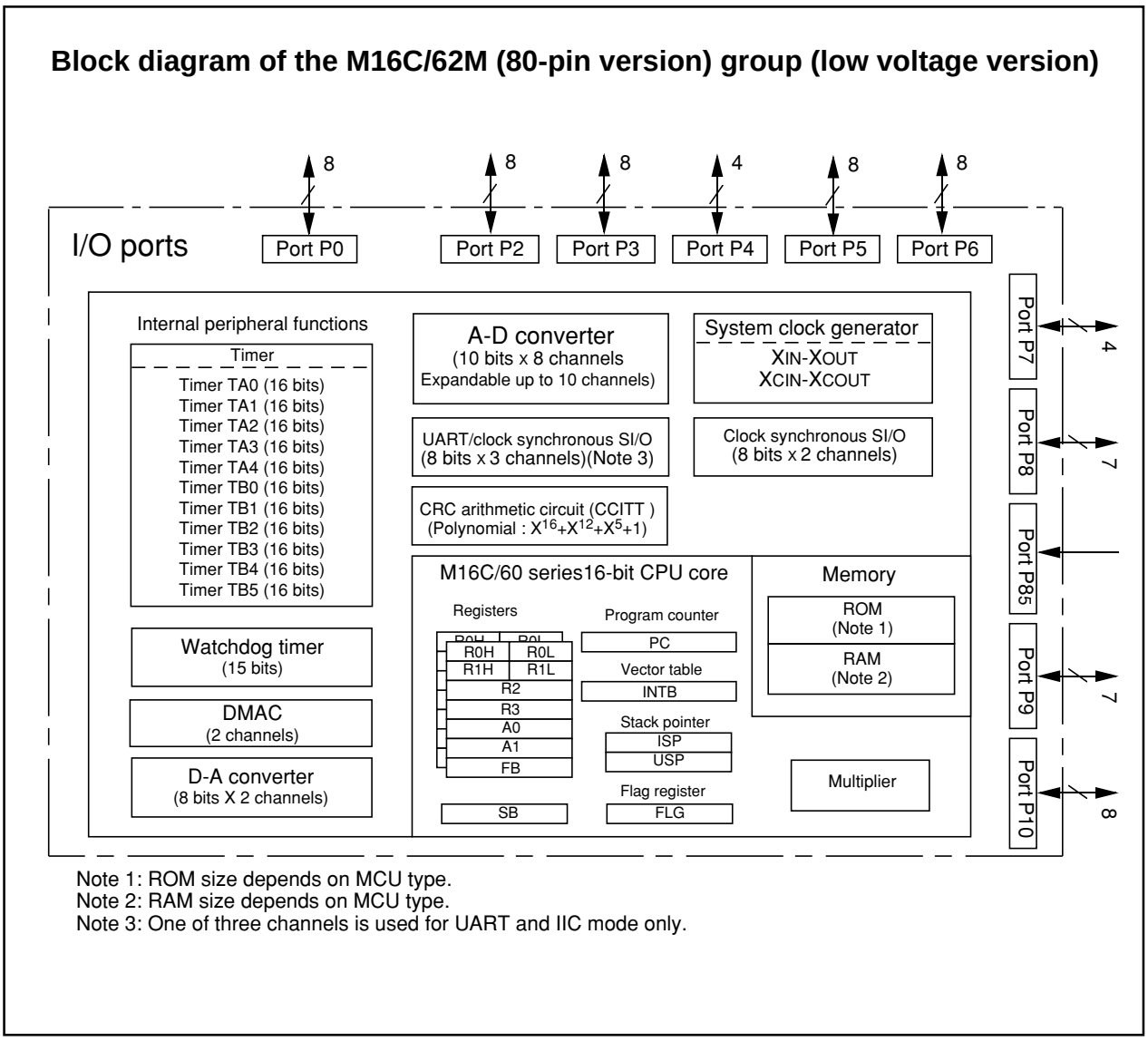


Figure 1.1.2. Block diagram of M16C/62M (80-pin version) group (low voltage version)

Performance Outline

Table 1.1.1 is a performance outline of M16C/62M (80-pin version) group (low voltage version).

Table 1.1.1. Performance outline of M16C/62M (80-pin version) group (low voltage version)

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		100ns(f(XIN)=10MHz, VCC=2.7V to 3.6V) 142.9ns (f(XIN)=7MHz, VCC=2.2V to 3.6V, with software one-wait)
Memory capacity	ROM	(See the figure 1.1.3. ROM Expansion)
	RAM	10K to 20K bytes
I/O port	P0 to P10 (except P85)	8 bits x 6, 7 bits x 2, 4 bits x 2
Input port	P85	1 bit x 1
Multifunction timer	TA0, TA3, TA4	16 bits x 3 (timer mode, internal/external event count, one-shot timer mode and pulse width measurement mode)
	TB0, TB2, TB3, TB4, TB5	16 bits x 5 (timer mode, internal/external event count and pulse period/pulse width measurement mode)
	TA1, TA2	16 bits x 2 (timer mode, internal event count and a trigger through one-shot timer mode occurs.)
	TB1	16 bits x 1 (timer mode and internal event count)
Serial I/O	UART0, UART1, UART2	(UART or clock synchronous) x 2, UART x 1(UART2)
	SI/O3, SI/O4	(Clock synchronous) x 2 (SI/O3 is output only)
A-D converter		10 bits x (8 + 2) channels
D-A converter		8 bits x 2
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		CRC-CCITT
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 5 external sources, 4 software sources, 7 levels
Clock generating circuit		2 built-in clock generation circuits (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage		2.7V to 3.6V (f(XIN)=10MHz, without software wait) 2.4V to 2.7V (f(XIN)= 7MHz, without software wait) 2.2V to 2.4V (f(XIN)= 7MHz, with software one-wait)
Power consumption		28.5mW (f(XIN) = 10MHz, VCC=3V with software one-wait)
I/O characteristics	I/O withstand voltage	3V
	Output current	1mA
Device configuration		CMOS high performance silicon gate
Package		80-pin plastic mold QFP

Note : M16C/62M (80-pin version) group (low voltage version) does not support memory expansion or microprocessor mode.

Mitsubishi plans to release the following products in the M16C/62M (80-pin version) group (low voltage version):

(1) Support for mask ROM version and flash memory version

(2) ROM capacity

(3) Package

80P6S-A : Plastic molded QFP (mask ROM and flash memory versions)

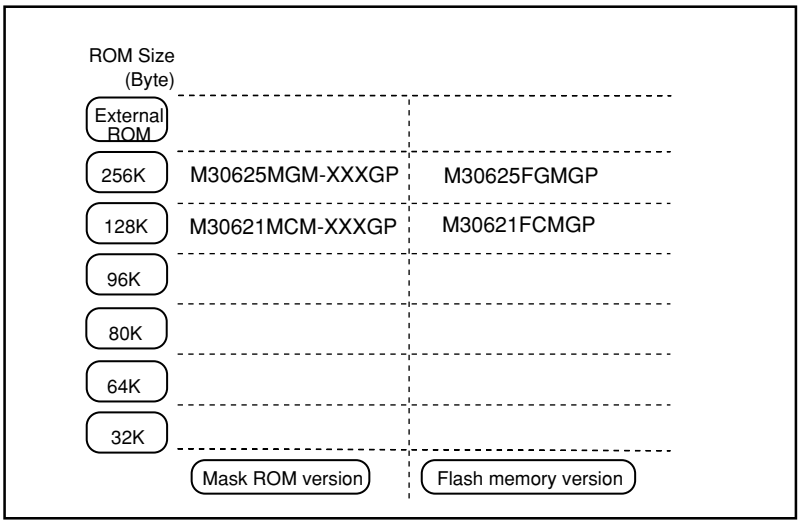


Figure 1.1.3. ROM expansion

The M16C/62M (80-pin version) group (low voltage version) products currently supported are listed in Table 1.1.2.

Table 1.1.2. M16C/62M (80-pin version) group (low voltage version)

As of April 2002

Type No	ROM capacity	RAM capacity	Package type	Remarks
M30621MCM-XXXGP	128 Kbytes	10 Kbytes	80P6S-A	mask ROM version
M30625MGM-XXXGP	256 Kbytes	20 Kbytes	80P6S-A	
M30621FCMGP	128 Kbytes	10 Kbytes	80P6S-A	Flash memory 3V version
M30625FGMGP	256 Kbytes	20 Kbytes	80P6S-A	

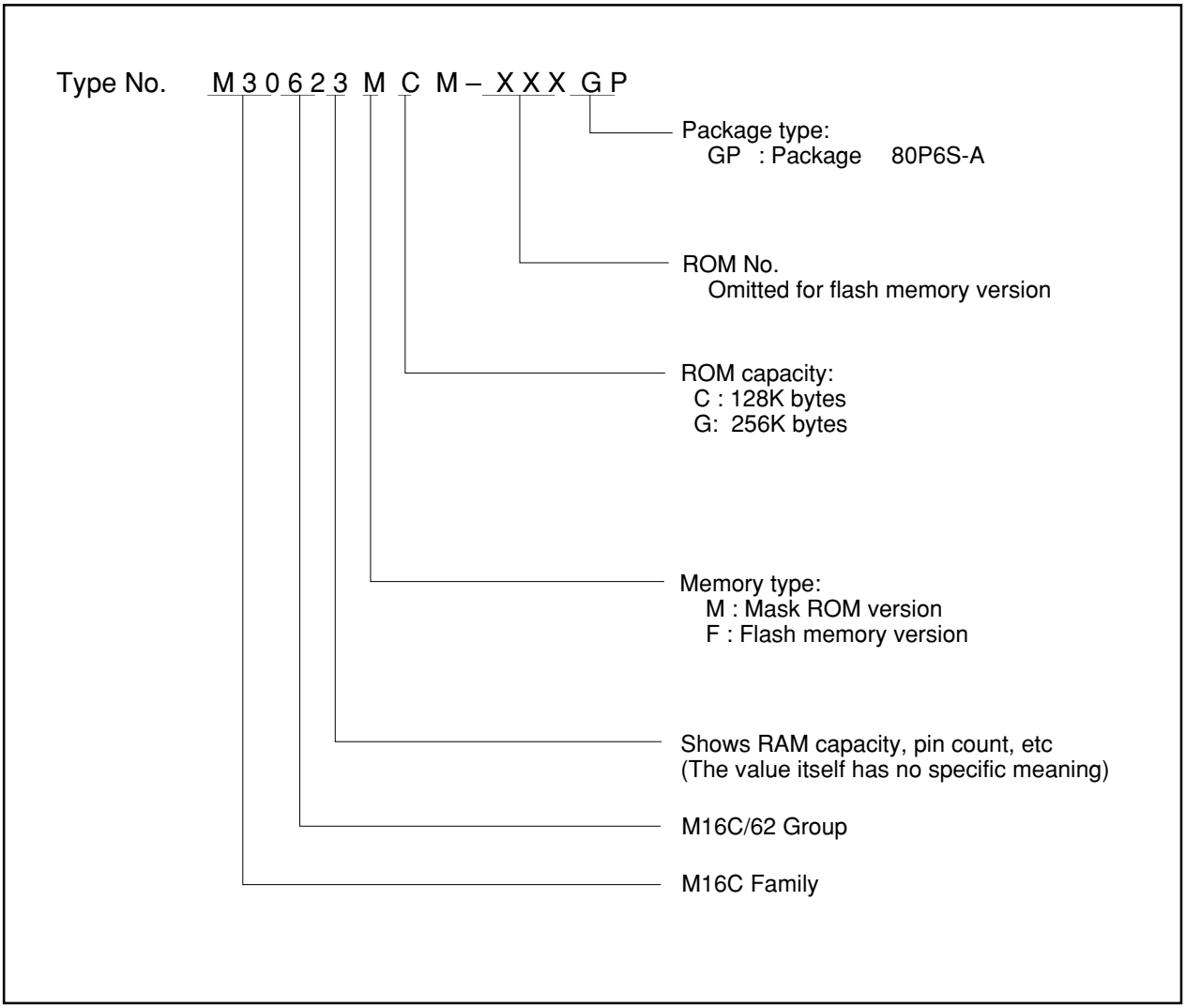


Figure 1.1.4. Type No., memory size, and package

About the M16C/62M (80-pin version) group (low voltage version)

The M16C/62M (80-pin version) group (low voltage version) is packaged in a 80-pin plastic mold package. The number of pins in comparison with the 100-pin package products is decreased. So be careful about the following.

(a) The M16C/62M (80-pin version) group (low voltage version) supports single chip mode alone. It supports neither memory expansion mode nor microprocessor mode.

(b) The input/output ports given below are absent from the M16C/62M (80-pin version) group (low voltage version). To stabilize the internal state, set to output mode the direction register of each input/output port. Failing in setting to output mode involves an increase in current consumption.

<Pins absent from the 80-pin version>
$P1_0$ to $P1_7$, $P4_4$ to $P4_7$, $P7_2$ to $P7_5$, $P9_1$

(c) INT3 to INT5 allocated to $P1_5$ to $P1_7$ cannot be used. Keep the INT3 interrupt control register disabled for interrupts. The INT4 interrupt control register and the INT5 interrupt control register are shared with SI/O3 and SI/O4. When the user don't use them as SI/O3 and SI/4, set them disabled for interrupts.

(d) The output pins of timers A1 and A2 - $TA1_{IN}$, $TA1_{OUT}$, $TA2_{IN}$ and $TA2_{OUT}$ - allocated to $P7_2$ to $P7_5$ cannot be used. In connection with this, the gate function and pulse outputting function of timers A1 and A2 cannot be used. Use timer mode and internal event count, or use as trigger signal generation in one-shot timer mode.

(e) The UART2 input/output pins - CLK2 and $\overline{CTS}/\overline{RTS}$ - allocated to $P7_2$ and $P7_3$ cannot be used. In connection with this, UART2 solely as UART of the internal clock can be used.

(f) The input pin $TB1_{IN}$ of timer B1 allocated to $P9_1$ cannot be used. With timer B1 under this state, use only timer mode or the internal event count.

(g) The input pin S_{IN3} of serial I/O3 allocated to $P9_1$ cannot be used. In connection with this, use serial I/O3 as a serial I/O exclusive to transmission.

(h) The output pins for three-phase motor control allocated to $P7_2$ to $P7_5$ cannot be used. So set to 0 (ordinary mode) the mode select bit (bit 2) of three-phase PWM control register 0.

Electrical characteristics (Vcc = 3V)

Table 1.20.1. Absolute maximum ratings

Symbol	Parameter		Condition	Rated value	Unit
Vcc	Supply voltage		VCC=AVCC	-0.3 to 4.6	V
AVcc	Analog supply voltage		VCC=AVCC	-0.3 to 4.6	V
VI	Input voltage	$\overline{\text{RESET}}$, CNVSS (BYTE) P00 to P07, P20 to P27, P30 to P37, P40 to P43, P50 to P57, P60 to P67, P76 to P77, P80 to P87, P90, P92 to P97, P100 to P107, VREF, XIN		-0.3 to Vcc+0.3	V
		P70, P71		-0.3 to 4.6	V
VO	Output voltage	P00 to P07, P20 to P27, P30 to P37,P40 to P43, P50 to P57, P60 to P67,P76 to P77, P80 to P84, P86, P87, P90, P92 to P97, P100 to P107, XOUT		-0.3 to Vcc+0.3	V
		P70, P71		-0.3 to 4.6	V
Pd	Power dissipation		Ta=25 °C	300	mW
Topr	Operating ambient temperature			-20 to 85 / -40 to 85(Note)	°C
Tstg	Storage temperature			-65 to 150	°C

Note: Specify a product of -40 to 85°C to use it.

Table 1.20.2. Recommended operating conditions (referenced to Vcc = 2.2V to 3.6V at Ta = – 20°C to 85°C / – 40°C to 85°C(Note3) unless otherwise specified)

Symbol	Parameter			Standard Min.	Standard Typ.	Standard Max.	Unit
Vcc	Supply voltage			2.2	3.0	3.6	V
AVcc	Analog supply voltage				Vcc		V
Vss	Supply voltage				0		V
AVss	Analog supply voltage				0		V
V_{IH}	HIGH input voltage	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_6$, $P7_7$, $P8_0$ to $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, RESET, CNV_{SS} (BYTE)		0.8Vcc		Vcc	V
		$P7_0$, $P7_1$		0.8Vcc		4.6	V
V_{IL}	LOW input voltage	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$, $P8_0$ to $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, RESET, CNV_{SS} (BYTE)		0		0.2Vcc	V
$I_{OH (peak)}$	HIGH peak output current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_6$, $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$				–10.0	mA
$I_{OH (avg)}$	HIGH average output current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_6$, $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$				–5.0	mA
$I_{OL (peak)}$	LOW peak output current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$ $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL (avg)}$	LOW average output current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$ $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
f (X_{IN})	Main clock input oscillation frequency (Note 5)	No wait	Vcc=2.7V to 3.6V	0		10	MHz
			Vcc=2.4V to 2.7V	0		10 X Vcc –17	MHz
			Vcc=2.2V to 2.4V	0		17.5 X Vcc –35	MHz
		with wait	Vcc=2.7V to 3.6V	0		10	MHz
			Vcc=2.2V to 2.7V	0		6 X Vcc –6.2	MHz
f (X_{CIN})	Subclock oscillation frequency				32.768	50	kHz

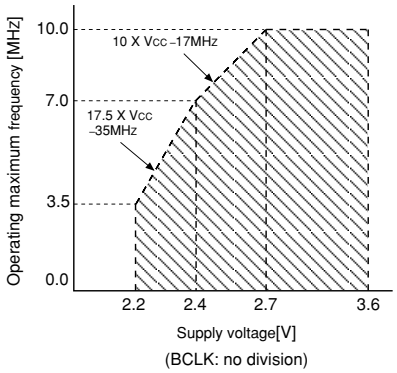
Note 1: The mean output current is the mean value within 100ms.

Note 2: The total I_{OL} (peak) for all ports must be 80mA max. The total I_{OH} (peak) for all ports must be 80mA max.

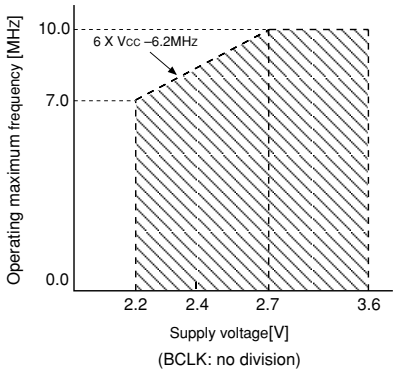
Note 3: Specify a product of –40°C to 85°C to use it.

Note 4: Relationship between main clock oscillation frequency and supply voltage.

Main clock input oscillation frequency (No wait)



Main clock input oscillation frequency (With wait)



Flash memory version program voltage and read operation voltage characteristics

Flash program voltage	Flash read operation voltage
Vcc=2.7V to 3.6V	Vcc=2.4V to 3.6V
Vcc=2.7V to 3.4V	Vcc=2.2V to 2.4V

Note 5: Execute case without wait, program / erase of flash memory by Vcc=2.7V to 3.6V and f(BCLK) ≤ 6.25 MHz.
Execute case with wait, program / erase of flash memory by Vcc=2.7V to 3.6V and f(BCLK) ≤ 10.0 MHz.

Vcc = 3V

Table 1.20.3. A-D conversion characteristics (referenced to Vcc = AVcc = VREF = 2.4V to 3.6V, Vss = AVss = 0V at Ta = – 20°C to 85°C / – 40°C to 85°C(Note2), f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Resolution	VREF = Vcc			10	Bits
–	Absolute accuracy, sample & hold function not available (8 bit)	VREF = Vcc = 3V, φAD = f(XIN)/2			±2	LSB
RLADDER	Ladder resistance	VREF = Vcc	10		40	kΩ
tCONV	Conversion time(8bit), sample & hold function not available	VREF = Vcc = 3V, φAD = f(XIN) =fAD/2 = 5MHz	9.8		Vcc	µs
tSAMP	Sampling time		0.3			µs
VREF	Reference voltage		2.4		Vcc	V
VIA	Analog input voltage		0		VREF	V

Note 1: Connect AVcc pin to Vcc pin and apply the same electric potential.
Note 2: Specify a product of -40°C to 85°C to use it.

Table 1.20.4. D-A conversion characteristics (referenced to Vcc = 2.4V to 3.6V, Vss = AVss = 0V, VREF = 3V, at Ta = – 20°C to 85°C / – 40°C to 85°C(Note2), f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note)			1.5	mA

Note 1: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "00$_{16}$".
The A-D converter's ladder resistance is not included.
Also, when DA register contents are not "00", the current I VREF always flows even though Vref may have been set to be unconnected by the A-D control register.
Note 2: Specify a product of -40°C to 85°C to use it.

Table 1.20.5. Flash memory version electrical characteristics (referenced to Vcc = 2.7V to 3.6V, at Ta =0°C to 60°C unless otherwise specified)

Parameter	Standard			Unit
	Min.	Typ.	Max	
Page program time		6	120	ms
Block erase time		50	600	ms
Erase all unlocked blocks time		50 X n (Note)	600 X n (Note)	ms
Lock bit program time		6	120	ms

Note : n denotes the number of block erases.

Table 1.20.6. Flash memory version program voltage and read operation voltage characteristics (Ta =0°C to 60°C)

Flash program voltage	Flash read operation voltage
Vcc=2.7V to 3.6V	Vcc=2.4V to 3.6V
Vcc=2.7V to 3.4V	Vcc=2.2V to 2.4V

VCC = 3V

Table 1.20.7. Electrical characteristics (referenced to VCC = 2.7V to 3.6V, VSS = 0V at Ta = – 20°C to 85°C / – 40°C to 85°C(Note 1), f(XIN) = 10MHz without wait unless otherwise specified)

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	HIGH output voltage	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_6$, $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$	I_{OH}=–1mA		2.5			V
V_{OH}	HIGH output voltage	X_{OUT} HIGHPOWER	I_{OH}=–0.1mA		2.5			V
		X_{OUT} LOWPOWER	I_{OH}=–50µA		2.5			
	HIGH output voltage	X_{COUT} HIGHPOWER	With no load applied			3.0		V
		X_{COUT} LOWPOWER	With no load applied			1.6		
V_{OL}	LOW output voltage	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$	I_{OL}=1mA				0.5	V
V_{OL}	LOW output voltage	X_{OUT} HIGHPOWER	I_{OL}=0.1mA				0.5	V
		X_{OUT} LOWPOWER	I_{OL}=50µA				0.5	
	LOW output voltage	X_{COUT} HIGHPOWER	With no load applied			0		V
		X_{COUT} LOWPOWER	With no load applied			0		
V_{T+}-V_{T-}	Hysteresis	$TA0_{IN}$, $TA3_{IN}$, $TA4_{IN}$, $TB0_{IN}$, $TB2_{IN}$ to $TB5_{IN}$, $\overline{INT_0}$ to $\overline{INT_2}$, $\overline{ADTRG}$, $\overline{CTS_0}$, $\overline{CTS_1}$ CLK_0, CLK_1, CLK_3, CLK_4, $TA3_{OUT}$, $TA4_{OUT}$, $\overline{NMI}$, $\overline{KI_0}$ to $\overline{KI_3}$, SIN_4, RxD_0 to RxD_2			0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		1.8	V
I_{IH}	HIGH input current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$, $P8_0$ to $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNVss (BYTE)	V_I=3V				4.0	µA
I_{IL}	LOW input current	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$, $P7_1$, $P7_6$, $P7_7$, $P8_0$ to $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNVss (BYTE)	V_I=0V				–4.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$ to $P0_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_6$, $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$ to $P9_7$, $P10_0$ to $P10_7$	V_I=0V		20	75	300	KΩ
R_{fXIN}	Feedback resistance X_{IN}					3.0		MΩ
R_{fXCIN}	Feedback resistance X_{CIN}					10.0		MΩ
V_{RAM}	RAM retention voltage		When clock is stopped		2.0			V
Icc	Power supply current	The output pins are open and other pins are VSS	Mask ROM version	f(X_{IN})=10MHz Square wave, no division		9.5	21.25	mA
			Flash memory 3V version	f(X_{IN})=10MHz Square wave, no division		12.0	21.25	mA
			Mask ROM version Flash memory 3V version	f(X_{CIN})=32kHz Square wave		45.0		µA
			Flash memory 3V version Program	f(X_{IN})=10MHz Square wave, division by 2		14.0		mA
			Flash memory 3V version Erase	f(X_{IN})=10MHz Square wave, division by 2		17.0		mA
			Mask ROM version Flash memory 3V version	f(X_{CIN})=32kHz When a WAIT instruction is executed. Oscillation capacity High (Note2)		2.8		µA
				f(X_{CIN})=32kHz When a WAIT instruction is executed. Oscillation capacity Low (Note2)		0.9		µA
				Ta=25°C when clock is stopped			1.0	µA
				Ta=85°C when clock is stopped			20.0	

Note 1: Specify a product of -40°C to 85°C to use it.
Note 2: With one timer operated using fC32.

VCC = 3V

Timing requirements (referenced to VCC = 3V, VSS = 0V at Ta = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)

* : Specify a product of -40°C to 85°C to use it.

Table 1.20.8. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

VCC = 3V

Timing requirements (referenced to VCC = 3V, VSS = 0V at Ta = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)

* : Specify a product of -40°C to 85°C to use it.

Table 1.20.9. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 1.20.10. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 1.20.11. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 1.20.12. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 1.20.13. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

VCC = 3V

Timing requirements (referenced to VCC = 3V, VSS = 0V at Ta = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)

* : Specify a product of -40°C to 85°C to use it.

Table 1.20.14. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	160		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	160		ns

Table 1.20.15. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 1.20.16. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 1.20.17. A-D trigger input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 1.20.18. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	50		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.20.19. External interrupt $\overline{INTi}$ inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

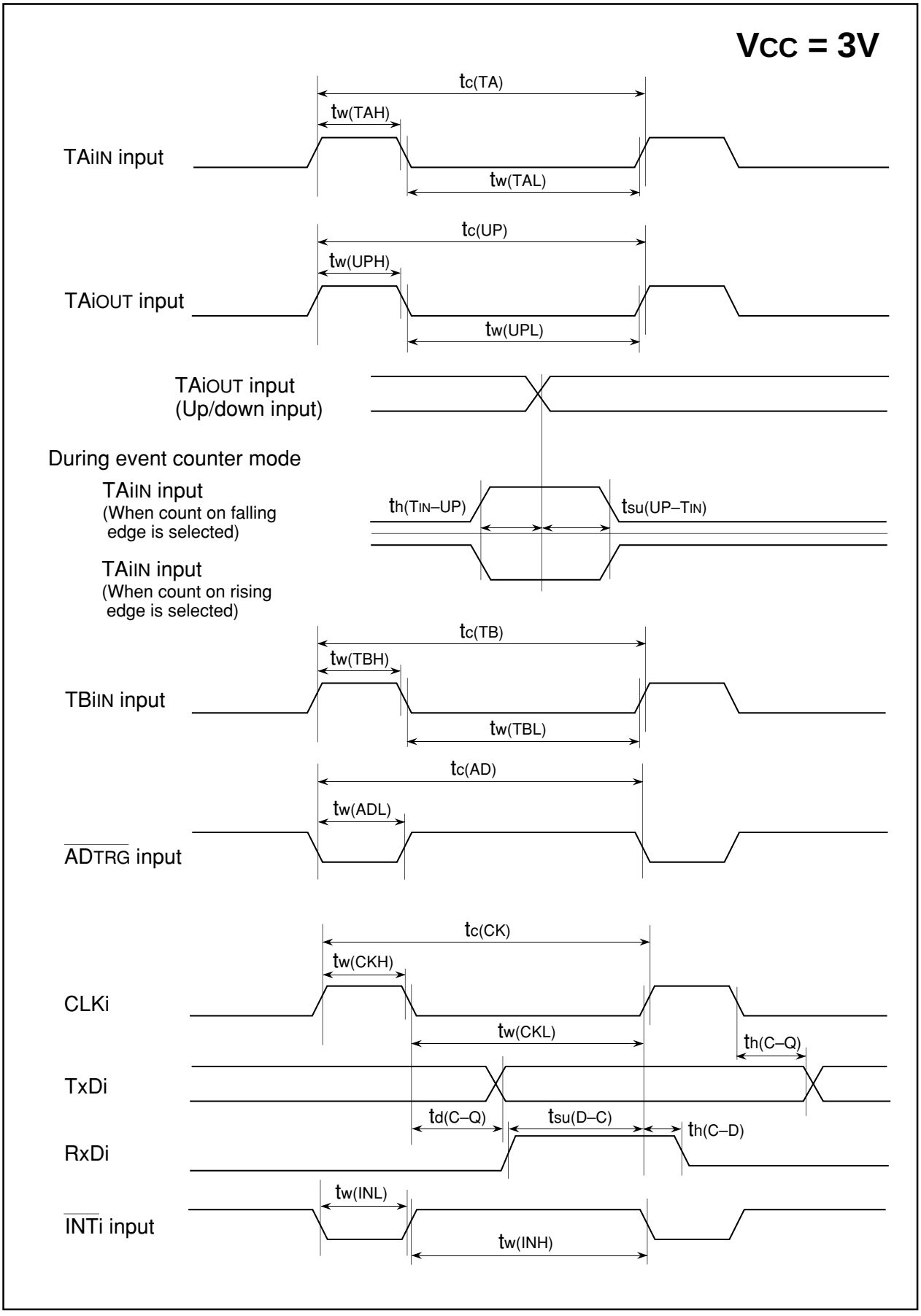


Figure 1.20.2. Vcc=3V timing diagram

Usage Precaution

Timer A (timer mode)

(1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF16". Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

Timer A (event counter mode)

(1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF16" by underflow or "000016" by overflow. Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

(2) When stop counting in free run type, set timer again.

Timer A (one-shot timer mode)

(1) Setting the count start flag to "0" while a count is in progress causes as follows:
- The counter stops counting and a content of reload register is reloaded.
- The TAiOUT pin outputs "L" level.
- The interrupt request generated and the timer Ai interrupt request bit goes to "1".

(2) The timer Ai interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
- Selecting one-shot timer mode after reset.
- Changing operation mode from timer mode to one-shot timer mode.
- Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

Timer A (pulse width modulation mode)

(1) The timer Ai interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
- Selecting PWM mode after reset.
- Changing operation mode from timer mode to PWM mode.
- Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

(2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TAiOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Ai interrupt request bit goes to "1". If the TAiOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Ai interrupt request bit does not becomes "1".

Timer B (timer mode, event counter mode)

(1) Reading the timer Bi register while a count is in progress allows reading , with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "FFFF16". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

Timer B (pulse period/pulse width measurement mode)

(1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to “1”.

(2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

A-D Converter

(1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).
In particular, when the Vref connection bit is changed from “0” to “1”, start A-D conversion after an elapse of 1 μs or longer.

(2) When changing A-D operation mode, select analog input pin again.

(3) Using one-shot mode or single sweep mode
Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)

(4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1
Use the undivided main clock as the internal CPU clock.

Stop Mode and Wait Mode

(1) When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to “L” level until main clock oscillation is stabilized.

(2) When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the every-clock stop bit to “1” within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the every-clock stop bit to “1”.

Interrupts

(1) Reading address 00000_{16}

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.
  The interrupt request bit of the certain interrupt written in address 00000_{16} will then be set to “0”.
  Reading address 00000_{16} by software sets enabled highest priority interrupt source request bit to “0”.
  Though the interrupt is generated, the interrupt routine may not be executed.
  Do not read address 00000_{16} by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000_{16}. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.
  When using the $\overline{\text{NMI}}$ interrupt, initialize the stack point at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the $\overline{\text{NMI}}$ interrupt is prohibited.

(3) The $\overline{\text{NMI}}$ interrupt

- The $\overline{\text{NMI}}$ interrupt can not be disabled. Be sure to connect $\overline{\text{NMI}}$ pin to Vcc via a pull-up resistor if unused.
- Do not get either into stop mode with the $\overline{\text{NMI}}$ pin set to “L”.

(4) External interrupt

• When the polarity of the $\overline{INT0}$ to $\overline{INT2}$ pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0".

(5) Rewrite the interrupt control register

• To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    NOP
    NOP
    FSET    I               ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    MOV.W   MEM, R0         ; Dummy read.
    FSET    I               ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
    PUSHC   FLG             ; Push Flag register onto stack
    FCLR    I               ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    POPC    FLG             ; Enable interrupts.
```

The reason why two NOP instructions or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

• When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.
Instructions : AND, OR, BCLR, BSET

Noise

(1) Insert bypass capacitor between V_{CC} and V_{SS} pin for noise and latch up countermeasure.

• Insert bypass capacitor (about 0.1 μF) and connect short and wide line between V_{CC} and V_{SS} lines.

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Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30621MCM-XXXGP MASK ROM CONFIRMATION FORM

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please complete all items marked ✵ .

					Issuance signature	Submitted by	Supervisor
✵	Customer	Company name	TEL ( )				
		Date issued	Date :				

✵1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.
Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. : ☐ M30621MCM-XXXGP

File code : ☐☐☐☐☐☐☐☐ (hex)

Mask file name : ☐☐☐☐☐☐☐☐ .MSK (alpha-numeric 8-digit)

✵2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30621MCM-XXXGP, submit the 80P6S mark specification sheet.

✵3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator
☐ External clock input ☐ Other ( )

What frequency do not use?

f(XIN) = ☐ MHz

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Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30621MCM-XXXGP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XCIN) = ☐ kHz

(3) Which operating supply voltage do you use?

(Circle the operating voltage range of use)

2.2 2.4 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 (V)

(4) Which operating ambient temperature do you use?

(Circle the operating temperature range of use)

-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90 (°C)

(5) Do you use I^2C (Inter IC) bus function?

☐ Not use ☐ Use

(6) Do you use IE (Inter Equipment) bus function?

☐ Not use ☐ Use

Thank you cooperation.

❋4. Special item (Indicate none if there is not specified item)

GZZ-SH13-49B<98A1>

Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30625MGM-XXXGP MASK ROM CONFIRMATION FORM

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	Section head signature	Supervisor signature

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				Issuance signature	Submitted by	Supervisor
✵	Customer	Company name	TEL ( )			
		Date issued	Date :			

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Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.
Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. : ☐ M30625MGM-XXXGP

File code : ☐☐☐☐☐☐☐☐ (hex)

Mask file name : ☐☐☐☐☐☐☐☐ .MSK (alpha-numeric 8-digit)

✵2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30625MGM-XXXGP, submit the 80P6S mark specification sheet.

✵3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XIN) = ☐ MHz

GZZ-SH13-49B<98A1>

Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30625MGM-XXXGP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XCIN) = ☐ kHz

(3) Which operating supply voltage do you use?

(Circle the operating voltage range of use)

2.2 2.4 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 (V)

(4) Which operating ambient temperature do you use?

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-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90 (°C)

(5) Do you use I^2C (Inter IC) bus function?

☐ Not use ☐ Use

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☐ Not use ☐ Use

Thank you cooperation.

❋4. Special item (Indicate none if there is not specified item)

REVISION HISTORY	M16C/62M(80-PIN VERSION) GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
A1	02/04/02	5	Figure 1.1.3 is revised. Table 1.1.2 is revised.

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

Printed in Japan (ROD) II
New publication, effective Apr. 2002.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC