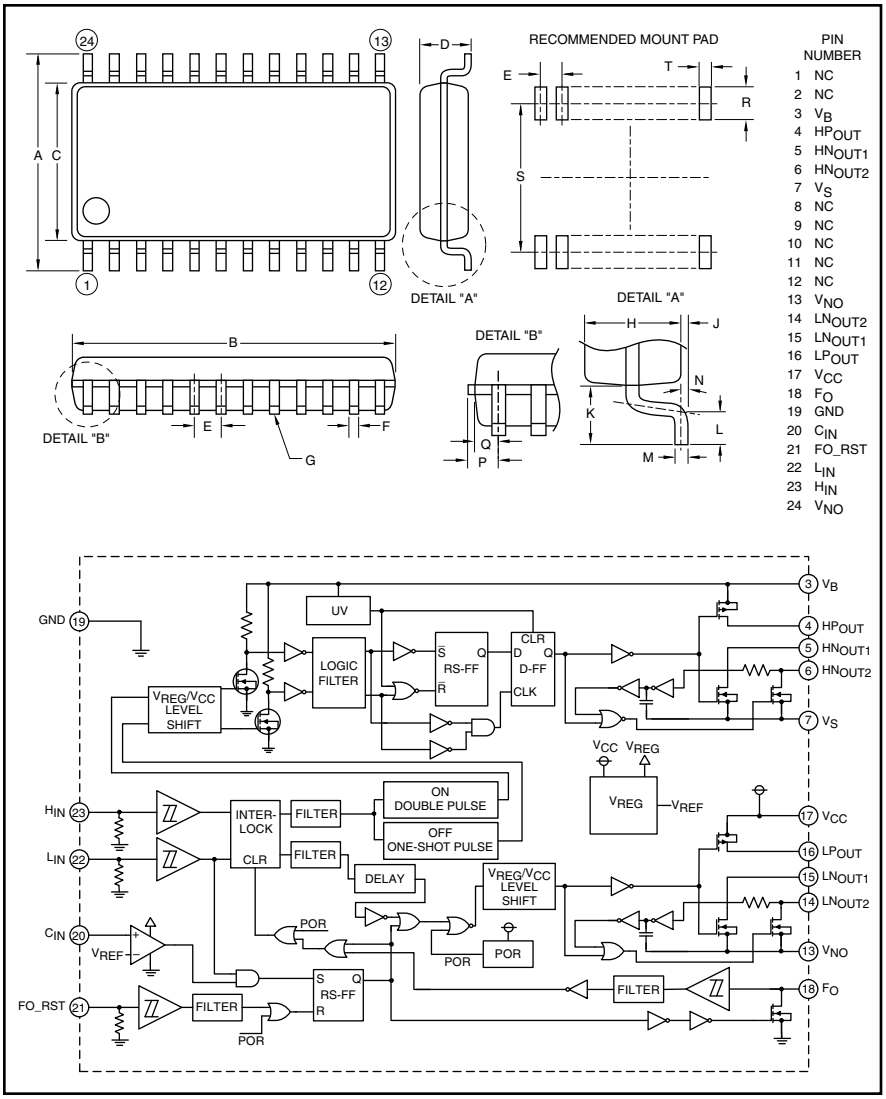
Powerex, Inc., 200 E. Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

HVIC

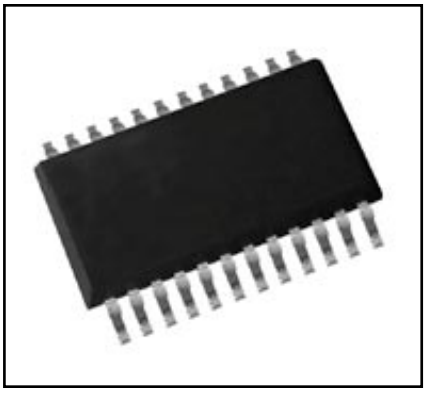
High Voltage Half-Bridge Driver 1200 Volts/±1 Ampere



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	0.31±0.01	7.8±0.3
B	0.40±0.004	10.1±0.1
C	0.21±0.004	5.3±0.1
D	0.08 Max.	2.1 Max.
E	0.03	0.8
F	0.01+0.004/0.002	0.35+0.1/-0.05
G	0.004	0.1
H	0.07	1.8
J	0.008 Max.	0.2 Max.

Dimensions	Inches	Millimeters
K	0.05	1.25
L	0.02±0.008	0.6±0.2
M	0.008+0.002/-0.008	0.2+0.05/-0.2
N	8° Max.	8° Max.
P	0.03 Max.	0.8 Max.
Q	0.026	0.65
R	0.051 Min.	1.27 Min.
S	0.30	7.62
T	0.02	0.5



Description:
M81019FP is a high voltage Power MOSFET and IGBT driver for half-bridge applications.

Features:
- ☐ Shoot Through Interlock
- ☐ Output Current ±1 Ampere
- ☐ Half-Bridge Driver
- ☐ 24-Lead SSOP Package
- ☐ Internal Dead Time - Fixed

Applications:
- ☐ HID Ballast
- ☐ PDP
- ☐ MOSFET Driver
- ☐ IGBT Driver
- ☐ Inverter Module Control

Ordering Information:
M81019FP is a ±1 Ampere, 1200 Volt HVIC, High Voltage Half-Bridge Driver

Absolute Maximum Ratings, T_a = 25°C unless otherwise specified

Characteristics	Symbol	M81019FP	Units
High Side Floating Supply Absolute Voltage	V_B	-0.5 ~ 1224	Volts
High Side Floating Supply Offset Voltage	V_S	V_B-24 ~ V_B+0.5	Volts
High Side Floating Supply Voltage ($V_{BS} = V_B - V_S$)	V_{BS}	-0.5 ~ 24	Volts
High Side Output Voltage	V_{HO}	V_S-0.5 ~ V_B+0.5	Volts
Low Side Fixed Supply Voltage	V_{CC}	-0.5 ~ 24	Volts
Power Ground	V_{NO}	V_{CC}-24 ~ VCC+0.5	Volts
Low Side Output Voltage	V_{LO}	V_{NO}-0.5 ~ V_{CC}+0.5	Volts
Logic Input Voltage (H_{IN}, L_{IN}, FO_RST)	V_{IN}	-0.5 ~ V_{CC}+0.5	Volts
F_O Input/Output Voltage	V_{FO}	-0.5 ~ V_{CC}+0.5	Volts
C_{IN} Input Voltage	V_{CIN}	-0.5 ~ V_{CC}+0.5	Volts
Allowable Offset Voltage Slew Rate	dVs/dt	±50	V/ns
Package Power Dissipation (T_a = 25°C, On Board)	P_d	~1.6	Watts
Linear Derating Factor (T_a > 25°C, On Board)	$K\theta$	~16	mW/°C
Junction to Case Thermal Resistance	$R_{th(j-c)}$	~60	°C/W
Junction Temperature	T_j	-20 ~ 150	°C
Operation Temperature	T_{opr}	-20 ~ 125	°C
Storage Temperature	T_{stg}	-40 ~ 150	°C

Recommended Operating Conditions
All voltage parameters are absolute voltages referenced to GND unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Floating Supply Absolute Voltage	V_B		V_S+13.5	V_S+15	V_S+20	Volts
High Side Floating Supply Offset Voltage	V_S	V_{BS} > 10V	-5*	—	900**	Volts
High Side Floating Supply Voltage	V_{BS}	$V_B = V_B - V_S$	13.5	15	20	Volts
High Side Output Voltage	V_{HO}		V_S	—	V_S+20	Volts
Low Side Fixed Supply Voltage	V_{CC}		13.5	—	20	Volts
Power Ground	V_{NO}		-5	—	5	Volts
Low Side Output Voltage	V_{LO}		V_{NO}	—	V_{CC}	Volts
Logic Input Voltage	V_{IN}	H_{IN}, L_{IN}, FO_RST	—	5	V_{CC}	Volts
F_O Input/Output Voltage	V_{FO}		—	—	V_{CC}	Volts
C_{IN} Input Voltag	V_{CIN}		—	—	5	Volts
Allowable Offset Voltage Slew Rate***	dVs/dt		-8	—	8	KV/µs

*The lowest logic operational condition for V_S is -5V. The lowest state held condition for V_S is -V_{BS}. The surge of -V_S should not exceed -100V to avoid improper operation of output.
**The maximum of allowable instantaneous voltage spike is up to 1200V.
***At operation mode, dVs/dt should not go beyond recommended operation conditions or it will cause improper operation output.

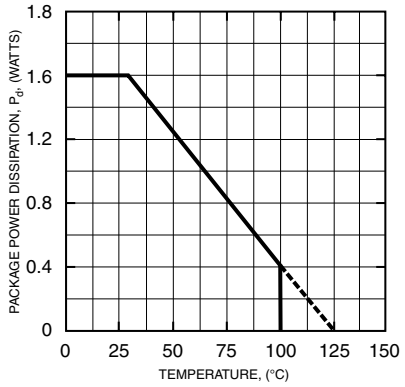
Electrical Characteristics, T_a = 25°C, V_{CC} = V_{BS} (= V_B – V_S) = 15V unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Leakage Current	I_{FS}	$V_B = V_S$ = 1200V	—	—	1.0	µA
V_{BS} Quiescent Supply Current	I_{BS}	$H_{IN} = L_{IN}$ = 0V	—	0.4	0.8	mA
V_{CC} Quiescent Supply Current	I_{CC}	$H_{IN} = L_{IN}$ = 0V	—	0.9	1.5	mA
High Level Output Voltage	V_{OH}	I_O = -20mA, H_{POUT}, L_{POUT}	14.5	—	—	Volts
Low Level Output Voltage	V_{OL}	I_O = 20mA, H_{NOUT1}, L_{NOUT1}	—	—	0.5	Volts
High Level Input Threshold Voltage	V_{IH}	H_{IN}, L_{IN}, FO_RST	3.0	—	—	Volts
Low Level Input Threshold Voltage	V_{IL}	H_{IN}, L_{IN}, FO_RST	—	—	1.5	Volts
High Level Input Bias Current	I_{IH}	V_{IN} = 5V	—	1.0	1.4	mA
Low Level Input Bias Current	I_{IL}	V_{IN} = 0V	-1.0	—	—	µA
Input Signals Filter Time	t_{Filter}	H_{IN}, L_{IN}, FO_RST, F_O	100	200	400	ns
High Side Low Impedance NMOS Input Threshold Voltage	V_{HNO2}	V_{IN} = 0V	2.5	3.4	5.0	Volts
Low Side Low Impedance NMOS Input Threshold Voltage	V_{LNO2}	V_{IN} = 0V	6.5	7.6	9.0	Volts
Low Impedance NMOS Filter Time	t_{VNO2}	V_{IN} = 0V	200	400	650	ns
Low Level F_O Output Voltage	V_{OLFO}	I_{FO} = 1mA	—	—	0.95	Volts
High Level F_O Input Threshold Voltage	V_{IHFO}	—	3.0	—	—	Volts
Low Level F_O Input Threshold Voltage	V_{ILFO}	—	—	—	1.5	Volts
V_{BS} Supply UV Reset Voltage	V_{BSuvr}	—	10.5	11.3	12.1	Volts
V_{BS} Supply UV Trip Voltage	V_{BSuvt}	—	10.0	10.8	11.6	Volts
V_{BS} Supply UV Hysteresis Voltage	V_{BSuvh}	$V_{BSuvh} = V_{BSuvr} – V_{BSuvt}$	0.3	0.5	0.8	Volts
V_{BS} Supply UV Filter Time	tV_{BSuv}	—	4.0	8.0	16.0	µs
C_{IN} Trip Voltage	V_{CIN}	—	0.4	0.5	0.6	Volts
POR Trip Voltage	V_{POR}	—	4.5	5.5	7.0	Volts
Output High Level Short Circuit Pulsed Current	I_{OH}	$H_{POUT(LPOUT)}$ = 0V, H_{IN} = 5V, P_W < 5µs	—	1.0	—	A
Output Low Level Short Circuit Pulsed Current	I_{OL1}	$H_{NOUT1(LNOUT1)}$ = 15V, L_{IN} = 5V, P_W < 5µs	—	-1.0	—	A
Low Impedance NMOS Output Low Level Short Circuit Pulsed Current	I_{OL2}	$H_{NOUT2(LNOUT2)}$ = 15V, L_{IN} = 5V, P_W < 5µs	—	-1.0	—	A
Output High Level ON Resistance	R_{OH}	I_O = -200mA, $R_{OH} = (V_{OH} – V_O)/I_O$	—	15	—	Ω
Output Low Level ON Resistance	R_{OL1}	I_O = 200mA, $R_{OL1} = V_O / I_O$	—	15	—	Ω
Low Impedance NMOS Output Low Level ON Resistance	R_{OL2}	I_O = 200mA, $R_{OL2} = V_O / I_O$	—	15	—	Ω

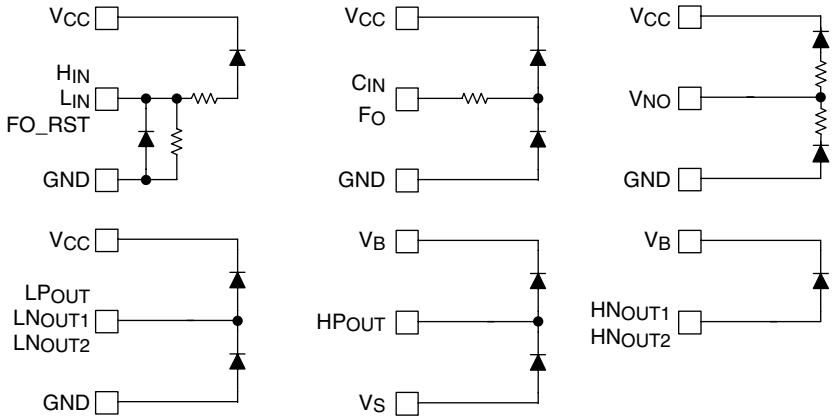
Electrical Characteristics, T_a = 25°C, V_{CC} = V_{BS} (= V_B – V_S) = 15V unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Turn-On Propagation Delay	$t_{dLH(HO)}$	H_{POUT} Short to H_{NOUT1} & H_{NOUT2}, C_L = 1nF	1.0	1.29	1.6	µs
High Side Turn-Off Propagation Delay	$t_{dHL(HO)}$	H_{POUT} Short to H_{NOUT1} & H_{NOUT2}, C_L = 1nF	0.9	1.19	1.5	µs
Low Side Turn-On Propagation Delay	$t_{dLH(LO)}$	L_{POUT} Short to L_{NOUT1} & L_{NOUT2}, C_L = 1nF	1.0	1.27	1.6	µs
Low Side Turn-Off Propagation Delay	$t_{dHL(LO)}$	L_{POUT} Short to L_{NOUT1} & L_{NOUT2}, C_L = 1nF	0.9	1.21	1.5	µs
Output Turn-On Rise Time	t_r	C_L = 1nF	—	40.0	—	ns
Ouyput Turn-Off Fall Time	t_f	C_L = 1nF	—	40.0	—	ns
Delay Matching, High Side Turn-On & Low Side Turn-Off	$\angle t_{dLH}$	$t_{dLH(HO)} - t_{dLH(LO)}$	—	80.0	—	ns
Delay Matching, High Side Turn-Off & Low Side Turn-On	$\angle t_{dHL}$	$t_{dHL(HO)} - t_{dHL(LO)}$	—	80.0	—	ns

THERMAL DERATING FACTOR CHARACTERISTICS



DIODE CLAMP CIRCUITS FOR INPUT AND OUTPUT PINS



FUNCTION TABLE (X = H or L; Z = High Impedance; Q = Keep Previous Status)

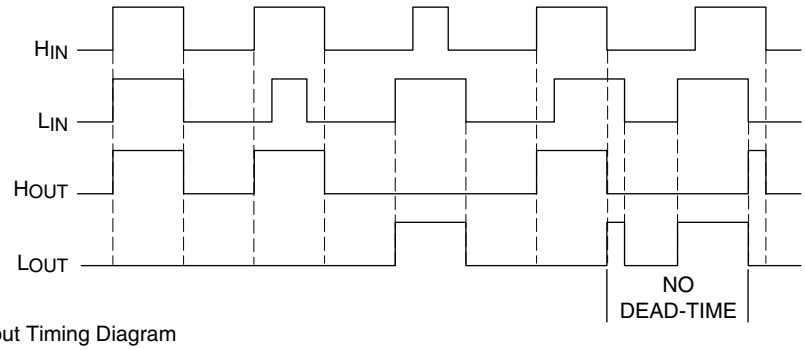
H_{IN}	L_{IN}	FO_RST	C_{IN}	FO (Input)	V_{BS}/U_V	$V_{CC/POR}$	HO	LO	FO (Output)	Behavorial State
L	L	L	L	–	H	H	L	L	H	
L	H	L	L	–	H	H	L	H	H	
H	L	L	L	–	H	H	H	L	H	
H	H	L	L	–	H	H	Q	Q	H	For Interlock
X	H	X	H	–	X	H	L	L	L	C_{IN} Tripped When L_{IN} = H
X	L	X	H	–	X	H	Q	Q	H	C_{IN} Not Tripped When L_{IN} = L
X	X	X	X	L	X	H	L	L	L	Output Shut Down When FO = L
X	X	X	X	–	X	L	L	L	H	V_{CC} Power Reset Tripped
X	L	L	L	–	L	H	L	L	H	V_{BS} Power Reset Tripped
X	H	L	L	–	L	H	L	H	H	V_{BS} Power Reset Tripped When L_{IN} = H

NOTE: "L" status of V_{BS}/U_V indicates high side UV tripped.
"L" status of V_{CC}/POR indicates V_{CC} power reset tripped.

TIMING DIAGRAM

1. Input Interlock Timing Diagram

When the input signals (H_{IN}/L_{IN}) are high at the same time, the output (H_{OUT}/L_{OUT}) will maintain previous status. But if the input signals (H_{IN}/L_{IN}) go high simultaneously, H_{IN} signals would be active and cause H_{OUT} to enter into high status.



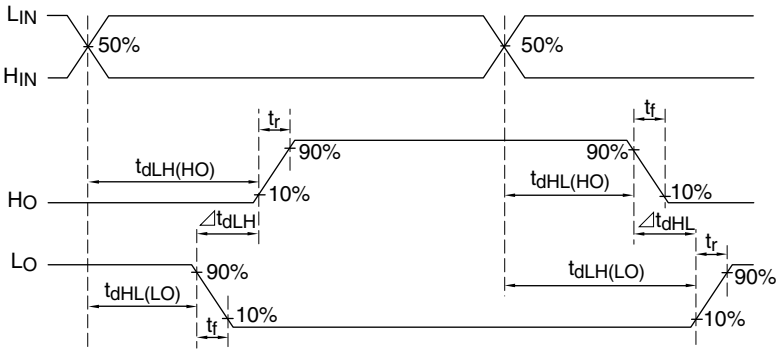
NOTE 1: Input pulse width should be set to more than 200ns for H_{IN}/L_{IN} input filter circuit.

NOTE 2: If high-high status of input signals H_{IN}/L_{IN} completes with one input signal in low level and the other in high level, the output will enter into high-low status without dead time.

NOTE 3: This diagram does not show delay time between input and output.

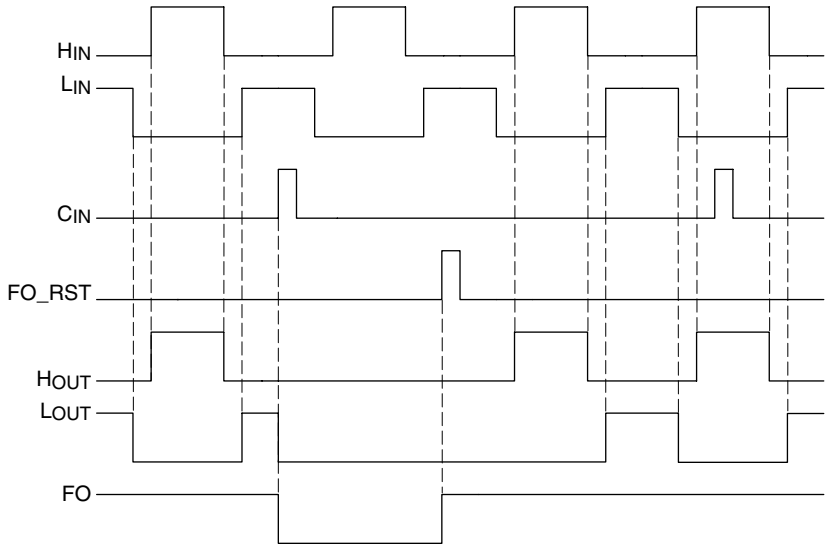
2. Input/Output Timing Diagram

The M81019FP matches delay between the low side and high side driver allowing minimized dead time control for better speed range and torque control in motor drive applications.



3. Short Circuit Protection Timing Diagram

When overcurrent is detected, C_{IN} will be tripped if L_{IN} is high; then the short circuit protection will activate and shut down the outputs and F_O will indicate fault by going low. As soon as FO_RST is driven high, short circuit protection will deactivate and F_O goes high. The output will then respond to any subsequent active input signal.

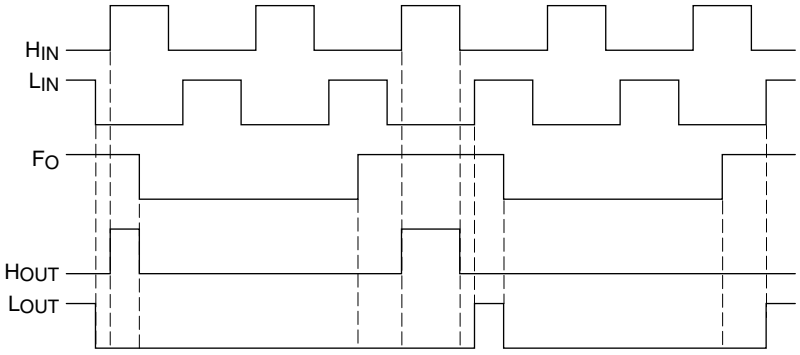


NOTE 1: This diagram does not show delay time between input and output.

NOTE 2: FO_RST pulse width should be set to more than 400ns for FO_RST input filter circuit.

4. F_O Input Timing Diagram

When F_O is pulled low by an enternal signal, the output will be shut down. As soon as F_O goes high again, the output will respond to the next active input signal.

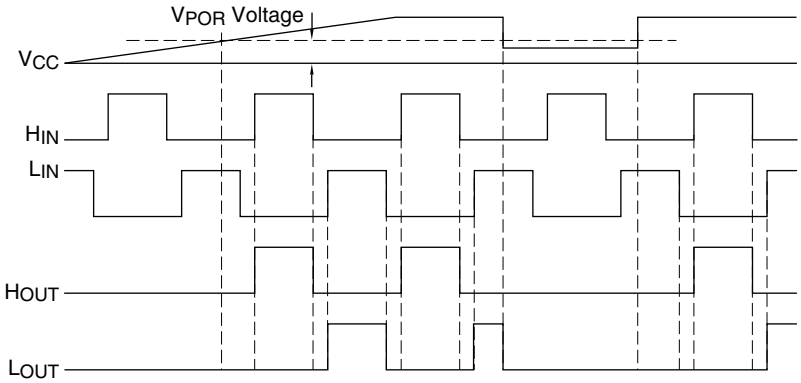


NOTE 1: This diagram does not show delay time between input and output.

NOTE 2: F_O pulse width should be set to more than 400ns for F_O input filter circuit.

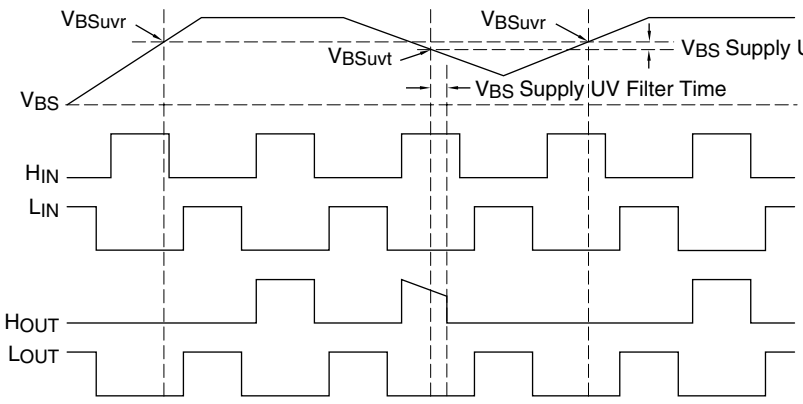
5. Low Side V_{CC} Supply Power Reset Sequence

When V_{CC} supply voltage is lower than power reset trip voltage, the power reset trips and output is locked out. As soon as V_{CC} supply voltage does higher than power reset trip voltage, the output will respond to the next active input signal.



6. High-Side V_{BS} Supply Under Voltage Lockout Sequence

When V_{BS} supply voltage goes lower than V_{BS} supply UV trip voltage for a period than the V_{BS} supply UV filter time, H_{OUT} goes low regardles of H_{IN}. As soon as V_{BS} supply voltage goes higher than V_{BS} supply reset voltage, the output will respond to the next active H_{IN} signal.



NOTE 1: This diagram does not show delay time between input and output.

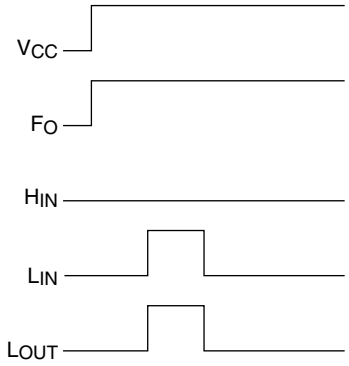
NOTE 2: At power supply start-up it is recommended that dV_{BS}/dt should be controlled to avoid H latch of outputs.

7. Power Start-Up Sequence

At power supply start-up the following sequence is recommended when bootstrap supply topology is used.

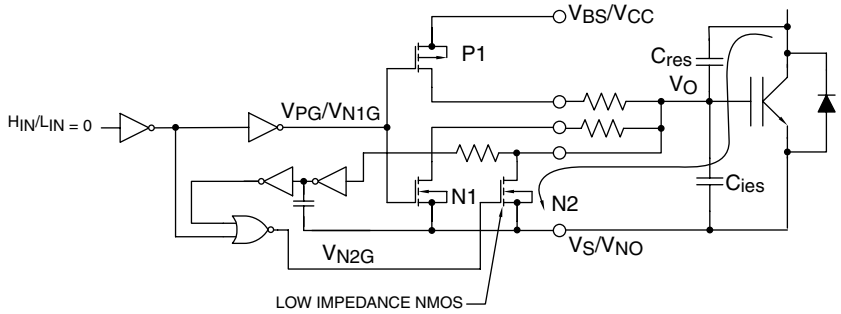
1. Set V_{CC}.
2. Make sure F_O is in high level.
3. Set L_{IN} to high level and set H_{IN} to low level so that bootstrap capacitor will charge.
4. Set L_{IN} to low level.

NOTE: If two power supplies are used to supply V_{CC} and V_{BS} individually, it is recommended to set V_{CC} first, then set V_{BS}.

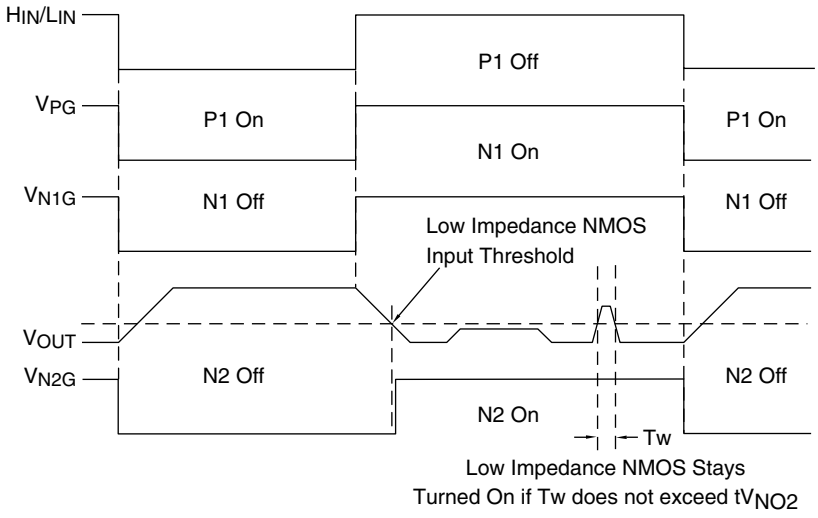


8. Low Impedance NMOS Output Timing Diagram

Output configuration is shown in the following figure. At turn-off an n-channel NMOS with sink current up to 1A is used to offer a low impedance path (AKA “low impedance NMOS) to prevent the power switch from turning itself on because of the parasitic Miller capacitor in the power switch.



When H_{IN}/L_{IN} is low level and V_{OUT} voltage is lower than low impedance NMOS input threshold voltage, the low impedance NMOS continues to discharge the parasitic current through C_{res}.



Low Impedance NMOS Stays
Turned On if Tw does not exceed tV_{NO2}