HARRIS Semiconductor

MCTV35P60F1D

PART WITHDRAWN
PROCESS OBSOLETE - NO NEW DESIGNS

April 1999

35A, 600V P-Type MOS Controlled Thyristor (MCT) with Anti-Parallel Diode

Features

- **35A, -600V**
- **V_{TM} = -1.35V (Max) at I = 35A and +150°C**
- **800A Surge Current Capability**
- **800A/μs di/dt Capability**
- **MOS Insulated Gate Control**
- **50A Gate Turn-Off Capability at +150°C**
- **Anti-Parallel Diode**

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications. The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150°C with active switching. This device features a discrete anti-parallel diode that shunts current around the MCT in the reverse direction without introducing carriers into the depletion region.

PART NUMBER INFORMATION

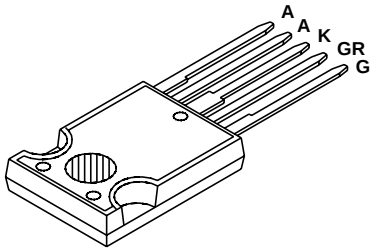
PART NUMBER	PACKAGE	BRAND
MCTV35P60F1D	TO-247	M35P60F1D

NOTE: When ordering, use the entire part number.

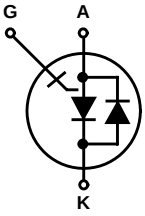
Formerly developmental type TA9789 (MCT) and TA49054 (diode).

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MCTV35P60F1D	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-600	V
Continuous Cathode Current (See Figure 2)			
T_C = +25°C (Package Limited)	I_{K25}	60	A
T_C = +90°C	I_{K115}	35	A
Non-repetitive Peak Cathode Current (Note 1)	I_{KSM}	800	A
Peak Controllable Current (See Figure 10)	I_{KC}	50	A
Gate-Anode Voltage (Continuous)	V_{GA1}	±20	V
Gate-Anode Voltage (Peak)	V_{GAM}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	800	A/μs
Maximum Power Dissipation	P_T	178	W
Linear Derating Factor		1.43	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	°C

NOTE: 1. Maximum Pulse Width of 250μs (Half Sine) Assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3694.4**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -600V	T_C = +150°C	-	-	5	mA
		V_{GA} = +18V	T_C = +25°C	-	-	200	µA
On-State Voltage	V_{TM}	$I_K = I_{K115}$	T_C = +150°C	-	-	1.35	V
		V_{GA} = -7V	T_C = +25°C	-	-	1.4	V
Gate-Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		-	-	100	nA
Input Capacitance	C_{ISS}	V_{KA} = -20V, T_J = +25°C V_{GA} = +18V		-	5	-	nF
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 200µH, $I_K = I_{K115}$ R_G = 1Ω, V_{GA} = +18V, -7V T_J = +125°C V_{KA} = -300V		-	140	-	ns
Current Rise Time	t_{RI}			-	180	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	640	-	ns
Current Fall Time	t_{FI}			-	1.1	1.4	µs
Turn-Off Energy	E_{OFF}			-	5.6	-	mJ
Thermal Resistance (MCT)	$R_{\theta JC}$			-	.6	.7	°C/W
Thermal Resistance (Diode)	$R_{\theta JC}$			-	1.1	1.2	°C/W
Diode Forward Voltage	V_{KA}	I_{KA} = 35A		-	-	1.4	V
Diode Reverse Recovery Time	t_{RR}	I_{KA} = 35A, di/dt = 100A/µs		-	-	600	ns

Typical Performance Curves

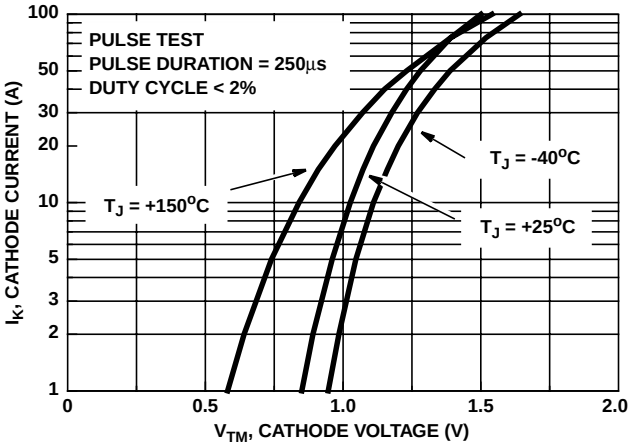


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

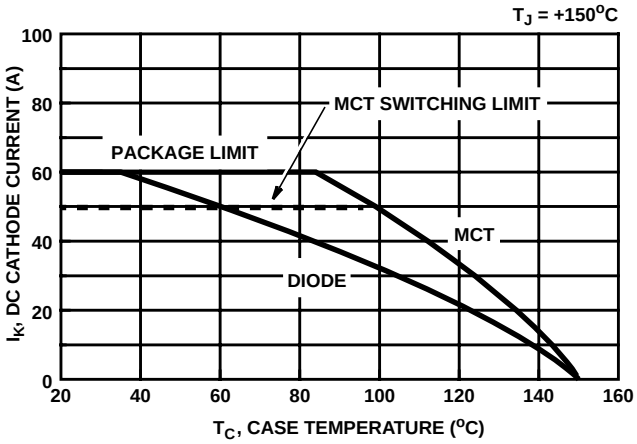


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

Typical Performance Curves (Continued)

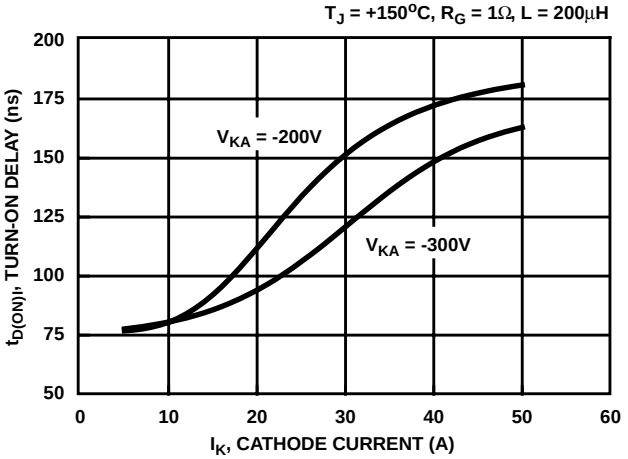


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

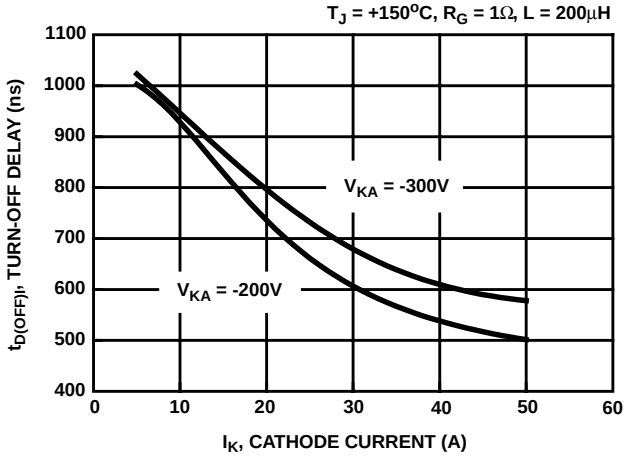


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

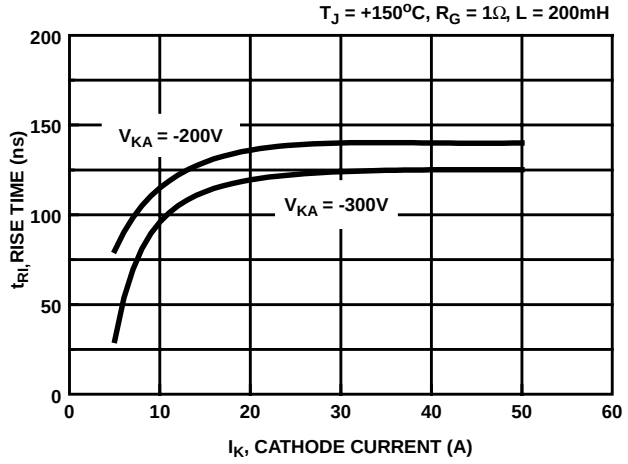


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

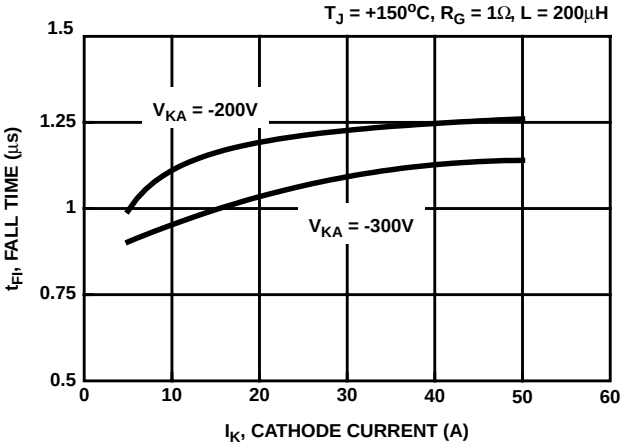


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

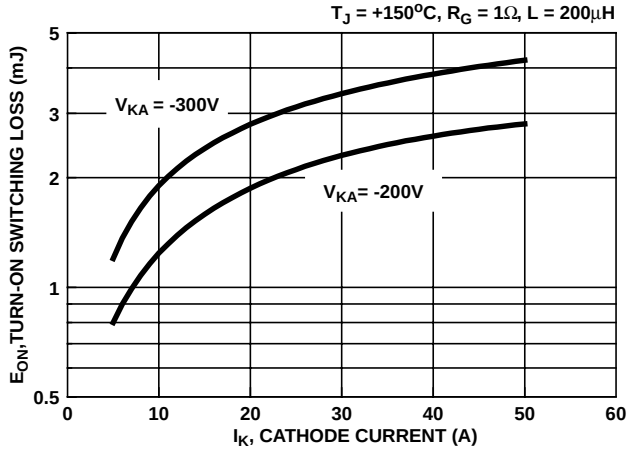


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

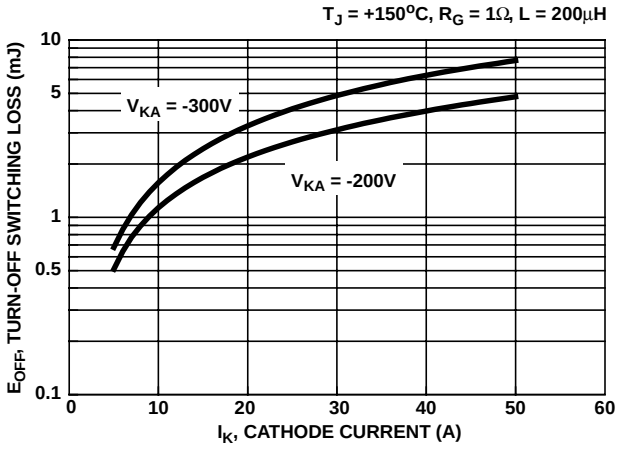


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

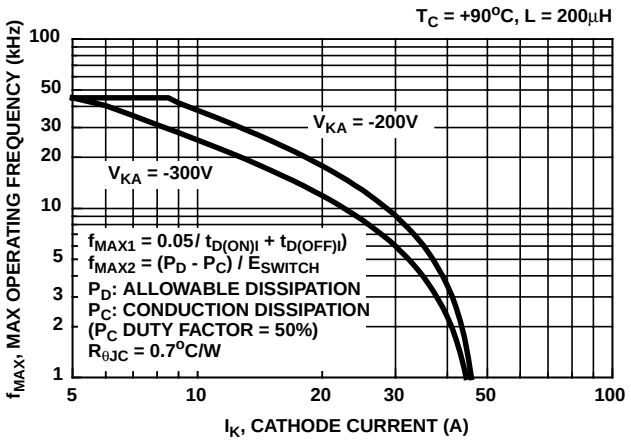


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

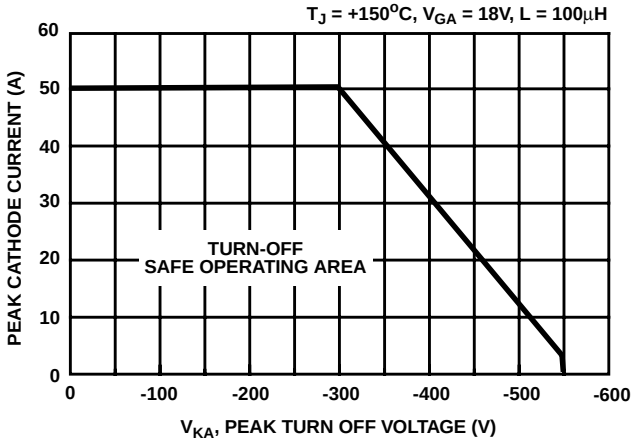


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

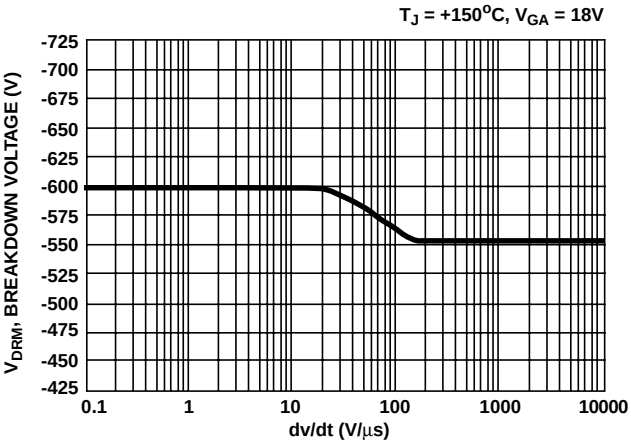


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

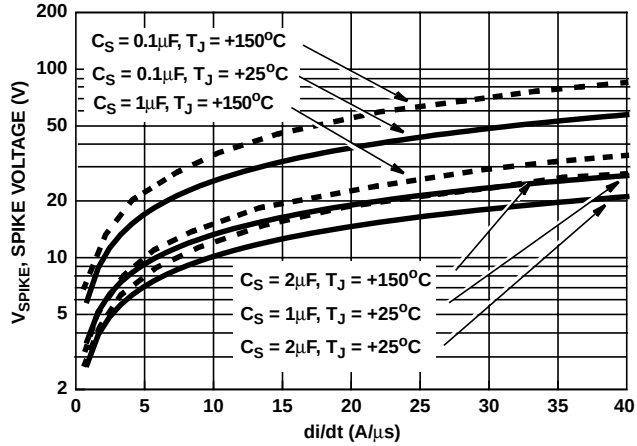


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

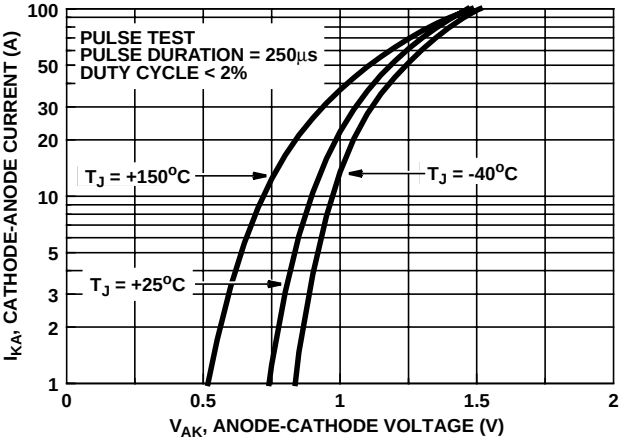


FIGURE 13. DIODE CATHODE-ANODE CURRENT vs VOLTAGE (TYPICAL)

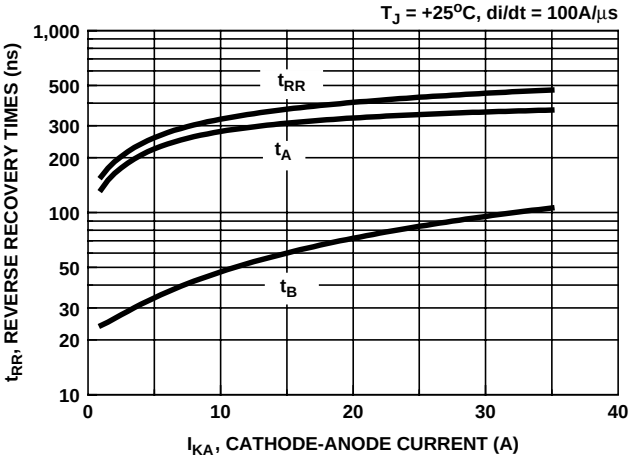


FIGURE 14. DIODE REVERSE RECOVERY TIMES vs CURRENT (TYPICAL)

Test Circuits

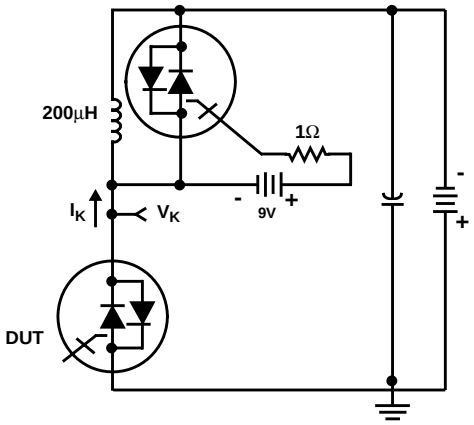


FIGURE 15. SWITCHING TEST CIRCUIT

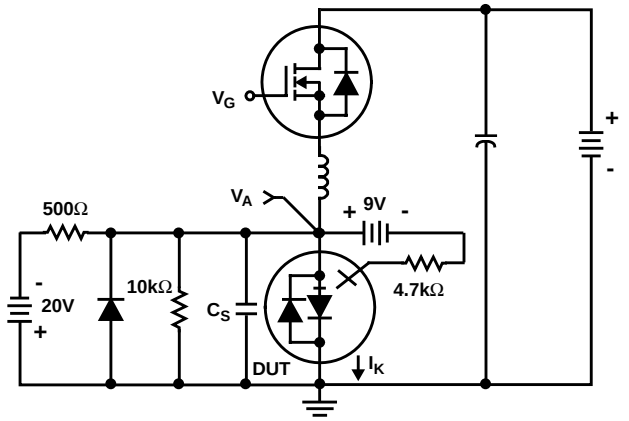


FIGURE 16. V_{SPIKE} TEST CIRCUIT

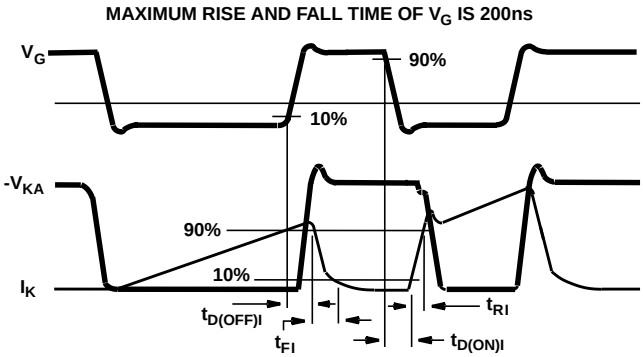


FIGURE 17. SWITCHING TEST WAVEFORMS

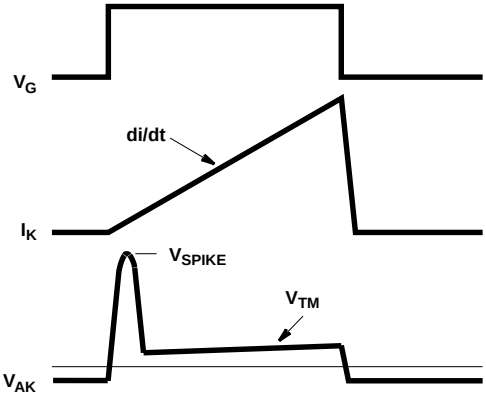


FIGURE 18. V_{SPIKE} TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is lower at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON}+E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 9) and the conduction losses (P_C) are approximated by $P_C = (V_{AK} \bullet I_{AK})$ / (duty factor/100). E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{AK} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).