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NTE67 MOSFET N-Ch, Enhancement Mode High Speed Switch

Description:

The NTE67 is a TMOS Power FET in a TO220 type package designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

Features:

- Lower $R_{DS(ON)}$
- Improved Inductive Ruggedness
- Fast Switching Times
- Lower Input Capacitance
- Extended Safe Operating Area
- Improved High Temperature Reliability

Absolute Maximum Ratings:

Drain–Source Voltage ($T_J = +25^{\circ}C$ to $+150^{\circ}C$), V_{DSS}	400V
Drain–Gate Voltage ($R_{GS} = 1M\Omega$, $T_J = +25^{\circ}C$ to $+125^{\circ}C$), V_{DGR}	400V
Gate–Source Voltage, V_{GS}	$\pm 20V$
Continuous Drain Current, I_D	
$T_C = +25^{\circ}C$	4.5A
$T_C = +100^{\circ}C$	3.0A
Pulsed Drain Current (Note 2), I_{DM}	18A
Pulsed Gate Current, I_{GM}	$\pm 1.5A$
Single Pulsed Avalanche Energy (Note 3), E_{AS}	290mJ
Avalanche Current, I_{AS}	5.5A
Total Power Dissipation ($T_C = +25^{\circ}C$), P_D	75W
Derate Above $25^{\circ}C$	0.6W/ $^{\circ}C$
Operating Junction Temperature Range, T_J	-55° to $+150^{\circ}C$
Storage Temperature Range, T_{stg}	-55° to $+150^{\circ}C$
Lead Temperature (During Soldering, 1/8" from case, 5sec max.), T_L	$+300^{\circ}C$
Thermal Resistance, Junction–to–Case, R_{thJC}	1.67K/W
Thermal Resistance, Junction–to–Ambient, R_{thJA}	80K/W
Thermal Resistance, Case–to–Sink (Mounting surface flat, smooth, and greased), R_{thCS}	0.24K/W

Note 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Note 2. Repetitive rating: Pulse width limited by max, junction temperature.

Note 3. $L = 17mH$, $V_{dd} = 50V$, $R_G = 25\Omega$, Starting $T_J = +25^{\circ}C$.

Electrical Characteristics: ($T_C = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	400	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	–	4.0	V
Gate–Source Leakage, Forward	I_{GSS}	$V_{GS} = 20V$	–	–	100	nA
Gate–Source Leakage, Reverse	I_{GSS}	$V_{GS} = -20V$	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$	–	–	250	μA
		$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0V, T_C = +125^\circ\text{C}$	–	–	1000	μA
On–State Drain–Source Current	$I_{D(on)}$	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{max}, V_{GS} = 10V, \text{Note 1}$	4.5	–	–	A
Static Drain–Source On–State Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3A, \text{Note 1}$	–	1.0	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} \geq 50V, I_D = 3A, \text{Note 1}$	2.9	4.4	–	mhos
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$	–	780	–	pF
Output Capacitance	C_{oss}		–	99	–	pF
Reverse Transfer Capacitance	C_{rss}		–	43	–	pF
Turn–On Delay Time	$t_{d(on)}$	$V_{DD} = 0.5BV_{DSS}, I_D = 5.5A, Z_O = 12\Omega$ (MOSFET switching times are essentially independent of operating temperature)	–	11	17	ns
Rise Time	t_r		–	19	29	ns
Turn–Off Delay Time	$t_{d(off)}$		–	37	56	ns
Fall Time	t_f		–	16	24	ns
Total Gate Charge (Gate–Source Plus Gate–Drain)	Q_g	$V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)	–	18	30	nC
Gate–Source Charge	Q_{gs}		–	40	–	nC
Gate–Drain (“Miller”) Charge	Q_{gd}		–	14	–	nC

Note 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Source–Drain Diode Ratings and Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Continuous Source Current (Body Diode)	I_S		–	–	4.5	A
Pulse Source Current (Body Diode)	I_{SM}	Note 2	–	–	18	A
Diode Forward Voltage	V_{SD}	$T_C = +25^\circ\text{C}, I_S = 4.5A, V_{GS} = 0V$	–	–	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = +25^\circ\text{C}, I_F = 5.5A, di_F/dt = 100A/\mu s$	–	310	660	ns

Note 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Note 2. Repetitive rating: Pulse width limited by max, junction temperature.

