2M x 16Bit x 4 Banks synchronous DRAM

GENERAL DESCRIPTION

The TTS3816B4E is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 8 x 1,048,576 words by 16 bits, fabricated with M'tec high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

• JEDEC standard 3.3V power supply

• LVTTL compatible with multiplexed address

• Four-banks operation

• MRS cycle with address key programs

  -. CAS latency (2 & 3)

  -. Burst length (1, 2, 4, 8 & Full page)

  -. Burst type (Sequential & Interleave)

• All inputs are sampled at the positive going edge of the system clock.

• Burst read single-bit write operation

• DQM for masking

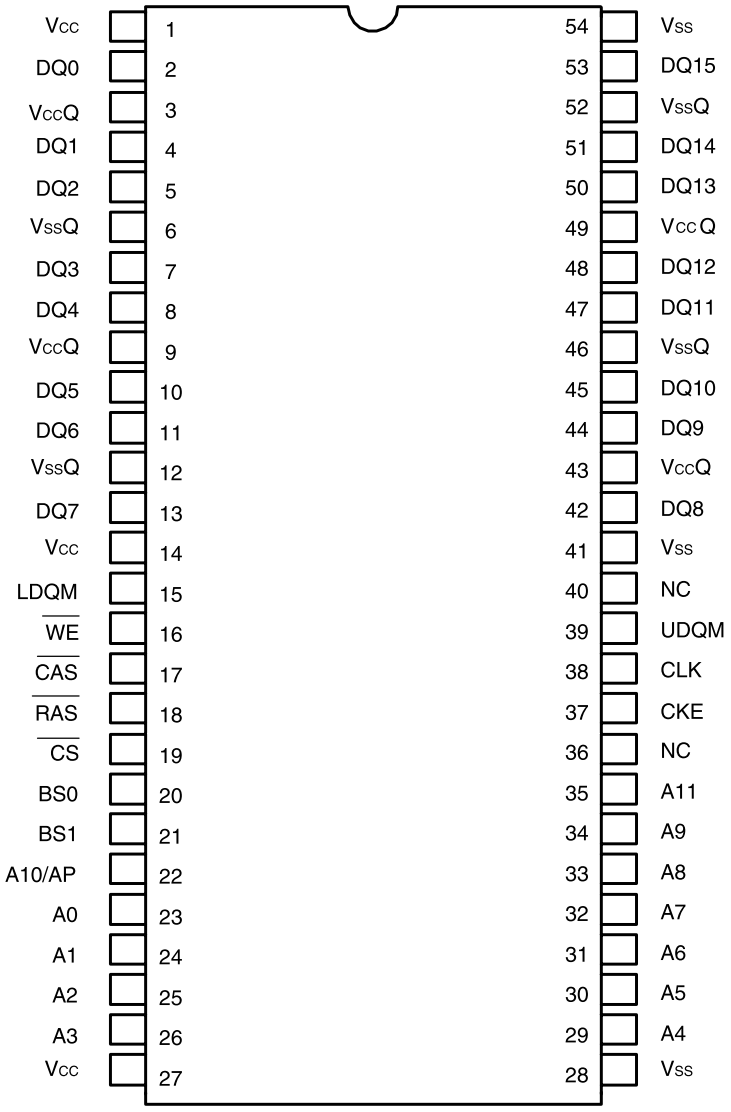
• Auto & self refresh

• 64ms refresh period (4K cycle)

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
TTS3816B4E-7	100MHz 2-2-2	LVTTL	54 TSOP(II)
TTS3816B4E-6	133MHz 3-3-3		
TTS3816B4E-6A	100MHz 2-3-3		
TTS3816B4E-6B	133MHz 2-3-2		
TTS3816B4E-6C	133MHz 2-2-2		
TTS3816B4E-6D	150MHz 3-3-3		
TTS3816B4E-6E	166MHz 3-3-3		

PIN CONFIGURATION (Top View)



54Pin TSOP (II)

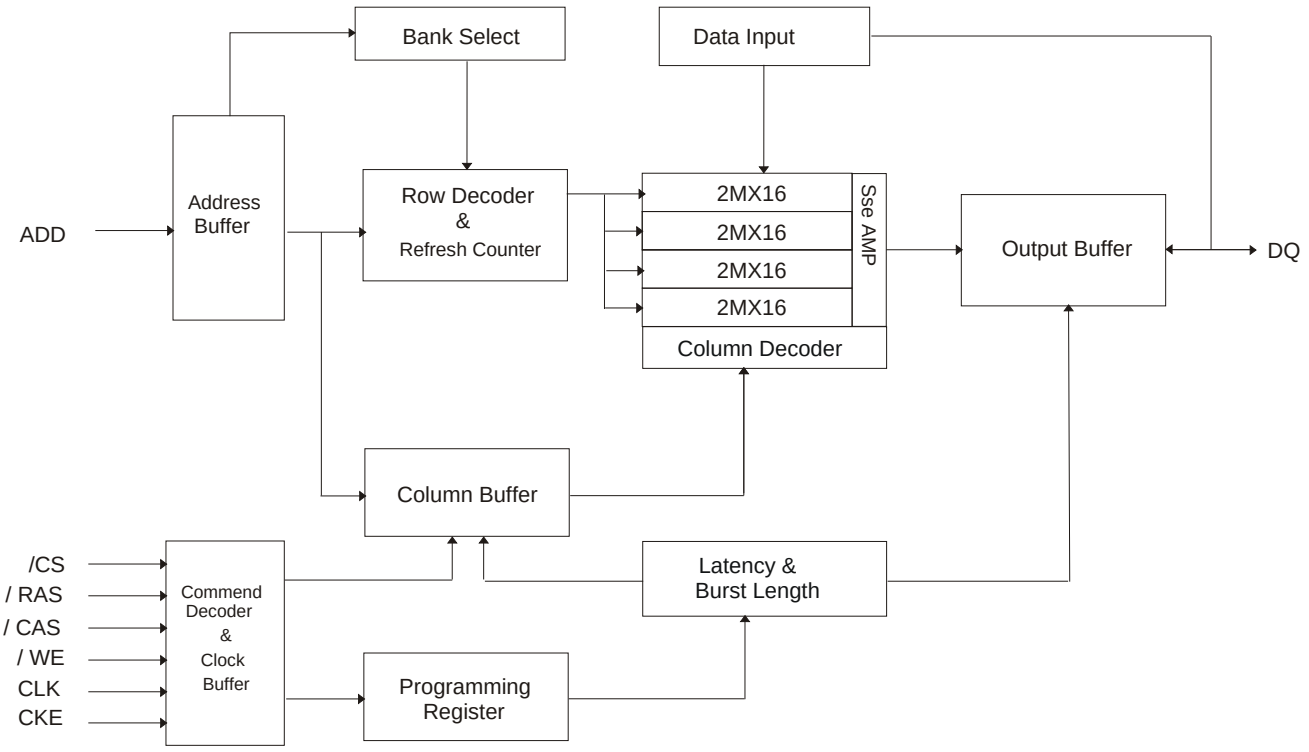
(400mil x 875mil)

(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin Name	Function	Description
A0~ A11	Address	Multiplexed pins for row and column address Row address: A0 ~ A11. Column address: A0 ~ A8.
BS0, BS1	Bank	Select bank to activate during row address latch time, or bank to read/write during address latch time.
DQ0 ~DQ15	Data Input / Output	Multiplexed pins for data output and input.
/CS	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
/RAS	Row Address Strobe	Command input. When sampled at the rising edge of the clock, /RAS, /CAS and /WE define the operation to be executed.
/CAS	Column Address Strobe	Referred to /RAS
/WE	Write Enable	Referred to /RAS
UDQM/LDQM	Input /output mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
CLK	Clock Input	System clock used to sample inputs on the rising edge of clock.
CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
Vcc	Power (+3.3 V)	Power for input buffers and logic circuit inside DRAM.
Vss	Ground	Ground for input buffers and logic circuit inside DRAM.
Vcc	Q Power (+ 3.3 V) for I/O buffer	Separated power from vcc, used for output buffers to improve noise.
Vss	Q Ground for I/O buffer	Separated ground from vss, used for output buffers to improve noise.
NC	No Connection	No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on VCC supply relative to V_{SS}	VCC, VCC_Q	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to the recommended operating conditions.

Exposure to higher voltage than recommended for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VCC, VCC_Q	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	VCC_Q+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL}=2mA
Input leakage current (Input)	I_{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes:

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is $\leqq$ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leqq$ 3ns.
3. Any input 0V $\leqq$ V_{IN} $\leqq$ VCC_Q,

   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. D_{out} is disabled, 0V $\leqq$ V_{out} $\leqq$ VCC_Q

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		TTS3816B4E	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geqq t_{RC}$(min) IOL = 0mA		100	mA	1
Pre-charge standby current in power- down mode	I_{CC2P}	CKE≦V_{IL}(max), t_{CC} = 15 ns		2	mA	
	I_{CC2PS}	CKE&CLK≦V_{IL}(max), t_{CC} = ∞		2		
Pre-charge standby current in non power-down mode	I_{CC2N}	CKE≧V_{IH}(min), /CS≧V_{IH}(min) , t_{CC} = 15ns Input signals are stable		30	mA	
	I_{CC2NS}	CKE≧V_{IH}(min), CLK≦V_{IL}(Max) , t_{CC} = ∞ Input signals are stable		10		
Active standby current in power-down mode	I_{CC3P}	CKE≦V_{IL}(max), t_{CC} = 15 ns		5	mA	
	I_{CC3PS}	CKE&CLK≦V_{IL}(max), t_{CC} = ∞		5		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE≧V_{IH}(min), /CS≧V_{IH}(min) , t_{CC} = 15ns Input signals are stable		40	mA	
	I_{CC3NS}	CKE≧V_{IH}(min), CLK≦V_{IL}(Max) , t_{CC} = ∞ Input signals are stable		20		
Operating current (Burst mode)	I_{CC4}	I_{OL}=0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	CL = 3	150	mA	1
			CL = 2	140		
Refresh current	I_{CC5}	$t_{RC} \geqq t_{RC}$(min)		160	mA	2
Self refresh current	I_{CC6}	CKE≦0.2V		1	mA	

Note: 1.Measured with outputs open.

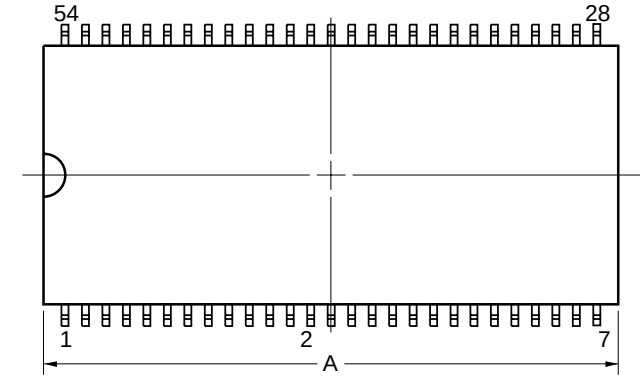
2.Refresh period is 64 ms.

AC CHARACTERISTICS AND OPERATING

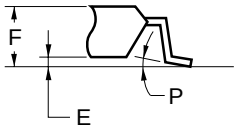
(Vcc=3.3V±0.3V, Ta=0° to 70°C)

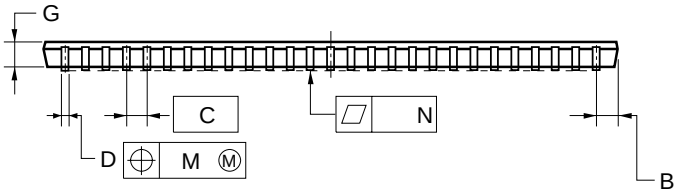
Parameter	Symbol		-7		-6		-6A		-6B		-6C		-6D		-6E		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Row active to row active delay	t_{RRD}		20		15		20		14		14		14		12		ns
/RAS to /RAS delay	t_{RCD}		20		20		30		20		15		20		18		ns
Row pre-charge time	t_{RP}		20		20		30		15		15		20		18		ns
Row active time	t_{RAS}		48	100K	45	100K	48	100K	45	100K	45	100K	45	100K	42	100K	ns
Row cycle time	t_{RC}		70		67.5		70		63		63		63		60		ns
Col. Address to col. Address delay	t_{CCD}		1		1		1		1		1		1		1		CLK
Write Recovery Time	t_{WR}		20		15		20		14		14		13		12		ns
CLK Cycle Time	t_{CK}	CL=2	10	1000	10	1000	10	1000	7.5	1000	7.5	1000	-		-		ns
		CL=3	8	1000	7.5	1000	8	1000	7.5	1000	7.5	1000	6.5	1000	6	1000	
CLK High Level width	t_{CH}		3		2.5		3		2.5		2.5		2		2		ns
CLK Low Level width	t_{CL}		3		2.5		3		2.5		2.5		2		2		ns
Access Time from CLK	t_{AC}	CL=2		6		6		8		5.4		5.4		-		-	ns
		CL=3		6		5.4		6		5.4		5.4		5.4		5	
Output Data Hold Time	t_{OH}		3		2.7		3		2.7		2.7		2.5		2		ns
Data-in Set-up Time	t_{DS}		2		1.5		2		1.5		1.5		1.5		1.5		ns
Data-in Hold Time	t_{DH}		1		1		1		1		1		1		1		ns
Address Set-up Time	t_{AS}		2		1.5		2		1.5		1.5		1.5		1.5		ns
Address Hold Time	t_{AH}		1		1		1		1		1		1		1		ns
CKE Set-up Time	t_{CKS}		2		1.5		2		1.5		1.5		1.5		1.5		ns
CKE Hold Time	t_{CKH}		1		1		1		1		1		1		1		ns
Command Set-up Time	t_{CMS}		2		1.5		2		1.5		1.5		1.5		1.5		ns
Command Hold Time	t_{CMH}		1		1		1		1		1		1		1		ns
Refresh Time	t_{REF}			64		64		64		64		64		64		64	ms
Mode register Set Cycle Time	t_{RSC}		20		15		20		14		14		12		12		ns

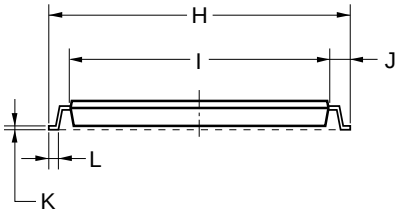
54PIN PLASTIC TSOP(II) (400mil)



detail of lead end







NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.62 MAX.	0.891 MAX.
B	0.91 MAX.	0.036 MAX.
C	0.80 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.10±0.05	0.004±0.002
F	1.20 MAX.	0.048 MAX.
G	1.00	0.039
H	11.76±0.20	0.463±0.008
I	10.16±0.10	0.400±0.004
J	0.80±0.20	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.50±0.10	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$