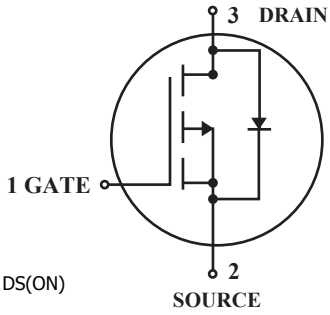
WEITRON

WTD9575

Surface Mount P-Channel Enhancement Mode POWER MOSFET

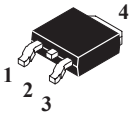
Pb Lead(Pb)-Free



DRAIN CURRENT
-15 AMPERES
DRAIN SOURCE VOLTAGE
-60 VOLTAGE

Features:

*Super High Dense Cell Design For Low $R_{DS(ON)}$
$R_{DS(ON)}$ <90m Ω@V_{GS}=-10V
*Simple Drive Requirement
*Lower On-resistance
*Fast Switching Characteristic
*TO-252 Package



1. GATE
2.4 DRAIN
3. SOURCE

D-PAK / (TO-252)

Maximum Ratings(T_A=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±25	
Continuous Drain Current, (V_{GS}@10V, T_C=25˚C) , (V_{GS}@10V, T_C=100˚C)	I_D	-15 -9.5	A
Pulsed Drain Current[1]	I_{DM}	-45	
Total Power Dissipation(T_C=25˚C)	P_D	36	W
Maximum Thermal Resistace Junction-case	$R_{\theta JC}$	3.5	˚C/W
Maximum Thermal Resistace Junction-ambient	$R_{\theta JA}$	110	˚C/W
Operating Junction and Storage Temperature Range	TJ,Tstg	-55~+150	˚C

Device Marking

WTD9575=9575

Electrical Characteristics (T_A = 25℃ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Static					
Drain-Source Breakdown Voltage V_{GS}=0,I_D=-250μA	BV_{DSS}	-60	-	-	V
Gate-Source Threshold Voltage V_{DS}=V_{GS},I_D=-250μA	$V_{GS(Th)}$	-1.0	-	-3.0	
Gate-Source Leakage current V_{GS}=±25V	I_{GSS}	-	-	±100	nA
Drain-SourceLeakage Current(Tj=25˚C) V_{DS}=-60V,V_{GS}=0	I_{DSS}	-	-	-1	μA
Drain-SourceLeakage Current(Tj=70˚C) V_{DS}=-48V,V_{GS}=0		-	-	-25	
Drain-SourceOn-Resistance V_{GS}=-10V,I_D=-12A V_{GS}=-4.5V,I_D=-9A	$R_{DS(on)}$	- -	- -	90 120	mΩ
Forward Transconductance V_{DS}=-10V,I_D=-9A	gfs	-	14	-	S
Dynamic					
Input Capacitance V_{GS}=0V,V_{DS}=-25V,f=1.0MHz	C_{iss}	-	1660	2660	pF
Output Capacitance V_{GS}=0V,V_{DS}=-25V,f=1.0MHz	C_{oss}	-	160	-	
Reverse Transfer Capacitance V_{GS}=0V,V_{DS}=-25V,f=1.0MHz	C_{rss}	-	100	-	

Switching

Turn-on Delay Time[2] V_{DS}=-30V,V_{GS}=-10V,I_D=-9A,R_D=3.3Ω,R_G=3.3Ω	$t_{d(on)}$	-	10	-	ns
Rise Time V_{DS}=-30V,V_{GS}=-10V,I_D=-9A,R_D=3.3Ω,R_G=3.3Ω	t_r	-	19	-	
Turn-off Delay Time V_{DS}=-30V,V_{GS}=-10V,I_D=-9A,R_D=3.3Ω,R_G=3.3Ω	$t_{d(off)}$	-	46	-	
Fall Time V_{DS}=-30V,V_{GS}=-10V,I_D=-9A,R_D=3.3Ω,R_G=3.3Ω	t_f	-	53	-	
Total Gate Charge[2] V_{DS}=-48V,V_{GS}=-4.5V,I_D=-9A	Q_g	-	17	27	nC
Gate-Source Charge V_{DS}=-48V,V_{GS}=-4.5V,I_D=-9A	Q_{gs}	-	5	-	
Gate-Source Change V_{DS}=-48V,V_{GS}=-4.5V,I_D=-9A	Q_{gd}	-	6	-	

Source-Drain Diode Characteristics

Forward On Voltage[2] V_{GS}=0V,I_S=-9A	V_{SD}	-	-	-1.2	V
Reverse Recovery Time V_{GS}=0V,I_S=-9A,dI/dt=100A/μs	T_{rr}	-	56	-	ns
Reverse Recovery Charge V_{GS}=0V,I_S=-9A,dI/dt=100A/μs	Q_{rr}	-	159	-	nC

Note: 1. Pulse width limited by safe operating area.
2. Pulse width ≤ 300μs, duty cycle ≤ 2%.

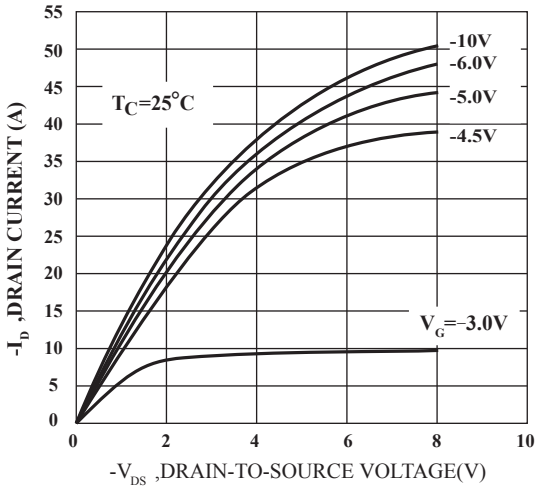


FIG.1 Typical Output Characteristics

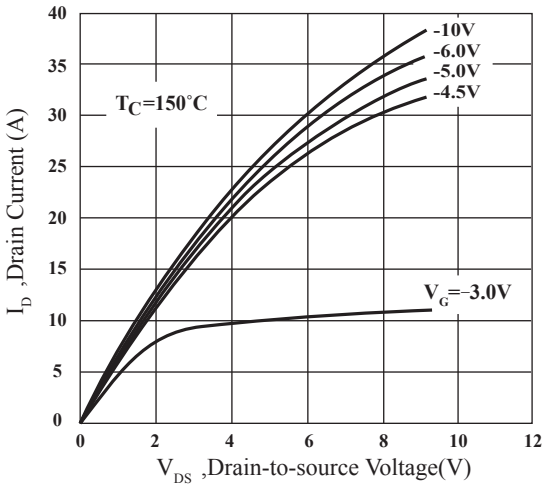


Fig.2 Typical Output Characteristics

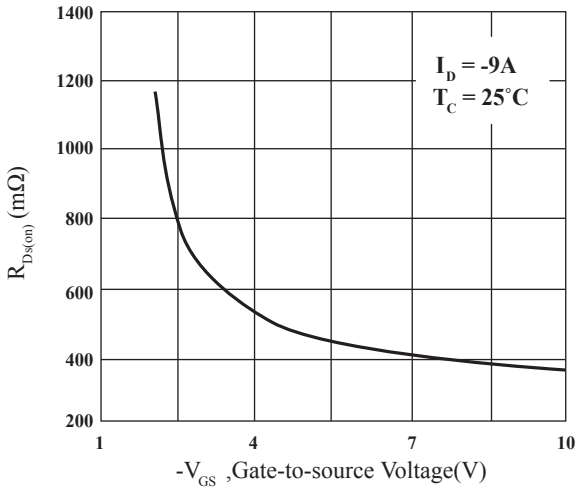


Fig.3 On-Resistance v.s. Gate Voltage

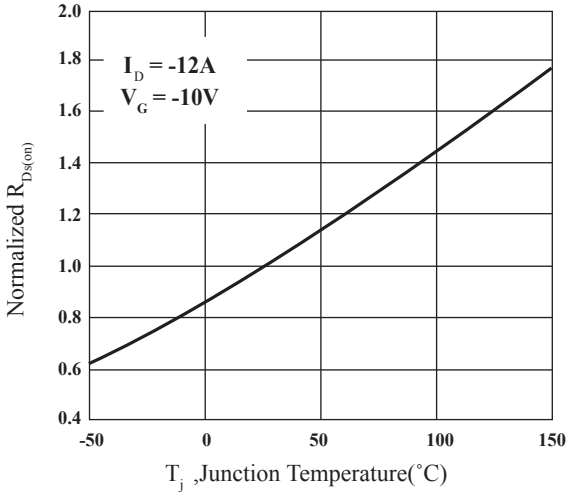


Fig.4 Normalized OnResistance

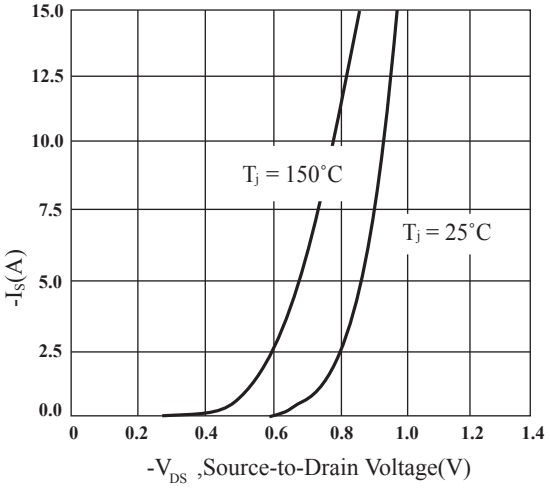


Fig.5 Forward Characteristics of Reverse Diode

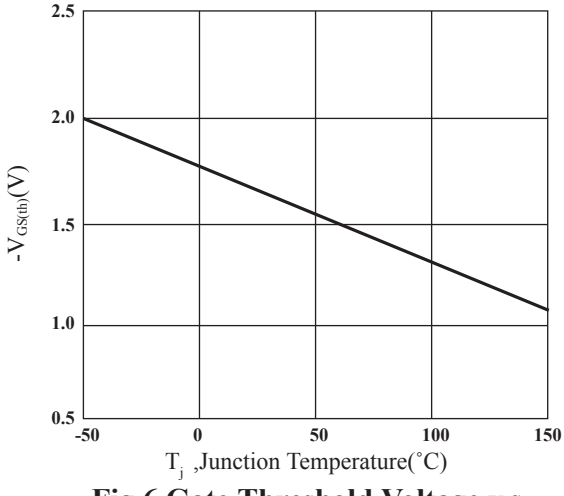


Fig.6 Gate Threshold Voltage v.s. Junction Temperature

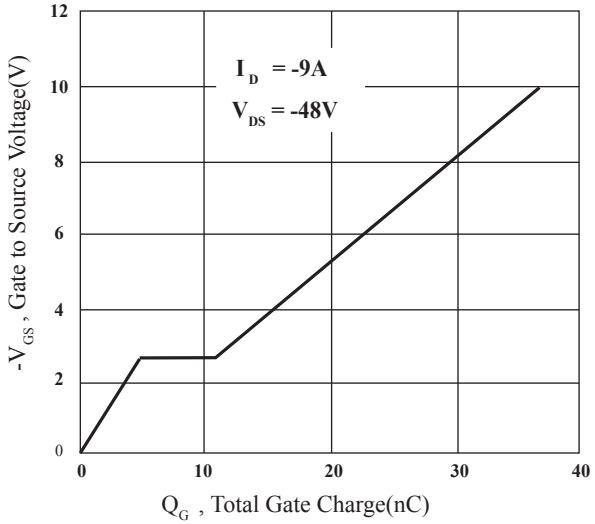


Fig 7. Gate Charge Characteristics

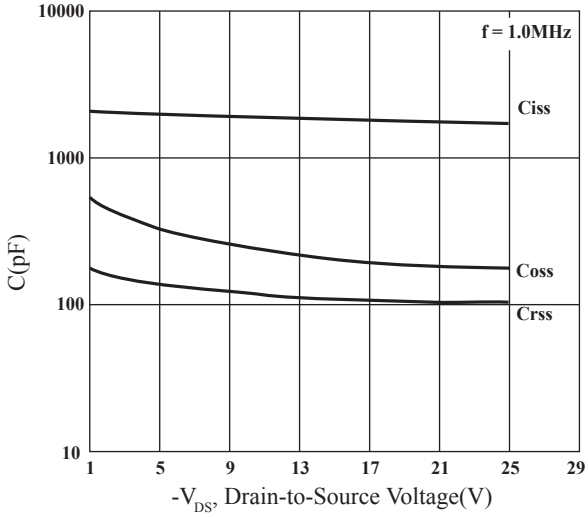


Fig 8. Typical Capacitance Characteristics

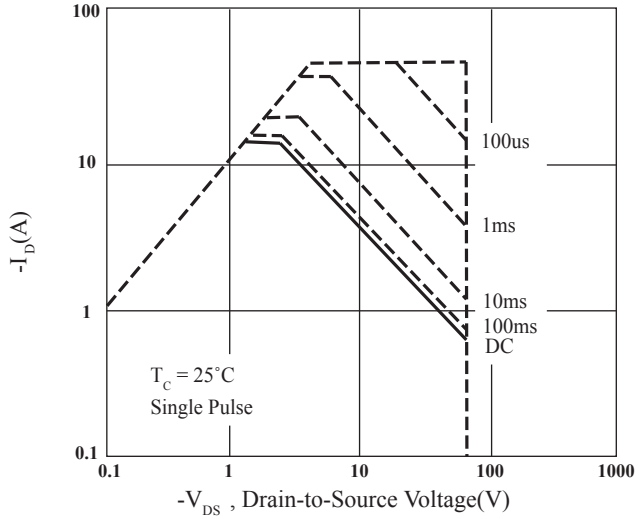


Fig 9. Maximum Safe Operation Area

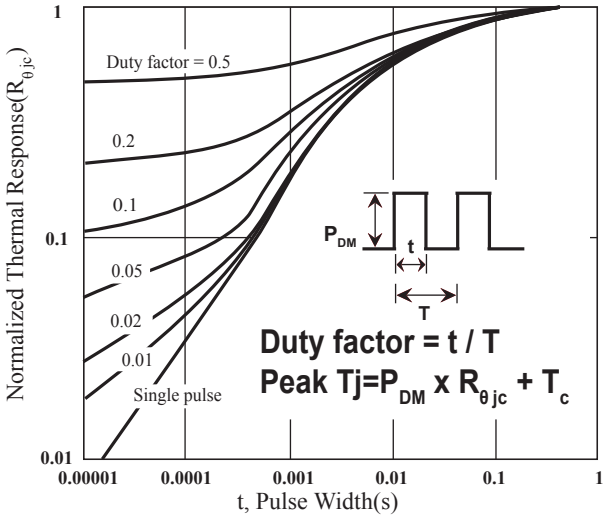


Fig 10. Effective Transient Thermal Impedance

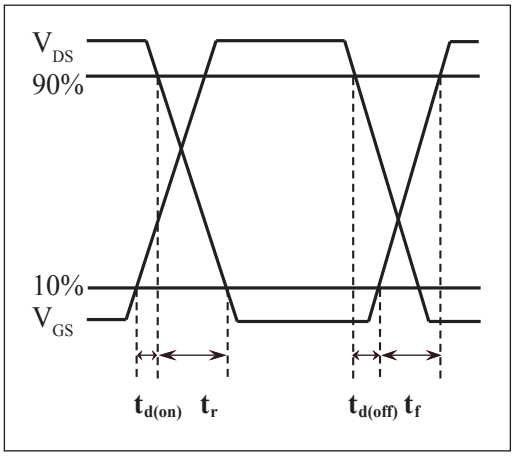


Fig 11. Switching Time Circuit

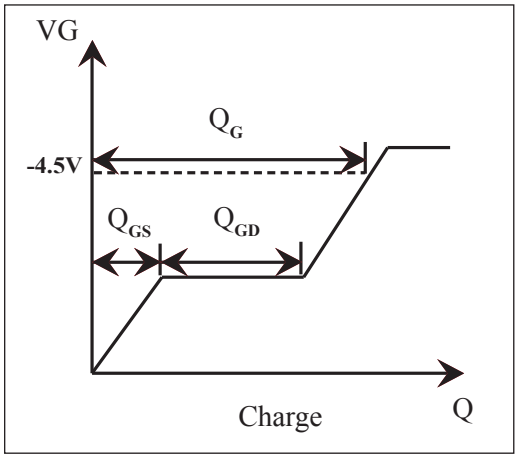
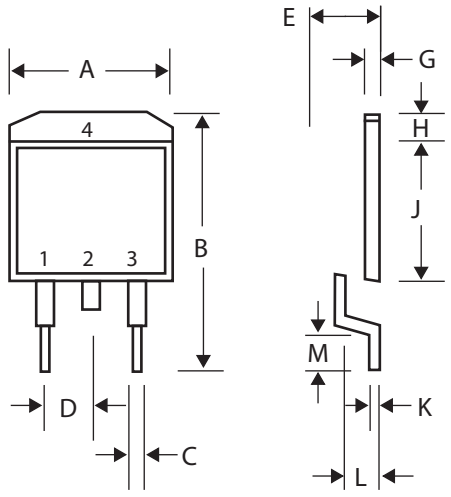


Fig.12 Gate Charge Waveform

D-PAK / (TO-252) Outline Dimension

Unit:mm



D-PAK		
Dim	**Min**	**Max**
A	6.40	6.80
B	9.00	10.00
C	0.50	0.80
D	-	2.30
E	2.20	2.50
G	0.45	0.55
H	1.00	1.60
J	5.40	5.80
K	0.30	0.64
L	0.70	1.70
M	0.90	1.50