

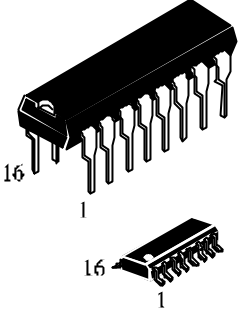
IN74HC174A

**Hex D Flip-Flop with
Common Clock and Reset
High-Performance Silicon-Gate CMOS**

The IN74HC174A is identical in pinout to the LS/ALS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

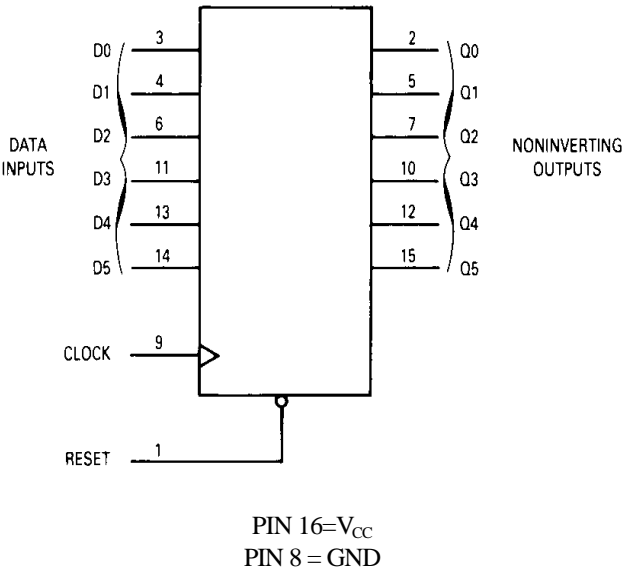


N SUFFIX
PLASTIC

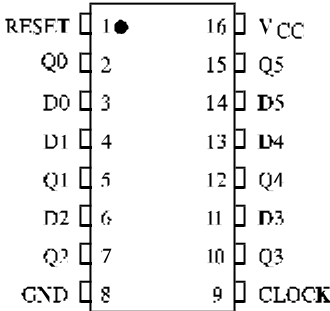
D SUFFIX
SOIC

ORDERING INFORMATION
IN74HC174AN Plastic
IN74HC174AD SOIC
IZ74HC174A Chip
 $T_A = -55^\circ$ to 125° C for all packages




LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

X = Don't care
L = LOW voltage level
H = HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1,5 mm from Case for 4 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} =2.0 V	0	1000	ns
	V _{CC} =4.5 V	0	500	
	V _{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} ≥ V _{CC} -0.1 V or ≤0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} ≤0.1 V or ≥V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$, $V_{IL}=0\text{ V}$, $V_{IH}=V_{CC}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{\text{PLH}}, t_{\text{PHL}}$	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t_{PHL}	Maximum Propagation Delay , Reset to Q (Figures 2 and 4)	2.0	110	140	160	ns
		4.5	21	28	32	
		6.0	19	24	27	
$t_{\text{TLH}}, t_{\text{THL}}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output)	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{\text{PD}}V_{CC}^2f+I_{CC}V_{CC}$	62			

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$, $V_{IL}=0\text{ V}$, $V_{IH}=V_{CC}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55 °C to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
t_{SU}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{h}	Minimum Hold Time, Clock to Data (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_{w}	Minimum Pulse Width, Clock (Figure 1)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t_{w}	Minimum Pulse Width, Reset (Figure 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

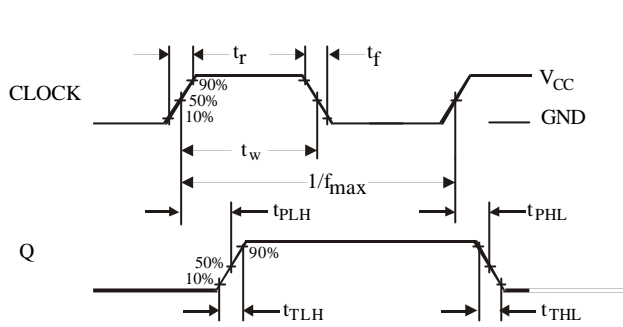


Figure 1. Switching Waveforms

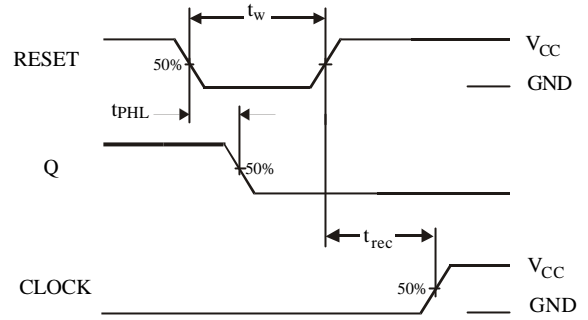


Figure 2. Switching Waveforms

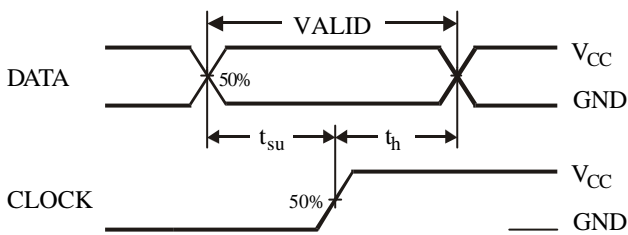


Figure 3. Switching Waveforms

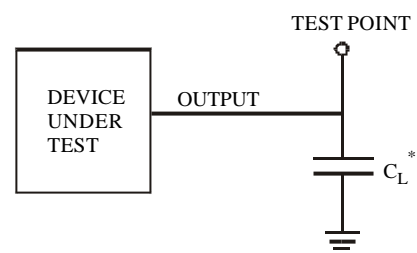
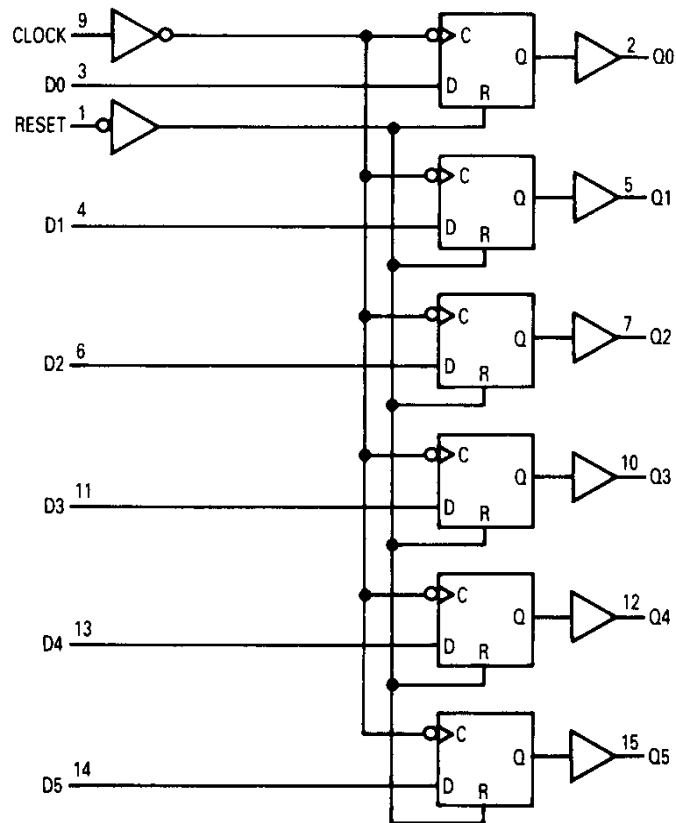
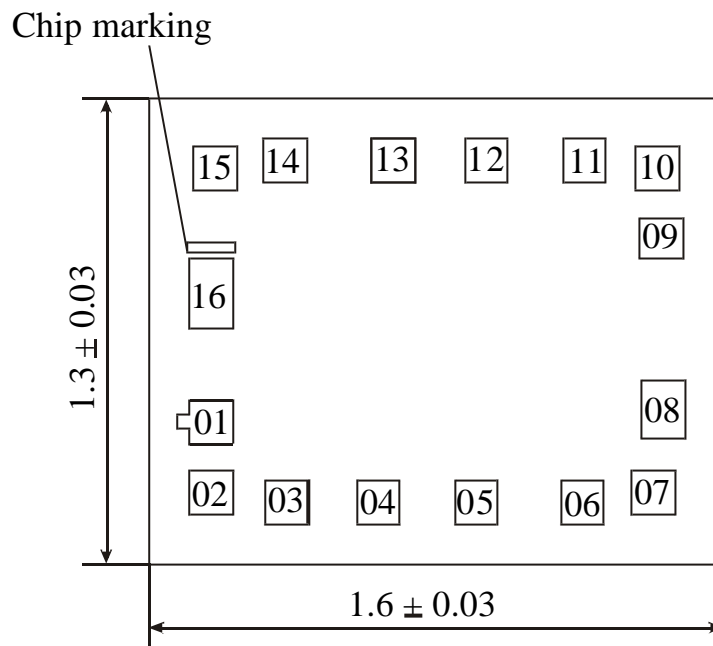


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Chip marking :15HC174

Location of marking (mm): left lower corner $x = 0.110$, $y = 0.870$; right lower corner $x = 0.240$, $y = 0.900$

Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset	0.115	0.340	0.12×0.12
02	Q0	0.115	0.140	0.12×0.12
03	D0	0.325	0.115	0.12×0.12
04	D1	0.580	0.115	0.12×0.12
05	Q1	0.850	0.115	0.12×0.12
06	D2	1.145	0.115	0.12×0.12
07	Q2	1.345	0.140	0.12×0.12
08	GND	1.370	0.355	0.12×0.16
09	Clock	1.365	0.815	0.12×0.12
10	Q3	1.355	1.045	0.12×0.12
11	D3	1.155	1.065	0.12×0.12
12	Q4	0.880	1.065	0.12×0.12
13	D4	0.620	1.065	0.12×0.12
14	D5	0.320	1.065	0.12×0.12
15	Q5	0.125	1.045	0.12×0.12
16	Vcc	0.115	0.660	0.12×0.19

Note: Location is given as per passivation layer