FEATURES

- Compatible with Sound Blaster™, Sound Blaster Pro™, and Windows Sound System™
- Integrated CrystalClear™ 3D Stereo Enhancement
- Enhanced Stereo Full Duplex Operation
- Dual Type-F DMA Support
- Industry Leading Delta-Sigma Data Converters (86 dB FS A)
- Default Internal PnP Resources
- 3.3 V or 5 V ISA Bus Operation
- APM and ACPI Compliant Power Management
- Asynchronous Digital Serial Interface (ZVPORT)
- CS4610 Audio Accelerator Interface
- CS9236 Wavetable Interface
- CS4236B/CS4237B/CS4238B Register Compatible

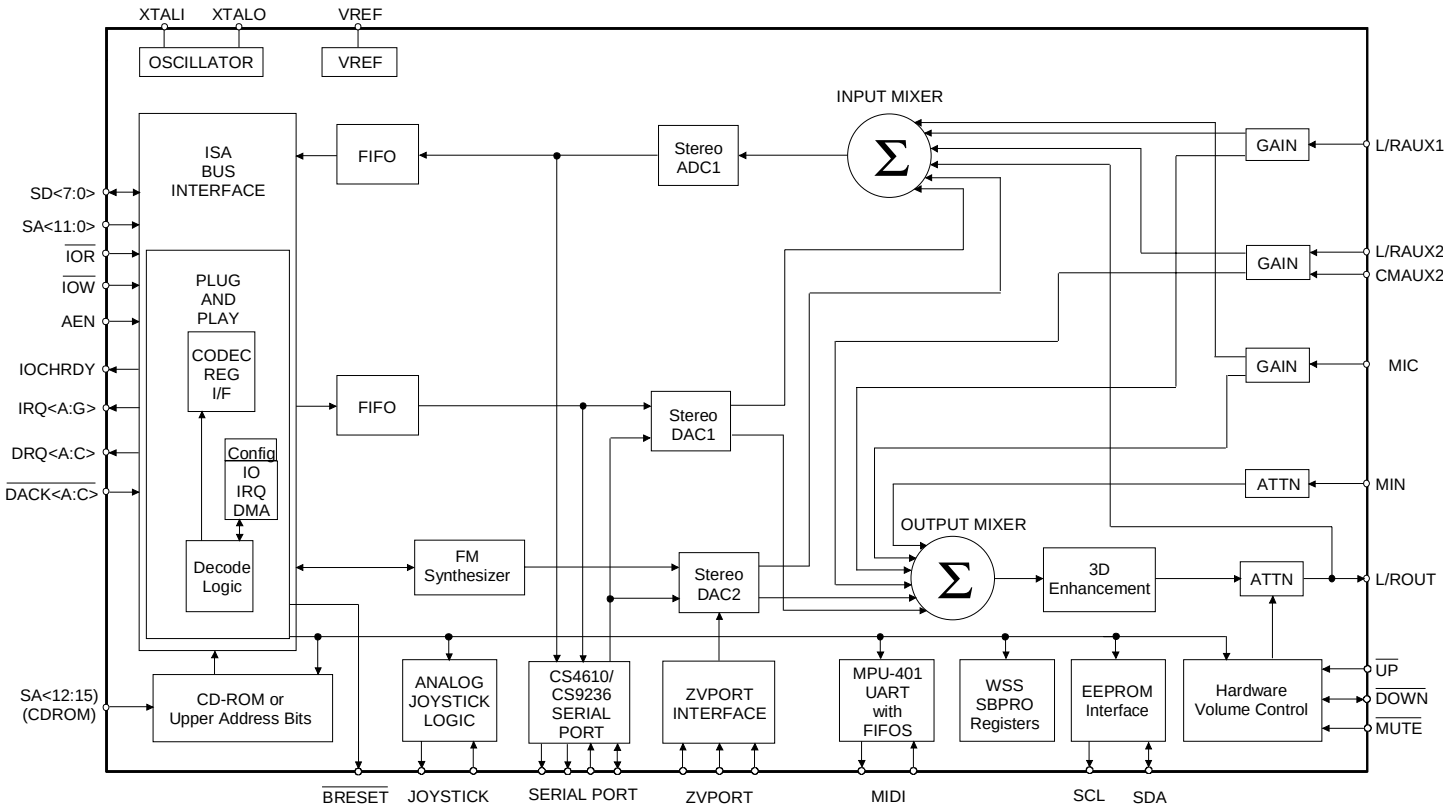
CrystalClear™ Portable ISA Audio System

DESCRIPTION

The CS4239 is a single chip multimedia audio system that is a pin-compatible upgrade to the CS423xB for many designs. The product includes an integrated FM synthesizer and a Plug-and-Play interface. In addition, the CS4239 includes hardware master volume control pins as well as extensive power management and 3D sound technology. The CS4239 adds a Zoom-Video asynchronous digital serial interface to the industry standard CS423xB. The CS4239 is compatible with the Microsoft® Windows Sound System standard and will run software written to the Sound Blaster and Sound Blaster Pro interfaces. The CS4239 is fully compliant with Microsoft's PC '97 and PC '98 audio requirements.

ORDERING INFO

CS4239-JQ 100 pin TQFP, 14x14x1.4mm
CS4239-KQ 100 pin TQFP, 14x14x1.4mm



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ANALOG CHARACTERISTICS

(T_A = 25 °C; VA, VD1, VDF1-VDF3 = +5 V;
Input Levels: Logic 0 = 0 V, Logic 1 = VD1; 1 kHz Input Sine wave; Sample Frequency, Fs = 44.1 kHz;
Measurement Bandwidth is 20 Hz to 20 kHz, 16-bit linear coding.)

Parameter*		Symbol	CS4239-JQ Min	CS4239-JQ Typ	CS4239-JQ Max	CS4239-KQ Min	CS4239-KQ Typ	CS4239-KQ Max	Units
Analog Input Characteristics (A-D-PC) - Volume set to 0 dB unless otherwise specified.									
ADC1 Resolution	(Note 1)		16	-	-	16	-	-	Bits
ADC1 Differential Nonlinearity	(Note 1)		-	-	±0.5	-	-	±0.5	LSB
Frequency Response	Ac = ±1 dB	FR	-	-	-	20	-	19000	Hz
Dynamic Range	AUX1, AUX2	DR	-	-80	-	-80	-85	-	dB FS A
	(Note 2) MIC		-	-75	-	-72	-79	-	dB FS A
Total Harmonic Distortion+Noise	AUX1, AUX2		-	-66	-	-75	-80	-	dB FS A
-3 dB FS input	(Note 2) MIC	THD+N	-	-66	-	-72	-80	-	dB FS A
Interchannel Isolation (Note 1):	Left to Right		-	-80	-	-70	-80	-	dB
10 kHz input	AUX1/2 to MIC		-	-80	-	-	-80	-	dB
	AUX1 to AUX2		-	-80	-	-	-90	-	dB
Interchannel Gain Mismatch	AUX1, AUX2		-	-	±0.5	-	-	±0.5	dB
	MIC		-	-	±0.5	-	-	±0.5	dB
ADC1 Offset Error	0 dB Gain		-	-	-	-	±10	±200	LSB
Full Scale Input Voltage:									
	(MGE/MBST=1) MIC		0.25	0.28	-	0.25	0.28	-	V_{pp}
	(MGE/MBST=0) MIC		2.5	2.8	-	2.5	2.8	-	V_{pp}
	AUX1, AUX2, MIN		2.5	2.8	-	2.5	2.8	-	V_{pp}
Gain Drift			-	±100	-	-	±100	-	ppm/°C
Input Resistance (Note 1):	MIC		8	11	-	8	11	-	kΩ
	AUX1, AUX2, MIN		20	23	-	20	23	-	kΩ
Input Capacitance	(Note 1)		-	-	15	-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, no production testing.
2. MGE or MBST = 1 (see WSS Indirect Reg I0 or X2).

*Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*	Symbol	CS4239-JQ Min	CS4239-JQ Typ	CS4239-JQ Max	CS4239-KQ Min	CS4239-KQ Typ	CS4239-KQ Max	Units
Analog Output Characteristics (PC-D-A) - Volume set to 0 dB unless otherwise specified.								
DAC1 Resolution (Note 1)		16	-	-	16	-	-	Bits
DAC1 Differential Nonlinearity (Note 1)		-	-	±0.5	-	-	±0.5	LSB
DAC1 Frequency Response Ac = ±1 dB	FR	-	-	-	20	-	19000	Hz
DAC1 Dynamic Range	DR	-	-86	-	-80	-86	-	dB FS A
DAC1 Total Harmonic Distortion + Noise -3 dB FS input (Note 3)	THD+N	-	-80	-	-75	-80		dB FS A
DAC1 Interchannel Isolation (Notes 1,3) 10 kHz input		-	-90	-	-80	-90	-	dB
DAC1 Interchannel Gain Mismatch		-	±0.1	±0.5	-	±0.1	±0.5	dB
Voltage Reference Output - VREF		2.0	2.2	2.5	2.0	2.2	2.5	V
Voltage Reference Output Current - VREF (Notes 1,4)		-	100	400	-	100	400	µA
DAC1 Programmable Attenuation Span		90	94.5	-	90	94.5	-	dB
DAC1 Atten. Step Size: Greater than -82.5 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2.0	1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC1 Offset Voltage		-	-	-	-	±1	±10	mV
Full Scale Output Voltage: (Note 3)		2.5	2.8	3.3	2.5	2.8	3.3	Vpp
Gain Drift (Note 1)		-	100	-	-	100	-	ppm/°C
DAC1 Deviation from Linear Phase (Note 1) (Passband)		-	-	1	-	-	1	Degree
External Load Impedance (Note 1)		10	-	-	10	-	-	kΩ
Mute Attenuation (Note 1)		80	-	-	80	-	-	dB
Power Supply								
Power Supply Current Digital, Operating Analog, Operating Total Operating Total Power Down		- - - -	70 30 100 -	- - - -	- - - -	70 30 100 -	80 35 - 1	mA mA mA mA
Power Supply Rejection, 1 kHz input (Note 1)		40	-	-	40	-	-	dB

Notes: 3. 10 kΩ, 100 pF load.
4. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.

MIXERS (T_A = 25 °C; VA, VD1, VDF1-VDF3 = +5 V; Input Levels: Logic 0 = 0 V, Logic 1 = VD1; 1 kHz Input Sine wave, Measurement Bandwidth is 20 Hz to 20 kHz.)

Parameter*		Symbol	CS4239-JQ			CS4239-KQ			Units
			Min	Typ	Max	Min	Typ	Max	
Mixer Gain Range Span	AUX1, AUX2		-	-	-	42	45	-	dB
	MIC		-	-	-	40	45	-	dB
	Hardware Master		-	-	-	75	86	-	dB
	DAC1, DAC2		-	-	-	85	94.4	-	dB
Step Size	MIC, AUX1, AUX2		-	-	-	1.3	1.5	1.7	dB
	Hardware Master		-	-	-	1.6	2.0	2.4	dB
	DAC1, DAC2		-	-	-	0.9	1.5	2.0	dB
Frequency Response (A-A)	Ac = ±1 dB (Notes 1,3)	FR	-	-	-	20		20000	Hz
Dynamic Range: (A-A)	(Notes 1,3)	DR	-	-88	-	-90	-97	-	dB FS A
Total Harmonic Distortion+Noise (A-A)	(Notes 1,3) -3 dB FS input	THD+N	-	-85	-	-85	90	-	dB FS A

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND, SGND = 0 V, all voltages with respect to 0 V.)

Parameter			Symbol	Min	Typ	Max	Units
Power Supplies:	Digital		VD1	4.75	5.0	5.25	V
		(Note 5)		3.0	3.3	3.6	V
	Digital Filtered		VDF1-VDF3	4.75	5.0	5.25	V
	Analog		VA	4.75	5.0	5.25	V
Operating Ambient Temperature			T_A	0	25	70	°C

Note 5. When VD1 is powered from 3.3 Volts, all ISA bus input pins connected to the CS4239 must also be 3.3 Volts.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND, SGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital	VD1	-0.3	6.0	V
		VDF1-VDF3	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)			1	W
Input Current per Pin	(Except Supply Pins)		-10.0	+10.0	mA
Output Current per Pin	(Except Supply Pins)		-50	+50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage:	SA<11:0>, IOR, IOW, AEN				
	SD<7:0>, DACK<A:C>		-0.3	VD1+0.3	V
	All other digital inputs		-0.3	VDF+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DIGITAL CHARACTERISTICS

(T_A = 25°C; VA, VDF1-VDF3 = 5 V, VD1 = 5 V/3 V; AGND, DGND1, SGND1-SGND4 = 0 V.)

Parameter			Symbol	Min	Max	Units
High-level Input Voltage		Digital Inputs	V_{IH}	2.0		V
		XTALI		VDF-1.0		V
Low-level Input Voltage			V_{IL}		0.8	V
High-level Output Voltage:	ISA Bus Pins	I_0 = -24.0 mA	V_{OH}	2.4	VD1	V
	IOCHRDY, SDA	(Note 6)			VDF	V
	All Others	I_0 = -1.0 mA		2.4	VDF	V
Low-level Output Voltage:	ISA Bus Pins	I_0 = 24.0 mA	V_{OL}		0.4	V
	MCLK, SDOUT, MIDOUT, IOCHRDY	I_0 = 8.0 mA			0.4	V
	All Others	I_0 = 4.0 mA			0.4	V
Input Leakage Current		(Digital Inputs)		-10	10	µA
Output Leakage Current		(High-Z Digital Outputs)		-10	10	µA

Note 6. Open Collector pins. High level output voltage dependent on external pull up (required) used and number of peripherals (gates) attached.

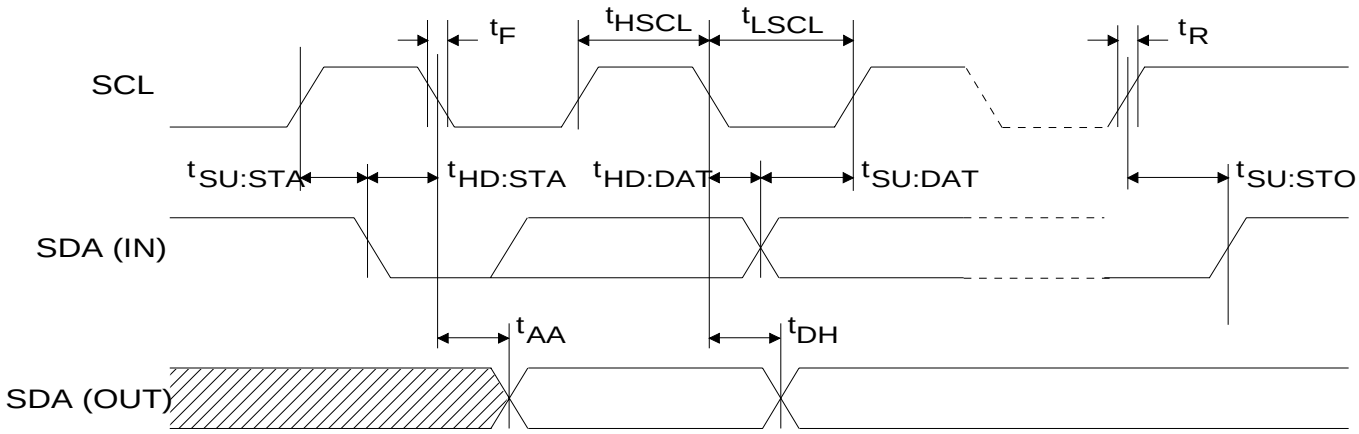
ADC1/DAC1 DIGITAL FILTER CHARACTERISTICS (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
Passband			0		0.40xFs	Hz
Frequency Response			-1.0		+0.5	dB
Passband Ripple	(0-0.40xFs)				±0.1	dB
Transition Band			0.40xFs		0.60xFs	Hz
Stop Band			0.60xFs			Hz
Stop Band Rejection			74			dB
Group Delay	8- and 16-bit formats				10/Fs	s
Group Delay Variation vs. Frequency	ADC1 DAC1				0.0 0.1/Fs	µs µs

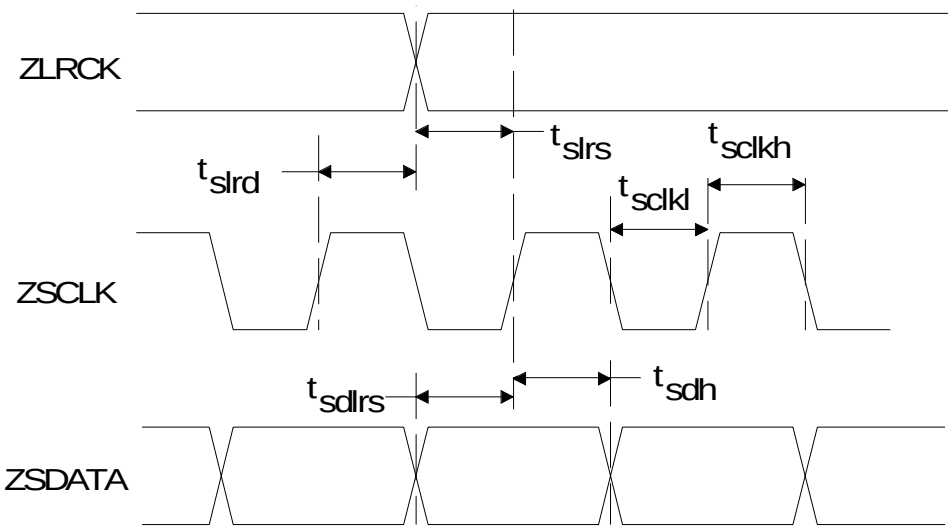
Timing Parameters (T$_A$ = 25 °C; VA, VD1, VDF1-VDF3 = +5 V; outputs loaded with 30 pF; Input Levels: Logic 0 = 0 V, Logic 1 = VD1, Rise/Fall time = 2 ns; Input/Output reference levels = 2.5 V)

Parameter		Symbol	Min	Max	Units
E^{2}PROM Timing (Note 1)					
SCL Low to SDA Data Out Valid		t_{AA}	0	3.5	µs
Start Condition Hold Time		$t_{HD:STA}$	4.0		µs
Clock Low Period		t_{LSCL}	4.7		µs
Clock High Period		t_{HSCL}	4.0		µs
Start Condition Setup Time (for a Repeated Start Condition)		$t_{SU:STA}$	4.7		µs
Data In Hold Time		$t_{HD:DAT}$	0		µs
Data In Setup Time		$t_{SU:DAT}$	250		ns
SDA and SCL Rise Time	(Note 7)	t_R		1	µs
SDA and SCL Fall Time		t_F		300	ns
Stop Condition Setup Time		$t_{SU:STO}$	4.7		µs
Data Out Hold Time		t_{DH}	0		ns
ZVPORT Timing					
ZLRCK delay after ZSCLK rising (to be ignored)		t_{slrd}	2		ns
ZLRCK setup before ZSCLK rising		t_{slrs}	32		ns
ZSCLK low period		t_{sclkl}	22		ns
ZSCLK high period		t_{sclkh}	22		ns
ZSDATA setup to ZSCLK rising		t_{sdlrs}	32		ns
ZSDATA hold after ZSCLK rising		t_{sdh}	2		ns

Notes 7. Rise time on SDA is determined by the capacitance of the SDA line with all connected gates and the external pullup resistor required.



E^{2}PROM 2-Wire Interface Timing

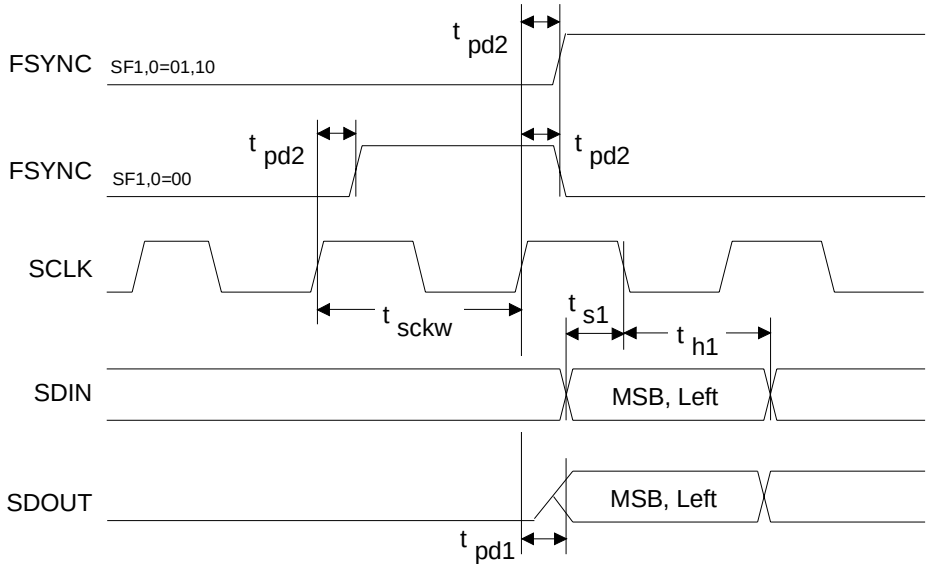


ZV-Port Input Timing

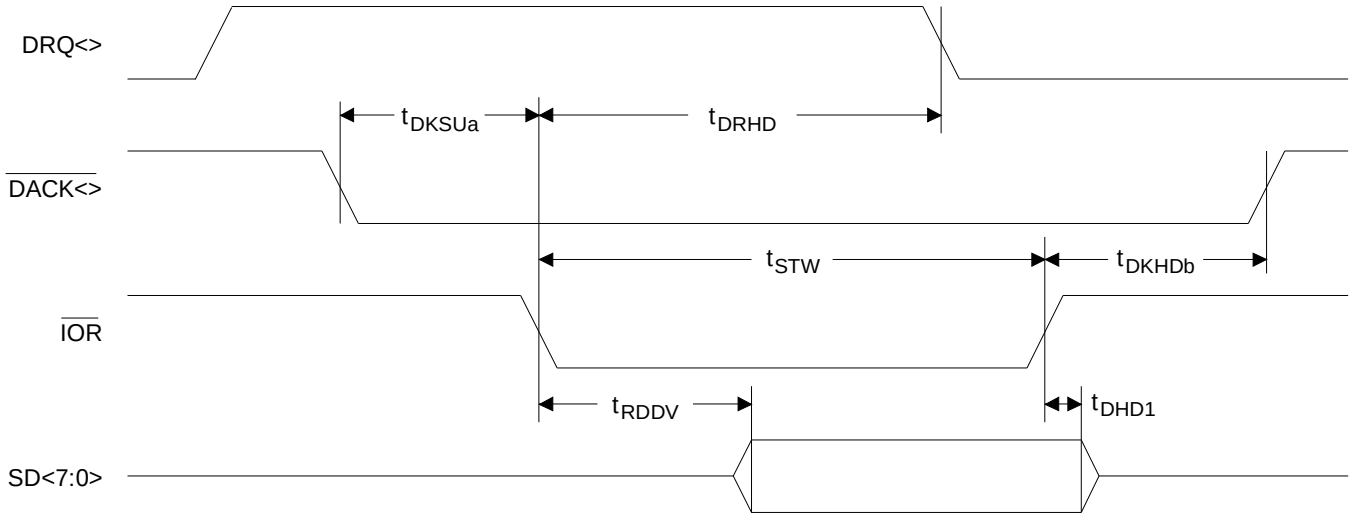
TIMING PARAMETERS (Continued)

Parameter	Symbol	Min	Max	Units
Parallel Bus Timing				
IOW or IOR strobe width	t_{STW}	90		ns
Data valid to IOW rising edge (write cycle)	t_{WDSU}	22		ns
IOR falling edge to data valid (read cycle)	t_{RDDV}		60	ns
SA <> and AEN setup to IOR or IOW falling edge	t_{ADSU}	22		ns
SA <> and AEN hold from IOW or IOR rising edge	t_{ADHD}	10		ns
DACK<> inactive to IOW or IOR falling edge (DMA cycle immediately followed by a non-DMA cycle) (Note 8)	t_{SUDK1}	60		ns
DACK<> active from IOW or IOR rising edge (non-DMA cycle completion followed by DMA cycle) (Note 8)	t_{SUDK2}	0		ns
DACK<> setup to IOR falling edge (DMA cycles) DACK<> setup to IOW falling edge (Note 8)	t_{DKSUa} t_{DKSUb}	25 25		ns ns
Data hold from IOW rising edge	t_{DHD2}	15		ns
DRQ<> hold from IOW or IOR falling edge DTM(I10) = 0 (assumes no more DMA cycles needed) DTM(I10) = 1	t_{DRHD}	 -25	45	ns
Time between rising edge of IOW or IOR to next falling edge of IOW or IOR	t_{BWDN}	80		ns
Data hold from IOR rising edge	t_{DHD1}	0	25	ns
DACK<> hold from IOW rising edge DACK<> hold from IOR rising edge	t_{DKHDa} t_{DKHDb}	25 25		ns ns
RESDRV pulse width high (Note 1)	t_{RESDRV}	1		ms
Initialization Time (Note 1, 9)	t_{INIT}	3	10	ms
EEPROM Read Time (Note 1, 10)	t_{EEPROM}	1	190	ms
XTAL, 16.9344 MHz, frequency (Notes 1, 11)		16.92	16.95	MHz
XTALI high time (Notes 1, 11)		24		ns
XTALI low time (Notes 1, 11)		24		ns
Sample Frequency (Note 1)	Fs	3.918	50	kHz
CS4610 DSP Serial Port Timing				
SCLK rising to SDOUT valid (Note 1)	t_{PD1}		60	ns
SCLK rising to FSYNC transition (Note 1)	t_{PD2}	-20	20	ns
SDIN valid to SCLK falling (Note 1)	t_{S1}	30		ns
SDIN hold after SCLK falling (Note 1)	t_{H1}	30		ns

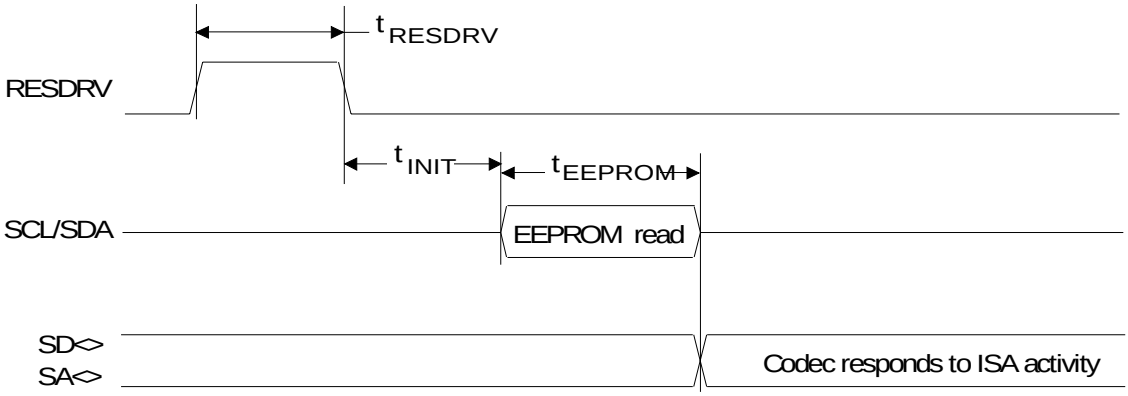
Notes: 8. AEN must be high during DMA cycles.
9. Initialization time depends on the power supply circuitry, as well as the the type of clock used.
10. EEPROM read time is dependent on amount of data in EEPROM. Minimum time relates to no EEPROM present. Maximum time relates to EEPROM data size of 1k bytes.
11. The Sample frequency specification must not be exceeded.



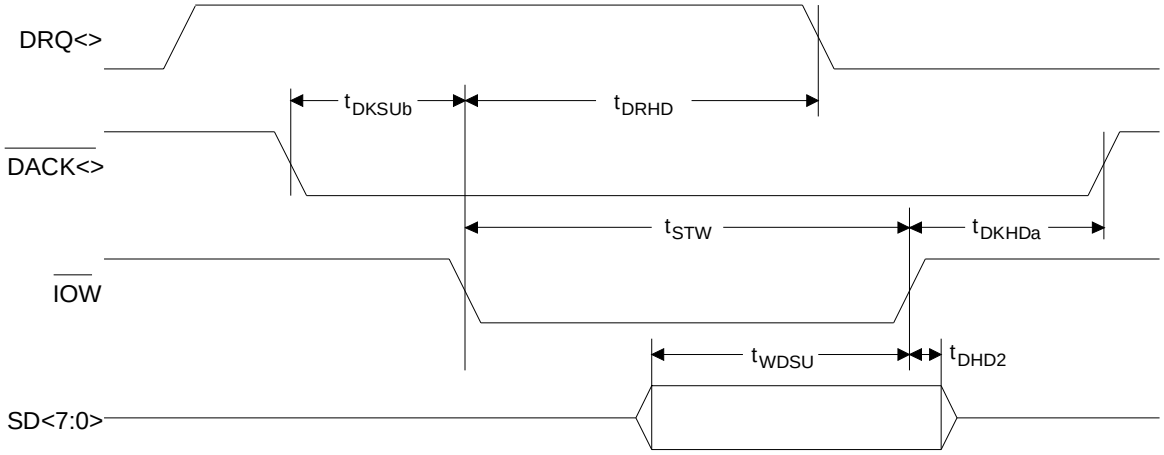
CS4610 DSP Serial Port Timing



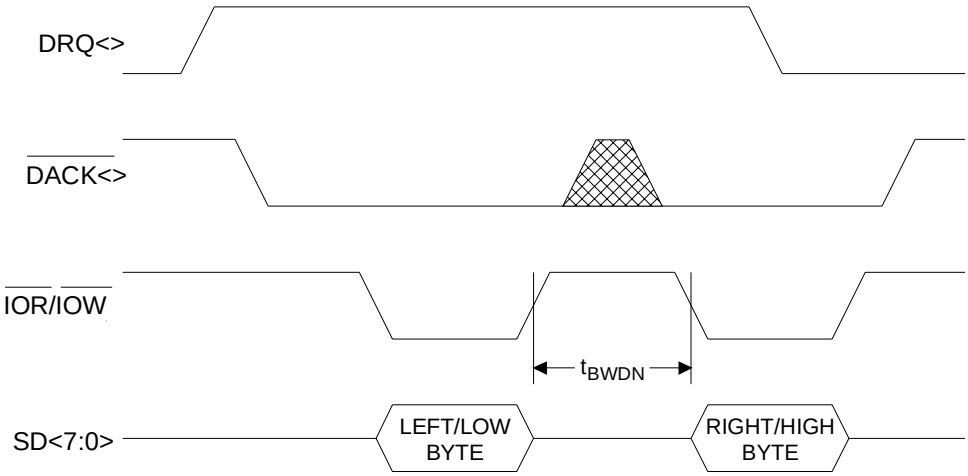
8-Bit Mono DMA Read/Capture Cycle



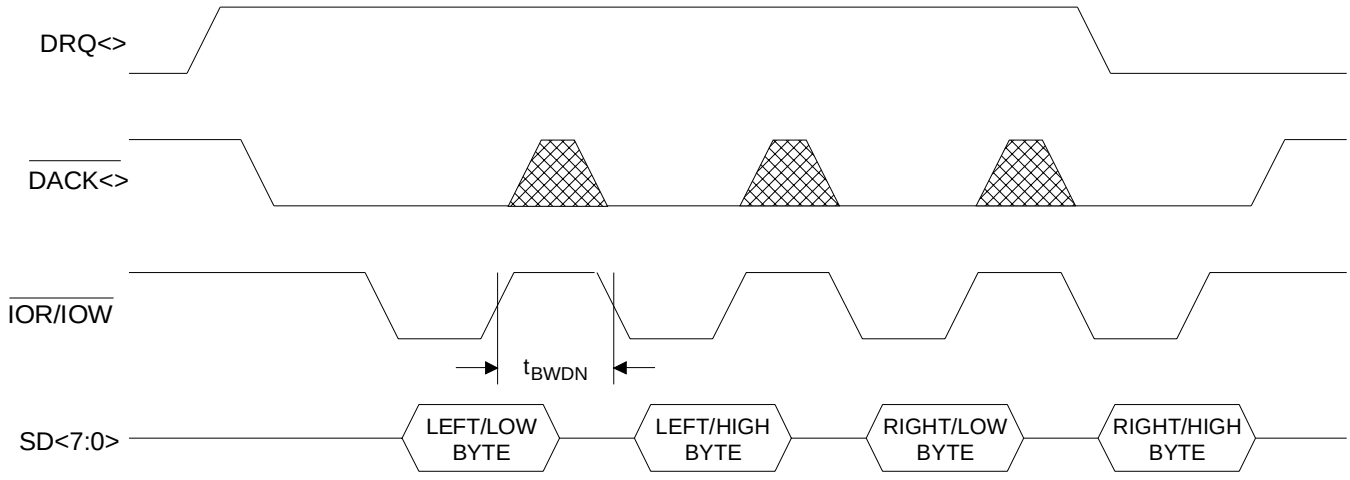
Reset Timing



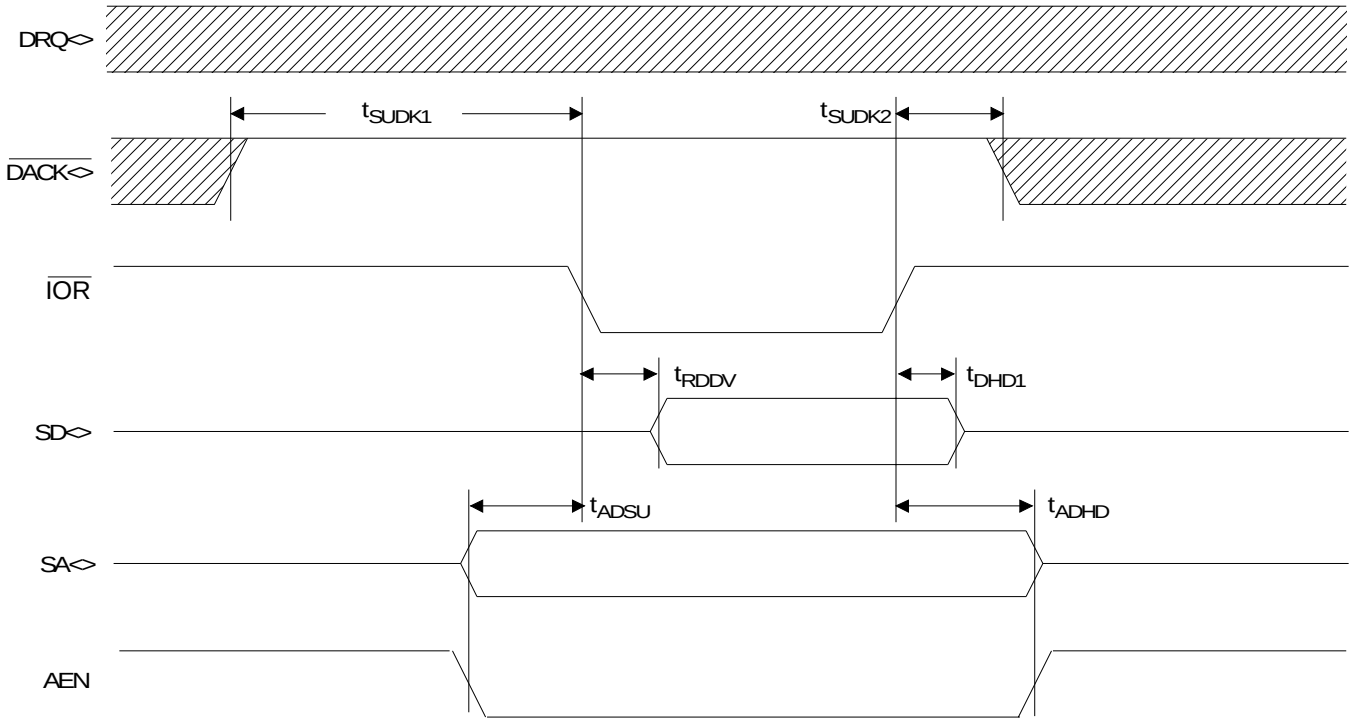
8-Bit Mono DMA Write/Playback Cycle



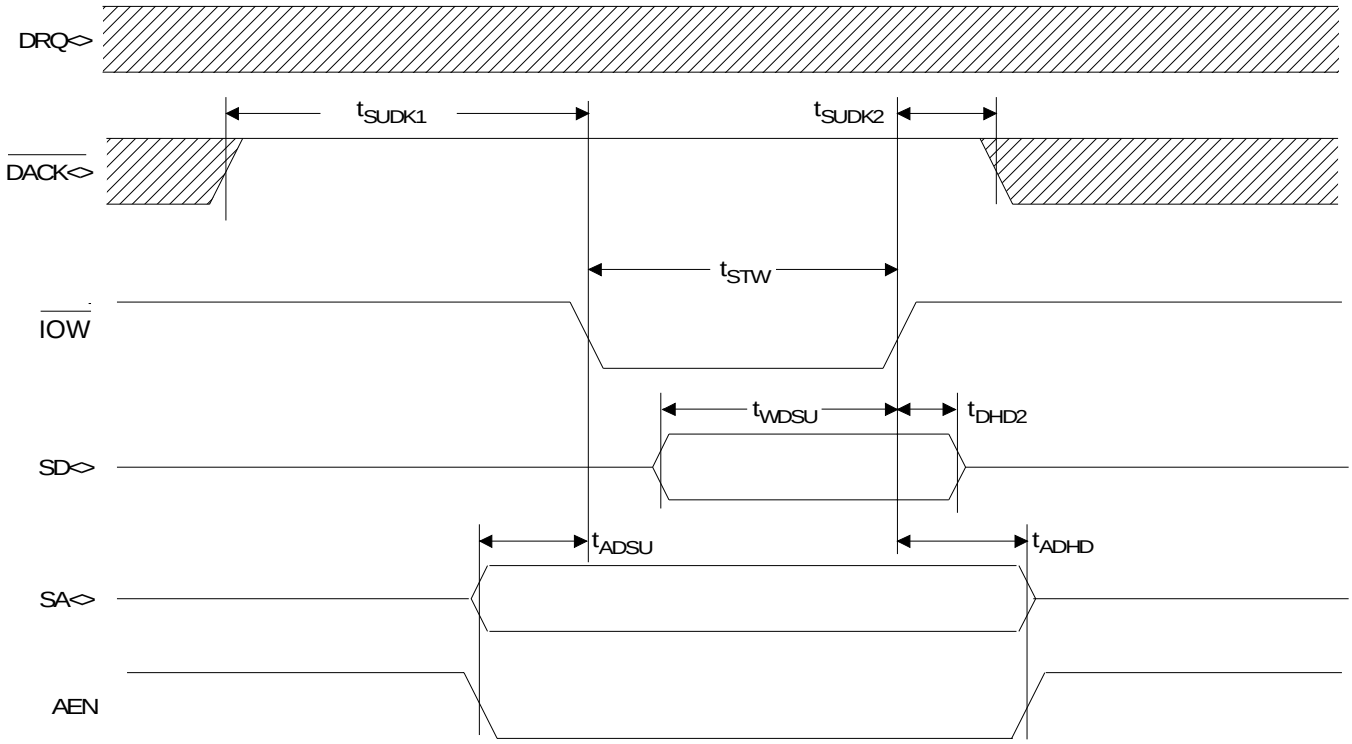
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo DMA Cycle



I/O Read Cycle



I/O Write Cycle

GENERAL DESCRIPTION

This device is comprised of six physical devices along with Plug-and-Play support for one additional external device. The internal devices are:

- Windows Sound System Codec
- Sound Blaster Pro Compatible Interface
- Game Port (Joystick)
- Control
- MPU-401
- FM Synthesizer

The external device is:

- IDE CDROM

On power up, this part requires a RESDRV signal to initialize the internal configuration. When initially powered up, the part is isolated from the bus, and each device supported by the part must be activated via software. Once activated, each device responds to the resources given (Address, IRQ, and DMA channels). The devices listed above are grouped into five logical devices, as shown in Figure 1 (bracketed features are supported, but typically not used). The five logical devices are:

LOGICAL DEVICE 0:
- Windows Sound System Codec (WSS Codec)
- Adlib/Sound Blaster-compatible Synthesizer
- Sound Blaster Pro Compatible Interface

LOGICAL DEVICE 1: Game Port

LOGICAL DEVICE 2: Control

LOGICAL DEVICE 3: MPU401

LOGICAL DEVICE 4: CDROM

Logical Device 0 consists of three physical devices. The WSS Codec and the Synthesizer are grouped together since the original Windows Sound System card expected an FM synthesizer if the codec was present. The Sound Blaster Pro Compatible interface, SBPro, is also grouped to allow the WSS Codec and the SBPro to share Interrupts and DMA channels. The WSS Codec, FM synthesizer, and the SBPro compatible devices are internal to the part.

Logical Device 1 is the Game Port that supports up to two joystick devices.

Logical Device 2 is the Control device that supports global features of the part. This device uses I/O locations to control power management, joystick rate, and PnP resource data loading.

Logical Device 3 is the MPU-401 interface. The MPU-401 MIDI interface includes a 16-byte FIFO for data transmitted out the MIDOUT pin and a 16-byte FIFO for data received from the MIDIN pin.

Logical Device 4 supports an IDE CDROM device. Although this logical device is listed as a CDROM, any external device that fits within the resources listed above may be substituted. This interface, is generic and can support devices using 1 to 127 I/O locations for the base address, 1 to 8 I/O locations for the alternate base address, an interrupt, and a DMA channel.

ISA Bus Interface

The 8-bit parallel I/O and 8-bit parallel DMA ports provide an interface which is compatible with the Industry Standard Architecture (ISA) bus. The ISA Interface enables the host to communicate with the various functional blocks within the part via two types of accesses: Programmed I/O (PIO) access, and DMA access.

A number of configuration registers must be programmed prior to any accesses by the host computer. The configuration registers are programmed via a Plug-and-Play configuration sequence or via configuration software provided by Cirrus Logic.

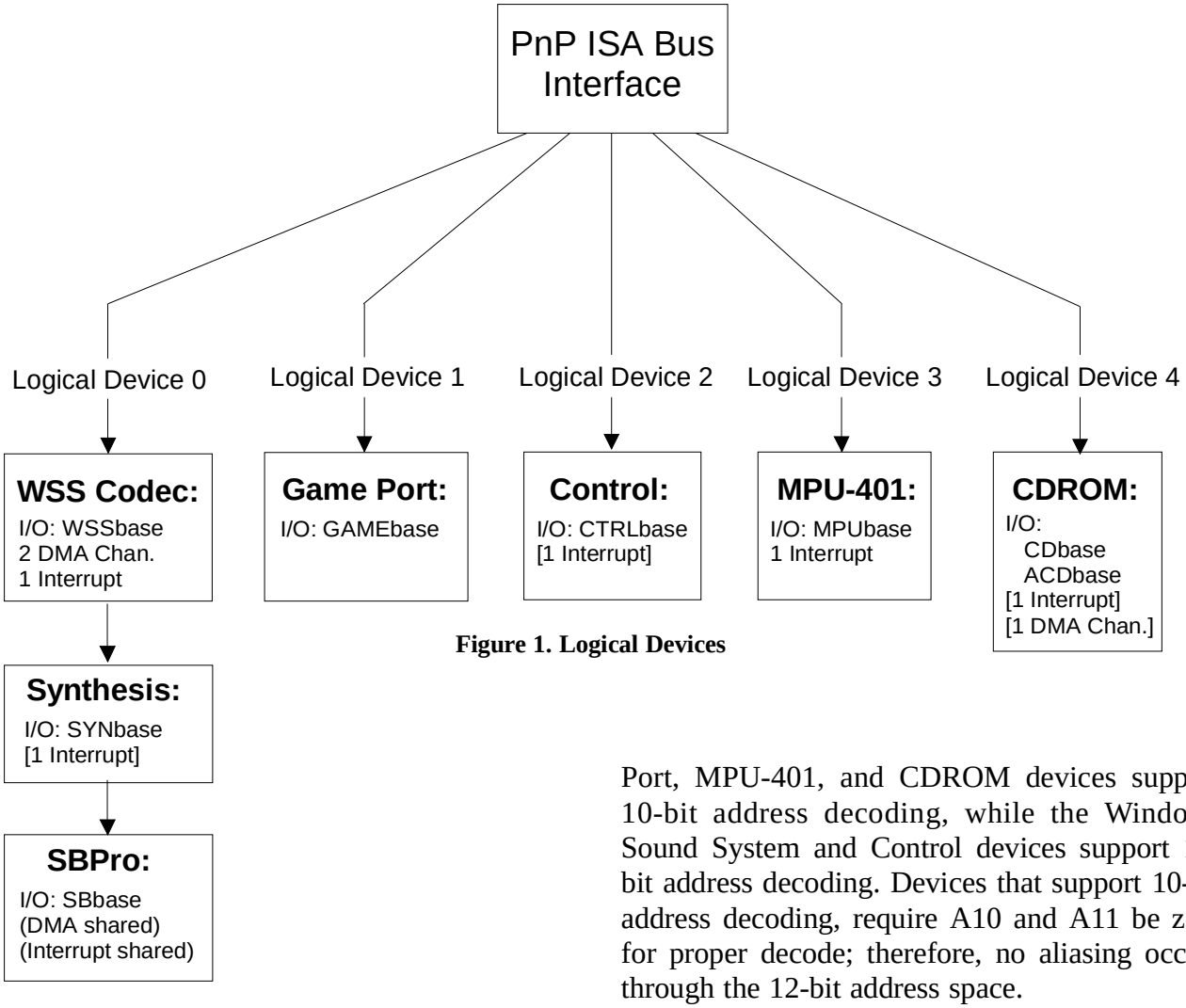


Figure 1. Logical Devices

I/O CYCLES

Every device that is enabled, requires I/O space. An I/O cycle begins when the part decodes a valid address on the bus while the DMA acknowledge signals are inactive and AEN is low. The $\overline{IOR}$ and $\overline{IOW}$ signals determine the direction of the data transfer. For read cycles, the part will drive data on the SD<7:0> lines while the host asserts the $\overline{IOR}$ strobe. Write cycles require the host to assert data on the SD<7:0> lines and strobe the $\overline{IOW}$ signal. Data is latched on the rising edge of the $\overline{IOW}$ strobe.

I/O ADDRESS DECODING

The logical devices use 10-bit or 12-bit address decoding. The Synthesizer, Sound Blaster, Game Port, MPU-401, and CDROM devices support 10-bit address decoding, while the Windows Sound System and Control devices support 12-bit address decoding. Devices that support 10-bit address decoding, require A10 and A11 be zero for proper decode; therefore, no aliasing occurs through the 12-bit address space.

To prevent aliasing into the upper address space, a "16-bit decode" option may be used, where the upper address bits SA12 through SA15 are connected to the part. SA12-SA15 are then decoded to be 0,0,0,0 for all logical device address decoding. When the upper address bits are used, the CDROM interface is no longer available since the upper address pins are multiplexed with the CDROM pins (See *Reset and Power Down* section). If the CDROM is needed, the circuit shown in Figure 2 can replace the SA12 through SA15 pins and provide the same functionality. Four cascaded OR gates, using a 74ALS32, can replace the ALS138 in Figure 2, but causes a greater delay in address decoding.

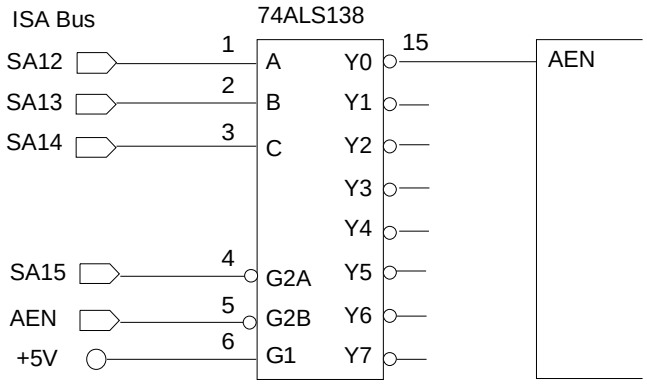


Figure 2. 16-bit Decode Circuit

DMA CYCLES

The part supports up to three 8-bit ISA-compatible DMA channels. The default hardware connections, which can be changed through the hardware configuration data, are:

DMA A = ISA DMA channel 0
DMA B = ISA DMA channel 1
DMA C = ISA DMA channel 3

The typical configuration would require two DMA channels. One for the WSS Codec and Sound Blaster playback, and the other for WSS Codec capture (to support full-duplex). The CDROM, if used, can also support a DMA channel, although this is not typical.

DMA cycles are distinguished from control register cycles by the generation of a DRQ (DMA Request). The host acknowledges the request by generating a $\overline{\text{DACK}}$ (DMA Acknowledge) signal. The transfer of audio data occurs during the $\overline{\text{DACK}}$ cycle. During the $\overline{\text{DACK}}$ cycle the address lines are ignored.

The digital audio data interface uses DMA request/grant pins to transfer the digital audio data between the part and the ISA bus. Upon receipt of a DMA request, the host processor responds with an acknowledge signal and a command strobe which transfers data to and from the part, eight bits at a time. The request pin stays active until the appropriate number of 8-bit cycles have occurred. The number of 8-bit transfers will vary depending on the digital audio data format, bit resolution, and operation mode.

The DMA request signal can be asserted at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs. A complete DMA cycle consists of one or more bytes depending on which device internal to the part is generating the request.

INTERRUPTS

For Plug-and-Play flexibility, seven interrupt pins are supported, although only one or two are typically used. The default hardware connections, which can be modified through the hardware configuration data, are:

IRQ A = ISA Interrupt 5
IRQ B = ISA Interrupt 7
IRQ C = ISA Interrupt 9
IRQ D = ISA Interrupt 11
IRQ E = ISA Interrupt 12
IRQ F = ISA Interrupt 15

IRQ G is new and defaults to not being connected for backwards compatibility. This new interrupt pin would typically be connected to ISA Interrupt 10. New designs that use IRQ G must change the Hardware Configuration Data to indicate which ISA Interrupt is connected to IRQ G.

The typical configuration would support two interrupt sources: one shared between the WSS Codec and the Sound Blaster Pro compatible devices, and the other for the MPU401 device. Interrupts are also supported for the FM Synthesizer, Control, and CDROM devices, but are typically not used.

PLUG AND PLAY

The Plug-and-Play (PnP) interface logic is compatible with the Intel/Microsoft Plug-and-Play specification, version 1.0a, for an ISA-bus device. Since the part is an ISA-bus device, it only supports ISA-compatible IRQs and DMA channels. Plug and Play compatibility allows the PC to automatically configure the part into the system upon power up. Plug and Play capability optimally resolves conflicts between Plug and Play and non-Plug and Play devices within the system. Alternatively, the PnP feature can be bypassed. See the *Bypassing PnP* section for more information. For a detailed Plug-and-Play protocol description, please refer to the *Plug and Play ISA Specification.*

To support Plug-and-Play in ISA systems that do not have a PnP BIOS or a PnP-aware operating system, the Configuration Manager (CM) TSR and an ISA Configuration Utility (ICU) from Intel Corp. are used to provide these functions. The CM isolates the cards, assigns Card Select Numbers, reads PnP card resource requirements, and allocates resources to the cards based on system resource availability. The ICU is used to keep the BIOS and the CM informed of the current system configuration. It also aids users in determining configurations for non-PnP ISA cards. A more thorough discussion of the Configuration Manager and the ISA Configuration Utility can be found in the *Product Development Information* document of the Plug and Play Kit by Intel Corp. In a PnP BIOS system, the BIOS is responsible for configuring all system board PnP devices. Some systems require additional software to aid the BIOS in configuring PnP ISA cards. The PnP BIOS can execute all PnP functions independently of the type of operating system. However, if a PnP aware operating system is present, the PnP responsibilities are shared between the BIOS and the operating system. For more information regarding PnP BIOS, please refer to the latest revision of the *Plug and Play BIOS Specification* published by Compaq Computer, Phoenix Technologies, and Intel.

The Plug and Play configuration sequence maps the various functional blocks of the part (logical devices) into the host system address space and configures both the DMA and interrupt channels. The host has access to the part via three 8-bit auto-configuration ports: Address port (0279h), Write Data port (0A79h), and relocatable Read Data port (020Bh - 03FFh). The read data port is relocated automatically by PnP software when a conflict occurs. Note that the Address Port can be moved for motherboard devices. See the *Address Port Configuration* section for more details.

The configuration sequence is as follows:

1. Host sends a software key which places all PnP cards in the sleep state (or Plug-and-Play mode).

2. The CS4239 is isolated from the system using an isolation sequence.

3. A unique identifier (handle) is assigned to the part and the resource data is read.

4. After all cards' resource requirements are determined, the host uses the handle to assign conflict-free resources

5. After the configuration registers have been programmed, each configured logical device is activated.

6. The part is then removed from Plug-and-Play mode.

Upon power-up, the chip is inactive and must be enabled via software. The CS4239 monitors writes to the Address Port . If the host sends a PnP initiation key, consisting of a series of 32 predefined byte writes, the hardware will detect

the key and place the part into the Plug-and-Play (PnP) mode. Another method to program the part is to use a special Crystal initiation key which functions like the PnP initiation key, but can be invoked by the user at any time. However, the Crystal Key only supports one Cirrus Audio part per system. The Crystal key and special commands are detailed in the *Crystal Key* and *Bypassing PnP* sections.

The isolation sequence uses a unique 72-bit serial identifier. The host performs 72 pairs of I/O read accesses to the Read Data port. The identifier determines what data is put on the data bus in response to those read accesses. When the isolation sequence is complete, the CM assigns a Card Select Number (CSN) to the part. This number distinguishes the CS4239 from the other PnP devices in the system. The Configuration Manager (CM) then reads the resource data from the CS4239. The 72-bit identifier and the resource data is either stored in an external user-programmable E^2PROM, or loaded via a "hostload" procedure from BIOS before PnP software is initiated.

The CM determines the necessary resource requirements for the system and then programs the part through the configuration registers. The configuration register data is written one logical device at a time. After all logical devices have been configured, CM activates each device individually. Each logical device is now available on the ISA bus and responds to the programmed address range, DMA channels, and interrupts that have been allocated to that logical device.

PnP Data

Hardware Configuration and Plug-and-Play resource data can be loaded into the part's RAM. The data may be stored in an external E^2PROM or may be downloaded from the host. Internal default PnP data is provided for motherboard designs.

To load the data, refer to the *Loading Resource Data* section. The following is the Plug-and-Play resource data:

The first nine bytes of the PnP resource data are the Plug-and-Play ID, which uniquely identifies the CS4239 from other PnP devices. The PnP ID is broken down as follows:

0Eh, 63h - Crystal ID - 'CSC' in compressed ASCII. (See the PnP Spec for more information)

42h - Oem ID. A unique Oem ID must be obtained from Cirrus for each unique Cirrus ISA Audio product used.

29h - Cirrus product ID for the CS4239

FFh, FFh, FFh, FFh - Serial number. This can be modified by each OEM to uniquely identify their card.

??h - Checksum.

Of the 9-byte serial number listed above, Cirrus software uses the first two bytes to indicate the presence of a Cirrus ISA Audio part, and the fourth byte, 0x29, to indicate the CS4239; therefore, these three bytes must not be altered. The part default in hex is 0E634236FFFFFFFFA9 for backwards compatibility.

The next 3 bytes are the PnP version number. The default is version 1.0a: 0Ah, 10h, 05h.

The next sequence of bytes are the ANSI identifier string. The default is: 82h, 0Eh, 00h, 'Crystal Codec', 00h.

The logical device data must be entered using the PnP ISA Specification format. Typical logical device values are found in Table 1. Internal default E^2PROM data is found in Appendix A.

Loading Resource Data

A serial E^2PROM interface allows user-programmable serial number and resource data to be stored in an external E^2PROM. The interface is compatible with devices from a number of ven-

dors and the size may vary according to specific customer requirements. The maximum size for resource data supported by the part's internal RAM is 384 bytes of combined Hardware Configuration and PnP resource data. With the addition of the 4-byte header, the maximum amount of E^2PROM space used would be 388 bytes. However, the part also supports firmware upgrades via the E^2PROM. To support firmware upgrades, the E^2PROM size must be greater than 770 bytes. After power-up, the existence of an E^2PROM is checked by reading the first two bytes from the E^2PROM interface. If the first two bytes from the E^2PROM port read 55h and BBh, then the rest of the E^2PROM data is loaded into the internal RAM. If the first two bytes aren't correct, the E^2PROM is assumed not to exist. For motherboard designs, internal default PnP data is provided or a Hostload sequence can be used to update the resource data. If the part is installed on a plug-in card, then an external E^2PROM is required to ensure that the proper PnP resource data is loaded into the internal RAM prior to a PnP sequence. See

Physical Device	Logical Device	Best Choice	Acceptable Choice 1	Sub optimal Choice 1	Sub optimal Choice 2
WSS	**0**	EISA ID = CSC0000		ANSI ID = WSS/SB	
16-bit address decode	WSSbase Length/Alignment	534h 4/4	534-FFC 4/4	534-FFCh 4/4	
high true edge sensitive	IRQ	5 (SB share)	5,7,9,11,12,15 (SB share)	5, 7, 9, 11, 12, 15 (SB share)	
8-bit, count by byte, type A	DMA0 (playback)	1 (SB share)	1, 3 (SB share)	0, 1, 3 (SB share)	
same	DMA1 (record)	0, 3	0, 1, 3	----	
Synthesis	**0**				
16-bit address decode	SYNbase Length/Alignment	388h 4/8	388h 4/8	388-3F8h 4/8	
	IRQ	----	----	----	
SB Pro	**0**				
16-bit address decode	SBbase Length/Alignment	220h 16/32	220-260h 16/32	220-300h 16/32	
Game Port	**1**	EISA ID = CSC0001		ANSI ID = GAME	
16-bit address decode	GAMEbase Length/Alignment	200h 8/8	208h 8/8		
Control	**2**	EISA ID = CSC0010		ANSI ID = CTRL	
16-bit address decode	CTRLbase Length/Alignment	120-FF8h 8/8			
	IRQ	----			
MPU401	**3**	EISA ID = CSC0003		ANSI ID = MPU	
16-bit address decode	MPUbase Length/Alignment	330h 2/8	330-360h 2/8	330-3E0h 2/8	
	IRQ	9	9,11,12,15	----	

---- Feature not supported in the listed configuration, but is supported through customization.

Table 1. Typical Motherboard Plug-and-Play Resource Data

the *External E²PROM* section for more information on the serial E²PROM interface and E²PROM programming.

The format for the data stored in the E²PROM is as follows:

2 bytes E²PROM validation: 55h, BBh

2 bytes length of resource data in E²PROM

19 bytes Hardware Configuration

9 bytes Plug and Play ID

3 bytes Plug and Play version number

Variable number of bytes of user defined ASCII ID string

Logical Device 0 (Windows Sound System, FM Synthesizer, Sound Blaster Pro) data

Logical Device 1 (Game Port) data

Logical Device 2 (Control) data

Logical Device 3 (MPU-401) data

Logical Device 4 (CD-ROM) data

End of Resource byte & checksum byte

Firmware patch code.

The default internal E²PROM data, in assembly format, can be found in Appendix A.

Loading Firmware Patch Data

An external E²PROM is read during the power-up sequence that stores Hardware Configuration and PnP data, and firmware patch data. The part contains RAM and ROM to run the core processor. The RAM allows updates to the core processor functionality. Placing the firmware patches in E²PROM, gives the maximum functionality at power-up without the need for a software driver.

The firmware patch data is typically included at the end of the PnP resource data. Cirrus provides a utility that will read in patch data from a file, and append it to the PnP resource data. The patch file must be obtained from Cirrus.

The Crystal Key

NOTE: The Crystal Key cannot differentiate between multiple Cirrus ISA Audio Codecs in a system; therefore, ONLY ONE CS4239 is allowed in systems using the Crystal Key. To allow multiple parts in a system, the Plug-and-Play isolation sequence must be used since it supports multiple parts via the serial identifier used in the isolation sequence. Crystal Key 2 is also designed to allow motherboard and add-in card chips to co-exist in a system.

The Crystal key places the part in the configuration mode. Once the Crystal key has been initiated, an alternate method of programming the configuration registers may be used. This alternate method is referred to as the "SLAM" method. The SLAM method allows the user to directly access the configuration registers, configure, and activate the chip, and then, optionally, disable the PnP and/or Crystal key feature. The SLAM method uses commands that are similar to the PnP commands; however, they are different since the user has direct access to the configuration registers. To use the SLAM method, see the *Bypassing PnP* section.

The following 32 bytes, in hex, are the Crystal key:

96, 35, 9A, CD, E6, F3, 79, BC,

5E, AF, 57, 2B, 15, 8A, C5, E2,

F1, F8, 7C, 3E, 9F, 4F, 27, 13,

09, 84, 42, A1, D0, 68, 34, 1A

Bypassing Plug and Play

The SLAM method allows the user to bypass the Plug and Play features and, as an option, allows the part to act like a non-Plug and Play or legacy device; however, the SLAM method only supports one Cirrus ISA Audio IC per system. The user directly programs the resources into the part, and then optionally disables the PnP and/or the Crystal Key, which forces the part to disregard any future PnP or Crystal initiation key sequences (All activated logical devices appear as legacy devices to PnP). The Crystal and PnP keys can also be disabled through the E^2PROM. The SLAM method uses the Address Port (AP) similarly to Plug-and-Play. Although the standard AP is 279h, two other selections are available for non-standard implementations. See the *Address Port Configuration* section for more details.

To use the SLAM method, the following sequence must be followed:

1. Host sends 32-byte Crystal key to the AP, chip enters configuration mode.

2. Host programs CSN (Card Select Number) by writing a 06h and 00h to the AP.

3. Host programs the configuration registers of each logical device by writing to the AP. The following data is the maximum amount of information per device. All current devices only need a subset of this data:
   Logical Device ID (15h, xxh)
   xxh is logical device number: 0-5

   I/O Port Base Address 0 (47h, xxh, xxh) high byte , low byte

   I/O Port Base Address 1 (48h, xxh, xxh) high byte , low byte

   I/O Port Base Address 2 (42h, xxh, xxh) high byte , low byte

   Interrupt Select 0 (22h, xxh)

   Interrupt Select 1 (27h, xxh)

   DMA Select 0 (2Ah, xxh)

   DMA Select 1 (25h, xxh)

   Activate Device (33h, 01h)
   (33h, 00h deactivates a device)

4. Repeat #3 for each logical device to be enabled. (Not all devices need be enabled.)

5. Host activates chip by writing a 79h to AP.

6. (Optional) Host disables PnP Key by writing a 55h to CTRLbase+5. The part will not participate in any future PnP cycles. The Crystal Key can also be disabled by writing a 56h to CTRLbase+5.

NOTE: To enable the PnP/Crystal Keys after they have been disabled by the SLAM method, bring the RESDRV pin to a logic high or remove power from the device.

The following illustrates typical data sent using the SLAM method.

```
006h, 001h          ; CSN=1

015h, 000h          ; LOGICAL DEVICE 0
047h, 005h, 034h    ; WSSbase = 0x534
048h, 003h, 088h    ; SYNbase = 0x388
042h, 002h, 020h    ; SBbase = 0x220
022h, 005h          ; WSS & SB IRQ = 5
02Ah, 001h          ; WSS & SB DMA0 = 1
025h, 003h          ; WSS capture DMA1 = 3
033h, 001h          ; activate logical device 0

015h, 001h          ; LOGICAL DEVICE 1
047h, 002h, 000h    ; GAMEbase = 0x200
033h, 001h          ; activate logical device 1
```

```
015h, 002h          ; LOGICAL DEVICE 2
047h, 001h, 020h    ; CTRLbase = 0x120
033h, 001h          ; activate logical device 2

015h, 003h          ; LOGICAL DEVICE 3
047h, 003h, 030h    ; MPUbase=0x330

022h, 009h          ; MPU IRQ = 9
033h, 001h          ; activate logical device 3

079h                ; activate CS4239 device
```

If all the above data is sent, after the Crystal key, all devices except the CDROM will respond to the appropriate resources given.

Crystal Key 2

A new feature of this part is the addition of another way to bypass the PnP interface using a new key, designated Crystal Key 2 (CK2). This new key is designed for Codecs on the motherboard that are hidden from normal PnP. The following 32 bytes, in hex, are Crystal Key 2 followed by the upper 8 bits of the Read Data port (RDP):

95, B1, D8, 6C, 36, 9B, 4D, A6,

D3, 69, B4, 5A, AD, D6, EB, 75,

BA, DD, EE, F7, 7B, 3D, 9E, CF,

67, 33, 19, 8C, 46, A3, 51, A8, <RDP>

This key differs greatly from the original Crystal Key in that the 33rd byte defines the upper 8 bits of the 10-bit Read Data port address, with the lower 2 bits equal to 11. As an example, if the RDP byte is 0x82, then the actual Read Data port is 0x20B. Another difference is that the original Crystal Key uses custom commands and is write-only; whereas, CK2 places the part in a PnP Configuration state and uses standard PnP commands to access PnP configuration registers. Since CK2 is unique to the CS4239, the PnP isolation sequence is bypassed.

CK2 differs from normal PnP in that the RDP is read/write instead of read-only. In PnP the RDP is read-only and a second address, designated the Write Data Port (0xA79), is used to write data into PnP registers. Using CK2, all configuration is done through the RDP, there is no Write Data Port. When finished, a Wait-for-Key command should be issued to the Address Port which places the part back in the normal mode of operation. Note that the Address Port (AP) can also be moved away from the normal PnP location of 0x279. See the *Address Port Configuration* section for more information.

The CK2 configuration sequence is as follows:

1. CK2 32 bytes are sent to the Address Port followed by the upper 8 bits of the RDP.

2. The AP and RDP are used to read/write configuration information in normal PnP fashion.

6. A Wait-for-Key command is sent removing the part from the configuration state.

The particluar PnP register is set using the Address Port and the data for that register is read/written to/from the RDP. As an example, when finished configuring the part, to send the Wait-for-Key command, a 0x02 is sent to the AP (selecting the Config. Control register) and a 0x02 is sent to the RDP. This causes the part to exit the configuration state and enter normal operation (Wait-for-Key).

Hardware Configuration Data

The Hardware Configuration data contains mapping information that links interrupt and DMA pins with actual interrupt numbers used by PnP and SLAM procedures. The Hardware Configuration data precedes the PnP Resource data.

The Hardware Configuration data is either 19 or 23 bytes long and contains the data necessary to configure the part. If an E^2PROM is not used

(Hostload), the first four bytes are not needed; therefore, the configuration data is only 19 bytes long. The configuration data maps the many functions of the logical devices to the physical pins of the chip. Table 2 lists the Hardware Configuration bytes. The detailed bit descriptions for each byte follows. While the reserved bits are listed as "res" in the bit position (and must always be written as 0), "rbc" is used for "reserved, backwards compatible" for bits that were used on previous chips, but are no longer required on this chip. These bits are read/writable but should generally be set to 0 for backwards compatibility.

BYTE	Default	Description
1	55h	E^2PROM validation byte 1. The first two bytes indicate that the E^2PROM exists.
2	BBh	E^2PROM validation byte 2
3	00h	High byte for length of data in E^2PROM
4	DDh	Low byte for length of data in E^2PROM
5	00h	Alternate CDROM (Logical Device 4), ACDbase, Address length mask
6	03h	RESERVED
7	80h	Misc. Configuration Bits: CDROM Interrupt Polarity, Key Disables, VCEN
8	00h	Global Configuration Byte: IFM, VCF1, WTEN
9	05h	Code Base Byte
10	20h	FM Volume Scaling
11*	04h	RESERVED - Must be 0x04
12*	08h	RESERVED - Must be 0x08
13*	10h	RESERVED - Must be 0x10
14	80h	Mono and DSP Port Control
15	00h	E^2PROM Checksum
16	00h	Global Configuration Byte 2: EECS, AUX1R, 3DEN, DSPD1, PSH
17	08h	CDROM (Logical Device 4), CDbase, Address length
18*	48h	RESERVED - Must be 0x48
19	75h	IRQ A/B Selection: Lower nibble = A, Upper nibble = B. Along with next two bytes - specify hardware interrupts tied to IRQA-IRQF pins
20	B9h	IRQ C/D Selection: Lower nibble = C, Upper nibble = D.
21	FCh	IRQ E/F Selection: Lower nibble = E, Upper nibble = F.
22	10h	DMA A/B Selection: Lower nibble = A, Upper nibble = B. This byte and the next byte specify hardware DRQ/DACKs tied to the DMAA-DMAC pins and the 7th IRQ pin - IRQ G
23	03h	DMA C/IRQ G Selection: Lower nibble = DMA C, Upper nibble = IRQ G

NOTE:The first four bytes are exclusive to the E^2PROM and are not used in the Hostload mode.
* Currently not supported. Must be set to default values given in the table.

Table 2. Hardware Configuration Data

HW Config. Byte 5: ACDbase Address Length Mask, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	CM2	CM1	CM0

CM2-CM0 — Address bit masks for the Alternate CDROM address decode, ACDbase. See the *CDROM Interface* section for more details on ACDbase

000 - $\overline{\text{ACDCS}}$ low for 1 byte
001 - $\overline{\text{ACDCS}}$ low for 2 bytes
011 - $\overline{\text{ACDCS}}$ low for 4 bytes
111 - ACDCS low for 8 bytes
xxx - all others, RESERVED

HW Config. Byte 7: Misc. Configuration Bits, Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
IHCD	rbc	PKD	CKD	CK2D	VCEN	rbc	rbc

VCEN — Volume Control Enable. When set, the UP, DOWN, and MUTE pins become active and provide a hardware master volume control.

CK2D — Crystal Key 2 disable. When set, blocks the part from receiving the 2nd Crystal key.

CKD — Crystal Key disable. When set, blocks the part from receiving the Crystal key.

PKD — PnP Key disable. When set, blocks the part from receiving the Plug-and-Play key.

IHCD — Interrupt High - CDROM. When set, CDINT is active high. When clear, CDINT is active low.

HW Config. Byte 8: Global Configuration Byte, Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
IFM	VCF1	rbc	res	WTEN	rbc	res	res

WTEN — Wave\table Serial Port Enable. When set, enables the CS9236 Single-Chip Wavetable Music Synthesizer serial port pins. This function is also available in C8. NOTE: The DSP SPE bit in I16 must be 0 for the wavetable port to function.

VCF1 — Hardware Volume Control Format. This bit controls the format of the hardware volume control pins UP, DOWN, and MUTE. The volume control is enabled by setting VCEN in the previous Hardware Configuration byte. VCF1 is also available through C8.

0 - $\overline{\text{MUTE}}$ is a momentary switch. MUTE toggles between mute and un-mute. Pressing the up or down switch always un-mutes.
1 - MUTE is not used. Two button volume control. Pressing the up and down buttons simultaneously causes the volume to mute. Pressing up or down un-mutes.

IFM — Internal FM. When set, the internal FM synthesizer is enabled. When clear, FM is disabled.

HW Config. Byte 9: Code Base Byte, Default = 00000101

D7	D6	D5	D4	D3	D2	D1	D0
CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0

CB7-CB0 — Code Base Byte. Determines the code base located in the E^2PROM. If not correct, the Firmware code after the PnP resource data is not loaded.

0x05 - CS4239 E^2PROM Load
0x06 - CS4239 Host Load

HW Config. Byte 10: FM Volume Scaling, Default = 00100000

D7	D6	D5	D4	D3	D2	D1	D0
res	FMS2	FMS1	FMS0	res	res	res	res

FMS2-FMS0 — FM Volume Scaling relative to wavetable digital input. These bits set the default FM volume level relative to the CS9236 wavetable interface port. Once initialized, these bits can be controlled through X19. These bits are provided for backwards compatibility with previous chips.

010 - 0 dB
011 - +6 dB
100 - -12 dB
101 - -6 dB
110 - +12 dB
111 - +18 dB

HW Config. Byte 14: Mono & DSP Port Control, Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
MIM	res	res	res	SF1	SF0	SPE	MIA

This register sets the power up defaults for these features. After power-up, I16 may be used to control the DSP serial port, and I26 may be used to control the Mono Input.

MIA — Mono Input Attenuate. When set, the MIN input is attenuated 9 dB. When clear, the MIN volume is 0 dB.

SPE — DSP Serial Port Enable. When set, the DSP serial port is enabled.

SF1,0 — DSP Serial Port Format. Selects the format of the serial port once enabled by SPE. See the *DSP Serial Audio Data Port* section for more details.

00 - 64-bit enhanced.
01 - 64-bit.
10 - 32 bit.
11 - ADC/DAC.

MIM — Mono In mute. When set, the MIN analog input is muted. When clear, MIN is mixed into the output mixer at a level set by MIA.

HW Config. Byte 15: E^2PROM Checksum Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

EC7-EC0 — E^2PROM checksum byte. Starts with the first byte of the size (after 55h/BBh) and ends with the last programmed byte of the E^2PROM. Only valid if EECS in Hardware Configuration Byte 16 is set.

HW Config. Byte 16: Global Config. Byte 2 Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
res	EECS	AUX1R	3DEN	DSPD1	PSH	ZVEN	res

This register sets the power up defaults for these features. After power-up, X18 may be used to control all bits except EECS.

ZVEN — ZVPORT Enable. When set, the ZVPORT pins are enabled and selected as input to DAC2. While the ZVPORT is enabled, no other input to DAC2 is allowed (synthesizers or DSP).

PSH — Playback Sample Hold. When set, the last sample is held in DAC1 when PEN is cleared. When clear, zero is sent to DAC1 when PEN is cleared.

DSPD1 — DSP port controls DAC1. When set, the serial DSP port controls DAC1 instead of the ISA playback FIFO.

3DEN — 3D Sound Enable. When set, 3D sound is enabled on L/ROUT.

AUX1R — AUX1 Remap. When set, writes to I18/19 (DAC2 volume) also control the AUX1 volume. When clear, I18/19 control DAC2 volume and I2/3 control AUX1 volume. This bit provides some backwards compatibil-

ity when AUX1 analog inputs are substituted for LINE analog inputs which are no longer available.

EECS — EEPROM Checksum. If set, indicates that Hardware Configuration Byte 15 is a checksum for the entire EEPROM (starting after 55h/BBh).

HW Config. Byte 17: CDbase Address Length, Default = 00000100

D7	D6	D5	D4	D3	D2	D1	D0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0

CAL7-CAL0 — CDbase Address Length. Determines the address length decode for the primary CDROM address, CDbase.

00000001 - $\overline{\text{CDCS}}$ low for 1 byte
00000010 - $\overline{\text{CDCS}}$ low for 2 bytes
00000100 - $\overline{\text{CDCS}}$ low for 4 bytes
00001000 - $\overline{\text{CDCS}}$ low for 8 bytes
00010000 - $\overline{\text{CDCS}}$ low for 16 bytes
00100000 - $\overline{\text{CDCS}}$ low for 32 bytes
01000000 - $\overline{\text{CDCS}}$ low for 64 bytes
10000000 - $\overline{\text{CDCS}}$ low for 128 bytes
xxx - all others, RESERVED

Bytes 19 through 21 map the interrupt number to the actual interrupt pins A - F. As shown in Table 2, the byte 20 default is 0xB9; therefore, IRQ C, which is the lower nibble, maps to the ISA interrupt 9. Likewise IRQ D, which is the upper nibble, maps to the ISA interrupt 11 (0Bh).

Byte 22 maps the DMA channel number to the actual DMA pins A and B. As shown in the table, the byte 22 default is 0x10; therefore, DRQA/$\overline{\text{DACKA}}$ is the lower nibble which maps to the ISA DMA channel 0. Likewise DRQB/$\overline{\text{DACKB}}$ is the upper nibble which maps to the ISA DMA channel 1.

Byte 23 maps DMA C and IRQ G. The lower nibble maps DMA C and defaults to DMA 3. The upper nibble supports the seventh IRQ, IRQ G. The default is disabled (0), providing backwards compatibility with other Cirrus ISA audio parts. If IRQ G is connected to an ISA interrupt (typically 10), then this byte must be modified to reflect the hardware connection.

Hostload Procedure

This procedure is provided for backwards compatibility with the CS4236. Since the E^2PROM allows all resource and firmware patch data to be loaded at power-up, this procedure is typically only used with motherboard devices that do not include an E^2PROM. To download PnP resource data from the host to the part's internal RAM, use the following sequence:

1. Configure Control I/O base address, CTRLbase, by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the CTRLbase, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, send the 32-byte Crystal key to I/O address port (AP).

      Second, configure logical device 2 base address, CTRLbase, by writing to AP (15h, 02h, 47h, xxh, xxh, 33h, 01h, 79h). Note: The two xxh represent the base_address_high and base_address_low respectively. The default is: 01h, 20h.

2. Write 57h (Jump to ROM) command to CTRLbase+5.

3. Download the PnP Resource data.

   a. Send download command by writing AAh to CTRLbase+5.

   b. Send starting download address (4000h) by writing low byte (00h) first, and then high byte (40h) to CTRLbase+5.

c. Send the Hardware Configuration and resource data in successive bytes to CTRLbase+5. This includes the Hardware Configuration and the PnP resource data. The PnP resource format is described in the *PnP Data* section. The resource header should not contain the first four bytes which are only used for E^2PROM loads.

d. End download by writing 00h to CTRLbase+6.

4. Download Firmware data. To download firmware data, contact Cirrus Logic for the ISA Audio BIOS kit.

5. If any of the Hardware Configuration Data (first 19 bytes) has changed, 5Ah must be written to CTRLbase+5 to force the part to internally update this information.

The new PnP data is loaded and the part is ready for the next PnP cycle.

External E^2PROM

The Plug and Play specification defines 32 bits of the 72-bit Serial Identifier as being a user defined serial number. The E^2PROM is used to change the user section of the identifier, store default resource data for PnP, Hardware Configuration data specific to the CS4239, and firmware patches to upgrade the core processor functionality.

The E^2PROM interface uses an industry standard 2-wire interface consisting of a bi-directional data line and a clock line driven from the part. After power-on the part looks for the existence of an E^2PROM device and loads the user defined data. The existence is determined by the first two bytes read (0x55 followed by 0xBB). If the first two bytes are correct, the part reads the next two bytes to determine the length of data in the E^2PROM. The length bytes indicate the number of bytes left to be read (not including the two validation bytes or two length bytes). As shown in Figure 3, the E^2PROM is read using a start bit followed by a dummy write, to initialize the address to zero. Then another start bit and device address, followed by all the data. Since the part uses the sequential read properties of the E^2PROM, only one E^2PROM, is supported (ganged E^2PROMs are not supported).

Some E^2PROMs that are compatible with this interface are:

Atmel	AT24Cxx series
MicroChip	24LCxxB series
National	NM24CxxL series
Ramtron	FM24Cxx series
SGS Thompson	ST24Cxx series
Xicor	X24Cxx series

where the xx is replaced by 02, 04, 08, or 16 based on the size of the E^2PROM desired. The size of 08 (1k bytes) is preferred since it allows the maximum flexibility for upgrading firmware patches. Other E^2PROMs compatible with Figure 3 and the timing parameters listed in the front of the data sheet may also be used.

The maximum Hardware Configuration and PnP resource RAM data supported is 384 bytes, and a four byte header; therefore, the maximum amount of data storage, without firmware patches, in E^2PROM would be 388 bytes. The maximum size E^2PROM needed is 770 bytes, to allow the inclusion of firmware patches after the PnP resource data.

If an external E^2PROM exists, it is accessed by the serial interface and is connected to the SDA and SCL pins. The two-wire interface is controlled by three bits in the Control logical device, Hardware Control Register (CTRLbase+1). The serial data can be written to or read from the E^2PROM by sequentially writing or reading that register. The three register bits, D0, D1, D2 are labeled CLK, DOUT, and DIN/EEN respectively. The DIN/EEN bit, when written to a one, enables the E^2PROM serial interface. When the DIN/EEN bit is written to a zero, the serial inter-

face is disabled. The DIN/EEN bit is also the Data In (DIN) signal to read back data from the E^2PROM. The SDA pin is a bi-directional open-drain data line supporting DIN and DOUT; therefore, to read the correct data, the DOUT bit must be set to a one prior to performing a read of the register. Otherwise, the data read back from DIN/EEN will be all zeros. The E^2PROM data can then be read from the DIN/EEN bit. The CLK bit timing is controlled by the host software. This is the serial clock for the E^2PROM output on the SCL pin. The DOUT bit is used to write/program the data out to the E^2PROM. An external pull-up resistor is required on SDA because it is an open-drain output. Use the guidelines in the specific E^2PROM data sheet to select the value of the pull-up resistor (a typical value would be 3.3 kΩ).

Programming the E^2PROM:

1. Configure Control I/O base address by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the logical device 2 I/O base address, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, write to the AP, send the 32-byte Crystal key.

      Second, configure the Control I/O base address by writing 15h, 02h, 47h, 01h, 20h, 33h, 01h, 79h to the AP.

2. Refer to the specific data sheet for the E^2PROM you are using for timing requirements and data format. Also, refer to the *Loading Resource Data* section of this data sheet for the E^2PROM resource data format.

3. Send the E^2PROM data in successive bits to CTRLbase+1 (Hardware Control Register) while following the E^2PROM data sheet format.

The E^2PROM now contains the PnP resource data. For this new data to take effect, the part must be reset, causing the part to read the E^2PROM during initialization. Cirrus can provide a utility, RESOURCE.EXE, to program E^2PROMs through the Control logical device interface.

WINDOWS SOUND SYSTEM CODEC

The WSS Codec software interface consists of 4 I/O locations starting at the Plug and Play address 'WSSbase', and supports 12-bit address decoding. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. The WSS Codec also requires one interrupt and one or preferably two DMA channels, one for playback and one for capture. Since the WSS Codec and Sound Blaster device are mutually exclusive, the two devices share the same interrupt and DMA playback channel.

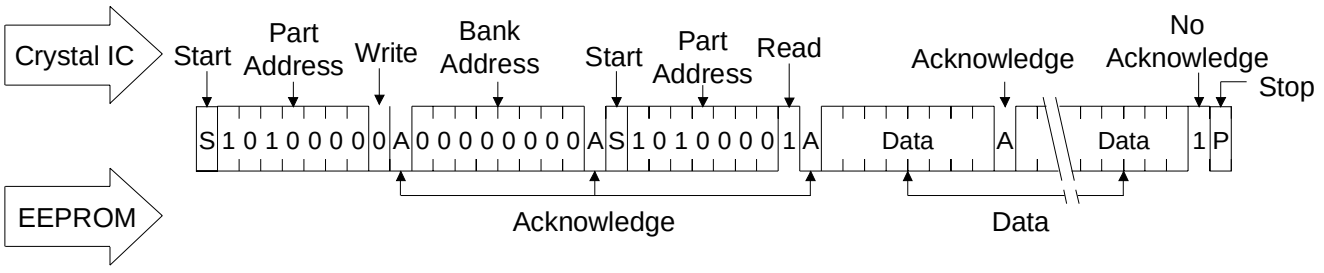


Figure 3. EEPROM Format

The WSS functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, simultaneous capture and playback (at independent sample frequencies) and a parallel bus interface.

Enhanced Functions (MODEs)

The initial state is labeled MODE 1 and forces the part to appear as a CS4248. The more popular second mode, MODE 2, forces the part to appear as a CS4231 super set and is compatible with the CS4232. To switch from MODE 1 to MODE 2, the CMS1,0 bits, in the MODE and ID register (I12), should be set to 10 respectively. When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, set the CMS1,0 bits to 00 and the part will resume operation in MODE 1. Except for the Capture Data Format (I28), Capture Base Count (I30/31), and Alternate Feature Status (I24) registers, all other Mode 2 functions retain their values when returning to Mode 1.

MODE 3 is selected by setting CMS1,0 to 11. MODE 3 allows access to a third set of "extended registers" which are designated X0-X31. The extended registers are accessed through I23. The additional MODE 3 functions are:

1. A full symmetrical mixer. This changes the input multiplexer to a input mixer.

2. Independent sample frequency control on the ADCs and DACs.

3. Programmable Gain and Attenuation on the Microphone inputs.

FIFOs

The WSS Codec contains 16-sample FIFOs in both the playback and capture digital audio data paths. The FIFOs are transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO starts to empty, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is clear) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling, thereby avoiding a loss of data in the audio data stream.

WSS Codec PIO Register Interface

Four I/O mapped locations are available for accessing the Codec functions and mixer. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{IOR}$ and $\overline{IOW}$ signals are used to define the read and write cycles respectively. A PIO access to the Codec begins when the host puts an address on to the ISA bus which matches WSSbase and drives AEN low. WSSbase is programmed during a Plug and Play configuration sequence. Once a valid base address has been decoded then the assertion of $\overline{IOR}$ will cause the WSS Codec to drive data on the ISA data bus lines. Write cycles require the host to assert data on the ISA data bus lines and strobe the $\overline{IOW}$ signal. The WSS Codec will latch data into the PIO register on the rising edge of the $\overline{IOW}$ strobe.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the WSS Codec and the bus. The WSS Codec is responsible for asserting a request signal whenever the Codec's internal buffers need updating. The bus responds with an acknowledge signal and strobes data to and from the Codec, 8 bits at a time. The WSS Codec keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Note that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle from the WSS Codec is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion of a DRQ followed by an acknowledgment by the host by the assertion of $\overline{\text{DACK}}$ (with AEN high). While the acknowledgment is received from the host, the WSS Codec assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines.

The WSS Codec may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs to the part. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If DRQ goes active while resetting PEN and/or CEN, the request must be acknowledged with $\overline{\text{DACK}}$ and a final sample transfer completed.

DMA CHANNEL MAPPING

Mapping of the WSS Codec's DRQ and $\overline{\text{DACK}}$ onto the ISA bus is accomplished by the Plug and Play configuration registers. If the Plug and Play resource data specifies only one DMA channel for the Codec (or the codec is placed in SDC mode) then both the playback and capture DMA requests should be routed to the same DRQ/$\overline{\text{DACK}}$ pair (DMA Channel Select 0). If the Plug and Play resource data specifies two DMA channels for the Codec, then the playback DMA request will be routed to the DMA pair specified by the DMA Channel Select 0 resource data, and the capture DMA requests will be routed to the DMA pair specified by the DMA Channel Select 1 resource data.

DUAL DMA CHANNEL MODE

The WSS Codec supports a single and a dual DMA channel mode. In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In dual DMA mode, SDC should be set to 0. The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

SINGLE DMA CHANNEL (SDC) MODE

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the WSS Codec will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the WSS Codec remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation; however, the capture audio channel is now diverted to the playback channel. Alternatively stated, the capture DMA request occurs on DMA channel select 0 for the WSS Codec. (In MODEs 2 and 3, the capture data format is al-

ways set in register I28.) If both playback and capture are enabled, the default will be playback. SDC does not have any affect when using PIO accesses.

Sound System Codec Register Interface

The Windows Sound System codec is mapped via four locations. The I/O base address, WSSbase, is determined by the Plug and Play configuration. The WSSbase supports four direct registers, shown in Table 3. The first two direct registers are used to access 32 indirect registers shown in Table 4. The Index Address register (WSSbase+0) points to the indirect register that is accessed through the Indexed Data register (WSSbase+1).

This section describes all the direct and indirect registers for the WSS Codec. Table 5 details a summary of each bit in each register with Tables 6 through 10 illustrating the majority of decoding needed when programming the WSS logical device, and are included for reference. When enabled, the WSS Codec default state is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Putting the part in MODE 2 or MODE 3, using CMS1,0 bits in the MODE and ID register (I12), allows access to indirect registers 16 through 31. Putting the part in MODE 3 also allows access to the extended registers through I23 and other extended features in the indirect registers.

Direct Registers: (R0-R3)

Address	Reg.	Register Name
WSSbase+0	R0	Index Address register
WSSbase+1	R1	Indexed Data register
WSSbase+2	R2	Status register
WSSbase+3	R3	PIO Data register

Table 3. WSS Codec Direct Register

Index	Register Name
I0	Left Analog Loopback
I1	Right Analog Loopback
I2	Left Aux #1 Volume
I3	Right Aux #1Volume
I4	Left Aux #2 Volume
I5	Right Aux #2 Volume
I6	Left DAC1 Volume
I7	Right DAC1 Volume
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID
I13	Reserved
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left DAC2 Volume
I19	Right DAC2 Volume
I20	Control/RAM Access
I21	RAM Access End
I22	Alternate Sample Frequency
I23	Extended Register Access (X regs)
I24	Alternate Feature Status
I25	Compatibility ID
I26	Mono Input Control
I27	Left Master Output Volume
I28	Capture Data Format
I29	Right Master Output Volume
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 4. WSS Codec Indirect Registers

DIRECT MAPPED REGISTERS

The first two WSS Codec registers provide indirect accessing to more codec registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the WSS Codec without using DMA cycles or indexing.

Note that register defaults are listed in binary form with reserved bits marked with 'x' to indicate unknown. Bits in the default marked with an 'e' indicate that the bit is initialized through E^2PROM. To maintain compatibility with future parts, these reserved bits must be written as 0, and must be masked off when the register is read. The current value read for reserved bits is not guaranteed on future revisions. While the reserved bits are listed as "res" in the bit position, "rbc" is used for "reserved, backwards compatible" for bits that were used on previous chips, but are no longer required on this chip. These bits are read/writable but should generally be set to 0 for backwards compatibility.

Index Address Register

(WSSbase+0, R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the indirect register accessed by the Indexed Data register (R1). These bits are read/write.

IA4 — Allows access to indirect registers 16 - 31. In MODE 1, this bit is reserved and must be written as zero.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the Status Register (R2) is set. Independent for playback and capture interrupts.

0 - Transfers Enabled (playback and capture DRQs occur uninhibited)
1 - Transfers Disabled (playback and capture DRQ only occur if INT bit is 0)

MCE — Mode Change Enable: This bit must be set whenever the current mode of the WSS Codec is changed. The Data Format (I8, I28) and Interface Configuration (I9) registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set.

INIT — WSS Codec Initialization: This bit is read as 1 when the Codec is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the WSS Codec has left the INIT state), the state of this register is: 010x0000 (binary - where 'x' indicates unknown).

During initialization and software power down (PDWN in CTRLbase+7), this register cannot be written and always reads 10000000 (80h)

Indexed Data Register

(WSSbase+1, R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 — Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

Status Register

(WSSbase+2, R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT

INT — Interrupt Status: This indicates the status of the internal interrupt logic of the WSS Codec. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin assigned to the WSS Codec.

Read States

0 - Interrupt inactive
1 - Interrupt active

PRDY — Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ — Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel.

0 - Right needed
1 - Left or Mono needed

PU/$\overline{L}$ — Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel.

0 - Lower needed
1 - Upper or 8-bit needed

SER — Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY — Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ — Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel.

0 - Right
1 - Left or Mono

CU/$\overline{L}$ — Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel.

0 - Lower available
1 - Upper or 8-bit available

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

I/O DATA REGISTERS

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

Capture I/O Data Register

(WSSbase+3, R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once the Status register (R2) is read and a new sample is received from the FIFO, the state machine and Status register (R2) will point to the first byte of the new sample.

During initialization and software power down of the WSS Codec, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register

WSSbase+3, R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset after the Status register (R2) is read, and the current sample is sent to the DACs via the FIFOs.

INDIRECT MAPPED REGISTERS

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). A detailed description of each indirect register is given below. All reserved bits should be written zero and may be 0 or 1 when read. Note that indirect registers 16-31 are not available when in MODE 1 (CMS1,0 in MODE and ID register I12 are both zero).

Left Analog Loopback (I0)

Default = 000xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	MGE	res	rbc	rbc	rbc	rbc

MGE This bit controls the 20 dB gain boost for the MIC analog input.

LSS1-LSS0 Left output loopback. Setting these bits to 11 enables the left output loopback into the input mixer. Bit combinations of 01, 10, and 00 disable the loopback.

Right Analog Loopback(I1)

Default = 000xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	MGE	res	rbc	rbc	rbc	rbc

MGE This bit is identical to the MGE bit in I0. It controls the 20 dB gain boost for the MIC analog input.

RSS1-RSS0 Right output loopback. Setting these bits to 11 enables the right output loopback into the input mixer. Other bit combinations disable the loopback.

Direct Registers: WSSbase (R0-R3)

ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
WSSbase+0	R0	INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0
WSSbase+1	R1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
WSSbase+2	R2	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
WSSbase+3	R3	CD7/PD7	CD6/PD6	CD5/PD5	CD4/PD4	CD3/PD3	CD2/PD2	CD1/PD1	CD0/PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	MGE	-	-	-	-	-
1	RSS1	RSS0	MGE	-	-	-	-	-
2	LX1OM	LX1IM	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1OM	RX1IM	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2OM	LX2IM	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2OM	RX2IM	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LD1OM	-	LD1A5	LD1A4	LD1A3	LD1A2	LD1A1	LD1A0
7	RD1OM	-	RD1A5	RD1A4	RD1A3	RD1A2	RD1A1	RD1A0
8 §	-	16B	-	S/$\overline{M}$	CFS2	CFS1	CFS0	C2SL
9 §	CPIO	PPIO	-	CAL1	CAL0	SDC	CEN	PEN
10	XCTL1	XCTL0	OSM1	OSM0	DEN	DTM	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	CMS1	CMS0	-	1	0	1	0
13	-	-	-	-	-	-	-	-
14	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16	-	-	CMCE	PMCE	SF1	SF0	SPE	DACZ
17	TEST	TEST	TEST	TEST	-	-	-	HPF
18	LD2OM	LD2IM	-	LD2A4	LD2A3	LD2A2	LD2A1	LD2A0
19	RD2OM	RD2IM	-	RD2A4	RD2A3	RD2A2	RD2A1	RD2A0
20	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
21	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
22	SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2
23	XA3	XA2	XA1	XA0	XRAE	XA4	-	-
24	-	-	CI	PI	CU	CO	PO	PU
25	0	0	0	0	0	0	1	1
26	MIM	-	-	-	MIA3	MIA2	MIA1	MIA0
27	LOM	LOS1	LOS0	LOG4	LOG3	LOG2	LOG1	LOG0
28	-	16B	-	S/$\overline{M}$	-	-	-	-
29	ROM	ROS1	ROS0	ROG4	ROG3	ROG2	ROG1	ROG0
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

Table 5. WSS Codec Direct & Indirect Register Bits

	A5	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.	.	.	.	.	.	.	.
8	0	0	1	0	0	0	-12.0 dB
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC1

CFS				
2	**1**	**0**	**C2SL = 0**	**C2SL=1**
0	0	0	8.0 kHz	5.51 kHz
0	0	1	16.0 kHz	11.025 kHz
0	1	0	27.42 kHz	18.9 kHz
0	1	1	32.0 kHz	22.05 kHz
1	0	0	N/A	37.8 kHz
1	0	1	N/A	44.1 kHz
1	1	0	48.0 kHz	33.075 kHz
1	1	1	9.6 kHz	6.62 kHz

Table 7. I8 Sample Frequency Selection

	G4	G3	G2	G1	G0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	muted

Table 8. AUX1, AUX2, DAC2

	G4	G3	G2	G1	G0	Master	MIC
0	0	0	0	0	0	6 dB	22.5 dB
1	0	0	0	0	1	4 dB	21.0 dB
2	0	0	0	1	0	2 dB	19.5 dB
3	0	0	0	1	1	***0 dB***	18.0 dB
4	0	0	1	0	0	-2 dB	16.5 dB
.	.	.	.	.	.	.	.
12	0	1	1	0	0	-18 dB	4.5 dB
13	0	1	1	0	1	-20 dB	3.0 dB
14	0	1	1	1	0	-22 dB	1.5 dB
15	0	1	1	1	1	-24 dB	***0 dB***
.	.	.	.	.	.	.	.
28	1	1	1	0	0	-50 dB	-19.5 dB
29	1	1	1	0	1	-52 dB	-21.0 dB
30	1	1	1	1	0	-54 dB	-22.5 dB
31	1	1	1	1	1	-56 dB	muted

Note: Master Volume also affected by L/RS1, L/RS0
Mic Volume assumes Boost is off (MBST = 0).

Table 9. Master and Microphone Volume

Decimal Value	ADC Fs (kHz)	ADC Divider	DAC Fs (kHz)	DAC Divider
0	50.40	16 X 21	50.40	16 X 21
1	48.00	353	48.00	353
2	32.00	529	32.00	529
3	27.42	617	27.42	617
4	16.00	1058	16.00	1058
5	9.600	1764	9.600	1764
6	8.000	2117	8.000	2117
7	6.620	2558	6.620	2558
8	50.40	16 X 21	50.40	16 X 21
.	.	.	.	.
21	50.40	16 X 21	50.40	16 X 21
22	48.10	16 X 22	48.10	16 X 22
23	46.01	16 X 23	46.01	16 X 23
24	44.10	16 X 24	44.10	16 X 24
25	42.36	16 X 25	42.36	16 X 25
26	40.70	16 X 26	40.70	16 X 26
.	.	.	.	.
189	5.600	16 X 189	5.600	16 X 189
190	5.570	16 X 190	5.570	16 X 190
191	5.541	16 X 191	5.541	16 X 191
192	5.512	16 X 192	5.512	16 X 192
193	5.512	16 X 192	5.483	16 X 193
194	5.512	16 X 192	5.455	16 X 194
.	.	.	.	.
255	5.512	16 X 192	4.150	16 X 255

Table 10. X12/13 Sample Frequency Selection

Left Auxiliary #1 Volume (I2)

Default = 11x00000

D7	D6	D5	D4	D3	D2	D1	D0
LX1OM	LX1IM	rbc	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

Note: Although this register generally controls the volume for LAUX1, the LAUX1 volume can be controlled through I18 by setting AUX1R in X18.

LX1G4-LX1G0 Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

LX1IM Left Auxiliary #1 Mute. When set, the left Auxiliary #1 input, LAUX1, to the input mixer is muted.

LX1OM Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the output mixer is muted.

Right Auxiliary #1 Volume (I3)

Default = 11x00000

D7	D6	D5	D4	D3	D2	D1	D0
RX1OM	RX1IM	rbc	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

Note: Although this register generally controls the volume for RAUX1, the RAUX1 volume can be control led through I19 by setting AUX1R in X18.

RX1G4-RX1G0 Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

RX1IM Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the input mixer is muted.

RX1OM Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the output mixer is muted.

Left Auxiliary #2 Volume (I4)

Default = 11x00000

D7	D6	D5	D4	D3	D2	D1	D0
LX2OM	LX2IM	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

LX2IM Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the input mixer is muted.

LX2OM Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the output mixer is muted.

Right Auxiliary #2 Volume (I5)

Default = 11x00000

D7	D6	D5	D4	D3	D2	D1	D0
RX2OM	RX2IM	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

RX2IM Right Auxiliary #2 Mute. When set, the right Auxiliary #2 input, RAUX2, to the input mixer is muted.

RX2OM Right Auxiliary #2 Mute. When set, the right Auxiliary #2 input, RAUX2, to the output mixer is muted.

Left DAC1 Volume (I6)

Default = 10000111

D7	D6	D5	D4	D3	D2	D1	D0
LD1OM	res	LD1A5	LD1A4	LD1A3	LD1A2	LD1A1	LD1A0

LD1A5-LD1A0 Left DAC1 Attenuation. The least significant bit represents -1.5 dB, with 000000 = 0 dB. The total range is 0 to -94.5 dB. See Table 6.

LD1OM Left DAC1 Output Mute. When set, the left DAC1 to the output mixer is muted.

Right DAC1 Volume (I7)

Default = 10000111

D7	D6	D5	D4	D3	D2	D1	D0
RD1OM	res	RD1A5	RD1A4	RD1A3	RD1A2	RD1A1	RD1A0

RD1A5-RD1A0 Right DAC1 Attenuation. The least significant bit represents -1.5 dB, with 000000 = 0 dB. The total range is 0 to -94.5 dB. See Table 6.

RD1OM Right DAC1 Mute. When set, the right DAC1 to the output mixer is muted.

Fs and Playback Data Format (I8)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
rbc	16B	rbc	S/$\overline{M}$	CFS2	CFS1	CFS0	C2SL

C2SL Clock 2 Source Select: This bit selects the clock base used for the audio sample rates for both capture and playback. Note that this bit can be disabled by setting SRE in I22 or by setting IFSE in X11.
CAUTION: C2SL can only be changed while MCE (R0) is set.

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock base (C2SL) is selected. Note that these bits can be disabled by setting SRE in I22 or IFSE in X11.
CAUTION: CFS2-CFS0 can only be changed while MCE (R0) is set.

DIVIDE	C2SL = 0	C2SL = 1
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODEs 2 and 3, this bit is only used for playback, and the capture format is independently selected via I28. MCE (R0) or P$\overline{M}$CE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

16B selects between 8-bit unsigned and 16-bit signed data for playback. The capture format is independently selected via register I28. MCE (R0) or PMCE (I16) must be set to modify the upper four bits of this register. See *Changing Audio Data Formats* section for more details.

0 - 8-bit unsigned data
1 - 16-bit signed data

Interface Configuration (I9)

Default = 00x00100

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	CAL1	CAL0	SDC	CEN	PEN

PEN Playback Enable. This bit enables playback. The WSS Codec will generate a DRQ and respond to DACK signal when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (playback DRQ and PIO inactive)
1 - Playback Enabled

CEN — Capture Enabled. This bit enables the capture of data. The WSS Codec will generate a DRQ and respond to DACK signal when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 - Capture Disabled (capture DRQ and PIO inactive)
1 - Capture Enabled

SDC — Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. This bit forces the WSS Codec to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the *DMA Interface* section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

CAL1,0 — Calibration: These bits determine which type of calibration the WSS Codec performs whenever the Mode Change Enable (MCE) bit, R0, changes from 1 to 0. The number of sample periods required for calibration is listed in parenthesis.

0 - No calibration (0)
1 - Converter calibration (321)
2 - DAC calibration (120)
3 - Full calibration (450)

PPIO — Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

CPIO — Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

Caution: This register, except bits CEN and PEN, can only be written while in Mode Change Enable (either MCE or PMCE). See the *Changing Sampling Rate* section for more details.

Pin Control (I10)

Default = 0000000x

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	OSM1	OSM0	DEN	DTM	IEN	res

IEN — Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

0 - Interrupt disabled
1 - Interrupt enabled

DTM — DMA Timing Mode. MODE 2 & 3 only. When set, causes the current DMA request signal to be deasserted on the rising edge of the IOW or IOR strobe during the next to last byte of a DMA transfer. When DTM = 0 the DMA request is released on the falling edge of the IOW or IOR during the last byte of a DMA transfer.

DEN — Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned data mode.

0 - Dither enabled
1 - Dither disabled

OSM1-OSM0 — These bits are enabled by setting SRE = 1 in I22. These bits in combination with DIV5-DIV0 and CS2 (I22) determine the current sample rate of the WSS Codec when SRE = 1. Note that these bits can be disabled by setting IFSE in X11.

00 - 12 kHz < Fs ≤ 24 kHz
01 - Fs > 24 kHz
10 - Fs ≤ 12 kHz
11 - reserved

XCTL1-XCTL0 XCTL Control: These bits are reflected on the XCTL1,0 pins of the part. NOTE: XCTL1 is multiplexed with other functions; therefore, it may not be available on a particular design.

0 - TTL logic low on XCTL1,0 pins
1 - TTL logic high on XCTL1,0 pins

Error Status and Initialization (I11, Read Only)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

ORR1-ORR0 Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS DRQ Status: This bit indicates the current status of the DRQs assigned to the WSS Codec.

0 - Capture AND Playback DRQs are presently inactive
1 - Capture OR Playback DRQs are presently active

ACI Auto-calibrate In-Progress: This bit indicates the state of calibration.

0 - Calibration not in progress
1 - Calibration is in progress

PUR Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and will not clear until the Status register (R2) is read.

COR Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and will not clear until the Status register (R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

MODE and ID (I12)

Default = 100x1010

D7	D6	D5	D4	D3	D2	D1	D0
1	CMS1	CMS0	res	1	0	1	0

res Reserved. Must write 0. Could read as 0 or 1.

CMS1,0 Codec Mode Select bits: Enables the Extended registers and functions of the part.

00 - MODE 1
01 - Reserved
10 - MODE 2
11 - MODE 3

Reserved (I13)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	res	rbc

rbc Reserved, backwards compatible.

res Reserved. Must write 0. Could read as 0 or 1.

Playback Upper Base (I14)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0 Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Playback Lower Base (I15)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0 Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Alternate Feature Enable I (I16)

Default = 0000eee0

D7	D6	D5	D4	D3	D2	D1	D0
rbc	res	CMCE	PMCE	SF1	SF0	SPE	DACZ

DACZ DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

1 - Go to center scale
0 - Hold previous valid sample

SPE DSP Serial Port Enable. When set, audio data from the ADCs is sent out SDOUT and audio data from SDIN is sent to the DACs. MCE in R0 must be set to change this bit. This bit is initialized through the Hardware Configuration data.

1 - Enable serial port
0 - Disable serial port.

SF1,SF0 DSP Serial Format. Selects the format of the serial port when enabled by SPE. MCE in R0 must be set to change these bits. These bits are initialized through the Hardware Configuration data.

0 - 64-bit enhanced. Figure 6.
1 - 64-bit. Figure 7.
2 - 32-bit. Figure 8.
3 - ADC/DAC. Figure 9.

PMCE Playback Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the playback channel, I8. MCE in R0 must be used to change the sample frequency.

CMCE Capture Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the capture channel, I28. MCE in R0 must be used to change the sample frequency in I8.

Alternate Feature Enable II (I17)

Default = 0000x000

D7	D6	D5	D4	D3	D2	D1	D0
TEST	TEST	TEST	TEST	rbc	res	rbc	HPF

HPF High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset to 0.

0 - disabled
1 - enabled

TEST — Factory Test. These bits are used for factory testing and must remain at 0 for normal operation.

Left DAC2 Volume (I18)

Default = 00000111

D7	D6	D5	D4	D3	D2	D1	D0
LD2OM	LD2IM	rbc	LD2A4	LD2A3	LD2A2	LD2A1	LD2A0

Note: When AUX1R in X18 is set, this register also controls the volume for the LAUX1 analog input. See I2 description for volume description of LAUX1.

LD2A4-LD2A0 — Left DAC2 Attenuation. The least significant bit represents 1.5 dB, with 01000 = 0 dB. The total range is +12 dB to -33.0 dB with 11111 = muted. See Table 8.

LD2IM — Left DAC2 Input Mute. When set, the left DAC2 to the input mixer is muted.

LD2OM — Left DAC2 Output Mute. When set, the left DAC2 to the output mixer is muted.

Right DAC2 Volume (I19)

Default = 11000111

D7	D6	D5	D4	D3	D2	D1	D0
RD2OM	RD2IM	rbc	RD2A4	RD2A3	RD2A2	RD2A1	RD2A0

Note: When AUX1R in X18 is set, this register also controls the volume for the RAUX1 analog input. See I3 description for volume description of RAUX1.

RD2A4-RD2A0 — Right DAC2 Attenuation. The least significant bit represents 1.5 dB, with 01000 = 0 dB. The total range is +12 dB to -33.0 dB with 11111 = muted. See Table 8.

RD2IM — Right DAC2 Input Mute. When set, the Right DAC2 to the input mixer is muted.

RD2OM — Right DAC2 Output Mute. When set, the right DAC2 to the output mixer is muted.

Control/RAM Access (I20)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

This register is identical to CTRLbase+5. For backwards compatibility, this register is not enabled until PAE in X18 is set. When PAE is clear, this register is read/writable, but does nothing.

CR7-CR0 — This register controls the loading of the part's internal RAM as well as internal processor commands. See the *Hostload Procedure* section as well as CTRLbase+5 register description for more details.

RAM Access End (I21)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

This register is identical to CTRLbase+6. For backwards compatibility, this register is not enabled until PAE in X18 is set. When PAE is clear, this register is read/writable, but does nothing.

RE7-RE0 — A 0 written to this location resets the previous location, I20, from data download mode, to command mode.

Alternate Sample Frequency Select (I22)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2

CS2 — Clock 2 Base Select. This bit selects the base clock frequency used for generating the audio sample rate. Note that the part uses only one crystal to generate both clock base frequencies. This bit can be disabled by setting IFSE in X11.

0 - 24.576 MHz base
1 - 16.9344 MHz base

DIV5 - DIV0 Clock Divider. These bits select the audio sample frequency for both capture and playback. These bits can be overridden by IFSE in X11.

Fs = (2*XT)/(M*N)

XT = 24.576 MHz CS2 = 0
XT = 16.9344 MHz CS2 = 1

N = DIV5-DIV0
16 ≤ N ≤ 49 for XT = 24.576 MHz
12 ≤ N ≤ 33 for XT = 16.9344 MHz

(M set by OSM1,0 in I10)
M = 64 for Fs > 24 kHz
M = 128 for 12 kHz < Fs ≤ 24 kHz
M = 256 for Fs ≤ 12 kHz

SRE Alternate Sample Rate Enable. When this bit is set to a one, bits 0-3 of I8 will be ignored, and the sample frequency is then determined by CS2, DIV5-DIV0, and the oversampling mode bits OSM1, OSM0 in I10. Note that this register can be overridden (disabled) by IFSE in X11.

Extended Register Access (I23)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
XA3	XA2	XA1	XA0	XRAE	XA4	res	rbc

XA4 Extended Register Address bit 4. Along with XA3-XA0, enables access to extended registers X16 through X31. MODE 3 only.

XRAE Extended Register Access Enable. Setting this bit converts this register from the extended address register to the extended data register. To convert back to an address register, R0 must be written. MODE 3 only.

XA3-XA0 Extended Register Address. Along with XA4, sets the register number (X0-X31) accessed when XRAE is set. MODE 3 only. See the *WSS Extended Register* section for more details.

Alternate Feature Status (I24)

Default = x0000000

D7	D6	D5	D4	D3	D2	D1	D0
res	rbc	CI	PI	CU	CO	PO	PU

PU Playback Underrun: When set, indicates the DAC has run out of data and a sample has been missed.

PO Playback Overrun: When set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO Capture Overrun: When set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case, this bit is set and the new sample is discarded.

CU Capture Underrun: Indicates the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI Playback Interrupt: Indicates an interrupt is pending from the playback DMA count registers.

CI Capture Interrupt: Indicates an interrupt is pending from the capture DMA count registers.

The PI and CI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

Compatibility ID (I25)

Default = 00000011

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

CID4-CID0 — Chip Identification. Distinguishes between this chip and previous codec chips that support this register set. This register is fixed to indicate code compatibility with the CS4236. X25 or C1 should be used to further differentiate between parts that are compatible with the CS4236.

All Chips:
00011 - CS4236, CS423xB, CS4239
00010 - CS4232/CS4232A
00000 - CS4231/CS4231A

V2-V0 — Version number. As enhancements are made to the part, the version number is changed so software can distinguish between the different versions.

000 - Compatible with the CS4236

These bits are fixed for compatibility with the CS4236. Register X25 or C1 may be used to differentiate between the CS4236 and newer chips.

Mono Input Control (I26)

Default = exxxeeee

D7	D6	D5	D4	D3	D2	D1	D0
MIM	rbc	rbc	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0 — Mono Input Attenuation. When MIM is 0, these bits set the level of MIN summed into the mixer. These bits are initialized through the Hardware Configuration data, Serial Port Control byte.

0000 = 0 dB.
0001-1111 = -9 dB

MIM — Mono Input Mute. In MODE 3, MIM mutes the MIN analog input to the left output mixer channel. MIMR in X4 mutes MIN analog input to the right output mixer channel. In MODE 2, MIM mutes both left and right channels. The mono input provides mix for the "beeper" function in most personal computers. This bit is initialized through the Hardware Configuration data, Serial Port Control byte.

0 - no mute
1 - muted

Left Master Output Volume (I27)

Default = 00100011

D7	D6	D5	D4	D3	D2	D1	D0
LOM	LOS1	LOS0	LOG4	LOG3	LOG2	LOG1	LOG0

When Hardware Volume is enabled, VCEN in C8 or X24 is set, this register will change based on external buttons.

LOG4-LOG0 — Left Output, LOUT, Master Gain. LOG0 is the least significant bit and represents -2 dB, with 00011 = 0 dB. The span is nominally +6 dB to -56 dB. See Table 9.

LOS1,0 — Left Output Mixer Select. These bits select and attenuation into the left output Master Gain stage, LOG4-0.

00 - -16 dB
01 - 0 dB
10 - -8 dB
11 - -24 dB

LOM — Left Output Mute. When set to 1, the left output, LOUT, is muted.

Capture Data Format (I28)

Default = x0x0xxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	16B	rbc	S/$\overline{M}$	res	res	res	res

S/$\overline{M}$ — Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel. MCE (R0) or C$\overline{M}$CE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

16B — selects between 8-bit unsigned and 16-bit signed data for capture. The capture data format can be different than the playback data format. MCE (R0) or CMCE (I16) must be set to modify this register. See *Changing Audio Data Formats* section for more details.

0 - 8-bit unsigned data
1 - 16-bit signed data

Right Master Output Volume (I29)

Default = 00100011

D7	D6	D5	D4	D3	D2	D1	D0
ROM	ROS1	ROS0	ROG4	ROG3	ROG2	ROG1	ROG0

When Hardware Volume is enabled, VCEN in C8 or X24 is set, this register will change based on external buttons.

ROG4-ROG0 — Right Output, ROUT, Master Gain. ROG0 is the least significant bit and represents -2 dB, with 00011 = 0 dB. The span is nominally +6 dB to -56 dB. See Table 9.

ROS1,0 — Right Output Mixer Select. These bits select and attenuation into the right output Master Gain stage, ROG4-0.

00 - -16 dB
01 - 0 dB
10 - -8 dB
11 - -24 dB

ROM — Right Output Mute. When set to 1, the right output, ROUT, is muted.

Capture Upper Base (I30)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 — Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

Capture Lower Base (I31)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

WSS EXTENDED REGISTERS

The Windows Sound System codec contains three sets of registers: R0-R3, I0-I31, and X0-X31. R0-R3 are directly mapped to the ISA bus through WSSbase+0 through WSSbase+3 respectively. R0 and R1 provide access to the indirect registers I0-I31. The third set of registers are extended registers X0-X31 that are indirectly mapped through the WSS register I23. I23 acts as both the extended address and extended data register. These extended registers are only available when in MODE 3.

Accessing the X registers requires writing the register address to I23 with XRAE set. When XRAE is set, I23 changes from an address register to a data register. Subsequent accesses to I23 access the extended data register. To convert I23 back to the extended address register, R0 must be written which internally clears XRAE. Assuming the part is in MODE 3, the following steps access the X registers:

1. Write 17h to R0 (to access I23).
   R1 is now the extended **address register**.
2. Write the desired X register address to R1 with XRAE = 1.
   R1 is now the extended **data register**.
3. Write/Read X register data from R1.

To read/write a different X register:

4. Write 17h to R0 again. (resets XRAE)
   R1 is now the extended **address register**.
5. Write the new X register address to R1 with XRAE = 1.
   R1 is now the new extended **data register**.
6. Read/Write new X register data from R1.

Address	Reg.	Register Name
WSSbase+0	R0	Reset Address
WSSbase+1	R1	Address/Data access
	I23	Indexed Address/Data

Extended Register Access (I23)

D7	D6	D5	D4	D3	D2	D1	D0
XA3	XA2	XA1	XA0	XRAE	XA4	res	rbc

Table 11. WSS Extended Register Control

Index	Register Name
X0	Reserved, backwards compatible
X1	Reserved, backwards compatible
X2	MIC Volume
X3	MIC Volume (same as X2)
X4	Synthesis and Input Mixer Control
X5	Right Input Mixer Control
X6	Left FM Synthesis Mute
X7	Right FM Synthesis Mute
X8	Left DSP Serial Port Mute
X9	Right DSP Serial Port Mute
X10	Reserved, backwards compatible
X11	DAC1 Mute and IFSE Enable
X12	Independent ADC Sample Freq.
X13	Independent DAC Sample Freq.
X14	Reserved, backwards compatible
X15	Reserved, backwards compatible
X16	Left Wavetable Serial Port Mute
X17	Right Wavetable Serial Port Mute
X18	3D Enable & RAM Port Enable
X19	FM Volume Scaling
X20	Reserved
X21	Reserved
X22	Reserved
X23	(C2) 3D Space Control
X24	(C8) Wavetable & Volume Control
X25	Chip Version and ID
X26	(Cb+0) Joystick Control
X27	(Cb+1) E^2PROM Interface
X28	(Cb+2) Power Down Control 1
X29	(C9) Power Down Control 2
X30	(Cb+7) Global Status
X31	Reserved

Table 12. WSS Extended Registers

Control Registers for the Extended Registers

ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
WSSbase+0	R0	INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0
WSSbase+1	R1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	I23	XA3	XA2	XA1	XA0	XRAE	XA4	-	-

Extended Registers: (X0-X31)

XA4 - XA0	D7	D6	D5	D4	D3	D2	D1	D0
X0	-	-	-	-	-	-	-	-
X1	-	-	-	-	-	-	-	-
X2	LMIM	LMOM	MBST	MG4	MG3	MG2	MG1	MG0
X3	RMIM	RMOM	MBST	MG4	MG3	MG2	MG1	MG0
X4	MIMR	LIS1	LIS0	IFM	-	-	-	-
X5	-	RIS1	RIS0	-	-	-	-	-
X6	LFMM	-	-	-	-	-	-	-
X7	RFMM	-	-	-	-	-	-	-
X8	LSPM	-	-	-	-	-	-	-
X9	RSPM	-	-	-	-	-	-	-
X10	-	-	-	-	-	-	-	-
X11	LD1IM	RD1IM	IFSE	-	-	-	-	-
X12	SRAD7	SRAD6	SRAD5	SRAD4	SRAD3	SRAD2	SRAD1	SRAD0
X13	SRDA7	SRDA6	SRDA5	SRDA4	SRDA3	SRDA2	SRDA1	SRDA0
X14	-	-	-	-	-	-	-	-
X15	-	-	-	-	-	-	-	-
X16	LWM	-	-	-	-	-	-	-
X17	RWM	-	-	-	-	-	-	-
X18	PAE	-	AUX1R	3DEN	DSPD1	PSH	ZVEN	DLEN
X19	-	FMS2	FMS1	FMS0	-	-	-	-
X20	-	-	-	-	-	-	-	-
X21	-	-	-	-	-	-	-	-
X22	-	-	-	-	-	-	-	-
X23 (C2)	SPC3	SPC2	SPC1	SPC0	-	-	-	-
X24 (C8)	VCIE	VCF1	-	-	WTEN	VCEN	DMCLK	BRES
X25	V2	V1	V0	CID4	CID3	CID2	CID1	CID0
X26 (Cb+0)	-	-	CONSW	-	-	-	JR1	JR0
X27 (Cb+1)	ICH	-	-	-	-	DIN/EEN	DOUT	CLK
X28 (Cb+2)	PDWN	SRC	VREF	MIX	ADC	DAC	PROC	FM
X29 (C9)	RESET	-	-	-	-	MIXCD	DAC2	SPORT
X30 (Cb+7)	CWSS	ICTRL	ISB	IWSS	IMPU	WDT	IMV	ZVA
X31	-	-	-	-	-	-	-	-

Table 13. Extended Register Bit Summary

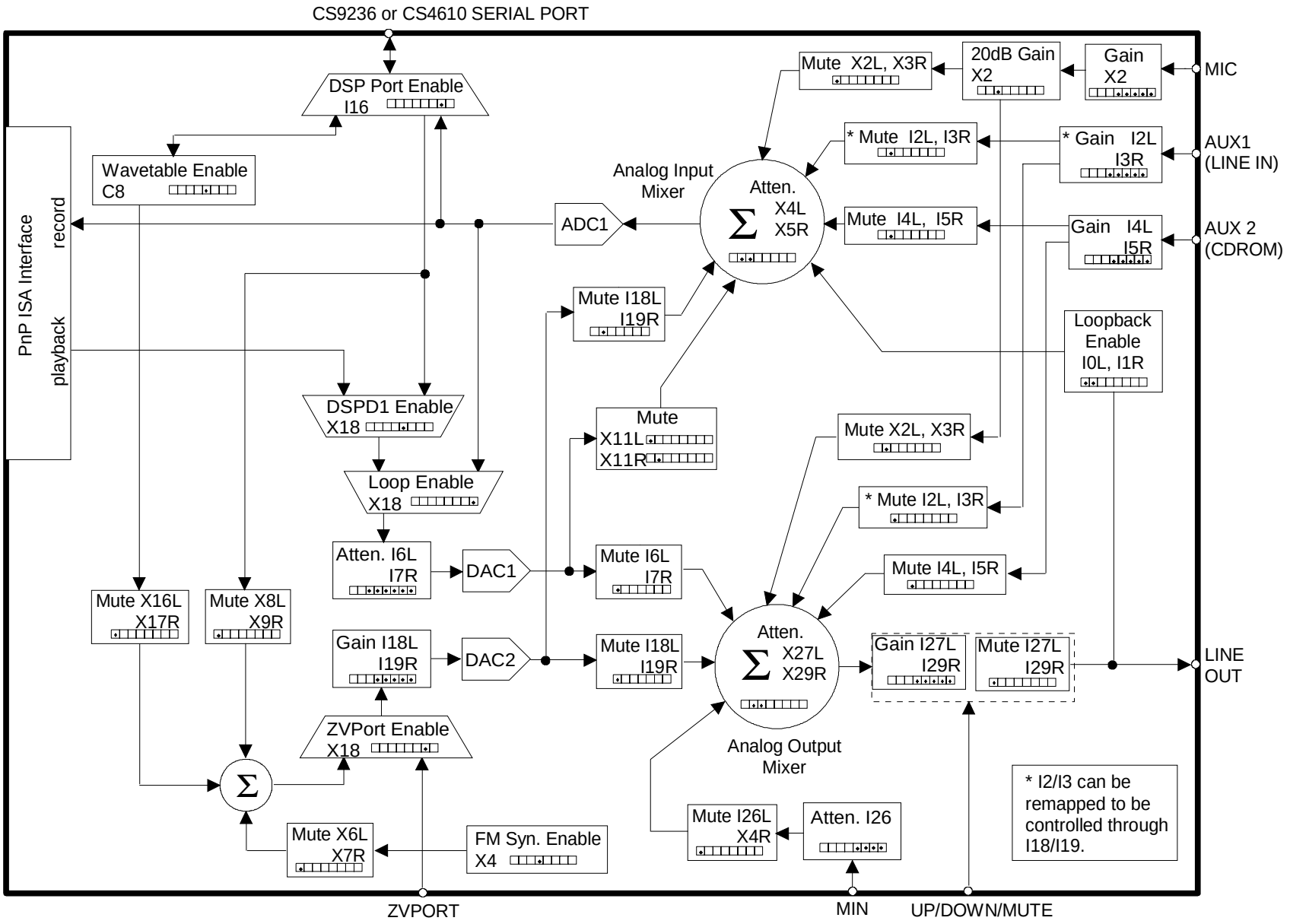


Figure 4. Mixer Block Diagram

Reserved (X0)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

Reserved (X1)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

MIC Volume (X2)

Default = 01011111

D7	D6	D5	D4	D3	D2	D1	D0
LMIM	LMOM	MBST	MG4	MG3	MG2	MG1	MG0

MG4-MG0 — Microphone Gain. The least significant bit represents 1.5 dB, where 01111 = 0 dB and 11110 = -22.5 dB. When all bits are 1, the Mic is muted with one exception. If MBST = 1 when going from 11110 to 11111, the Mic volume does not change. The attenuation steps are shown in Table 9.

MBST — Microphone 20 dB boost.
When set to 1, the MIC input is gained by 20 dB.

LMOM — Microphone Left Output Mixer Mute.
When set to 1, the signal to the left channel output mixer is muted.

LMIM — Microphone Left Input Mixer Mute.
When set to 1, the signal to the left channel input mixer is muted.

Right Channel MIC (X3)

Default = 01011111

D7	D6	D5	D4	D3	D2	D1	D0
RMIM	RMOM	MBST	MG4	MG3	MG2	MG1	MG0

MG4-MG0 — Microphone gain.
The least significant bit represents 1.5 dB, with 01111 = 0 dB. These are the same bits as in X2.
See Table 9.

MBST — Microphone 20 dB boost.
When set to 1, the MIC input is gained by 20 dB. This is the same bit as in X2.

RMOM — Microphone Right Output Mixer Mute.
When set to 1, the signal to the right channel output mixer is muted.

RMIM — Microphone Right Input Mixer Mute.
When set to 1, the signal to the right channel input mixer is muted.

Synthesis and Input Mixer Control (X4)

Default = e00exxxx

D7	D6	D5	D4	D3	D2	D1	D0
MIMR	LIS1	LIS0	IFM	rbc	rbc	res	res

IFM — Internal FM enable. When set to 1, the internal FM synthesis engine is enabled. This bit can be set through the Hardware Configuration data in the EEPROM.

LIS1-LIS0 — Left Input Mixer Summer Attenuator.
This attenuates the inputs to the left input mixer to enable overload protection when multiple input sources are utilized.

00 - 0 dB
01 - -6 dB
10 - -12 dB
11 - -18 dB

MIMR — Mono Input Mute to the Right Output mixer. When set to 1, the MIN signal to the right output mixer is muted. The default state of this bit is set by MIM in the Hardware Configuration Data, Mono & DSP Port byte.

Right Input Mixer Control (X5)

Default = x00xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	RIS1	RIS0	res	res	res	res	res

RIS1-RIS0 — Right Input Mixer Summer Attenuator. This attenuates the inputs to the right input mixer to enable overload protection when multiple input sources are utilized.

00 - 0 dB
01 - -6 dB
10 - -12 dB
11 - -18 dB

Left FM Synthesis Mute (X6)

Default = exxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LFMM	res	rbc	rbc	rbc	rbc	rbc	rbc

LFMM — Left FM mute. When set to 1, the left internal FM input to DAC2 is muted. The default state of this bit is the inverse of IFM in the Hardware Configuration Data, Global Configuration byte.

Right FM Synthesis Mute (X7)

Default = exxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RFMM	res	rbc	rbc	rbc	rbc	rbc	rbc

RFMM — Right FM mute. When set to 1, the right internal FM input to DAC2 is muted. The default state of this bit is the inverse of IFM in the Hardware Configuration Data, Global Configuration byte.

Left DSP Serial Port Mute (X8)

Default = exxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LSPM	res	rbc	rbc	rbc	rbc	rbc	rbc

LSPM — Left DSP Serial Port Mute. When set to 1, the Left DSP Serial Port input (SDIN) is muted. The default state of this bit is the inverse of SPE in the Hardware Configuration Data, Mono & DSP Port byte.

Right DSP Serial Port Mute (X9)

Default = exxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RSPM	res	rbc	rbc	rbc	rbc	rbc	rbc

RSPM — Right DSP Serial Port Mute. When set to 1, the Right DSP Serial Port input (SDIN) is muted. The default state of this bit is the inverse of SPE in the Hardware Configuration Data, Mono & DSP Port byte.

Reserved (X10)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	res	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

DAC1 Mute and IFSE Enable (X11)

Default = 110xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LD1IM	RD1IM	IFSE	res	res	res	res	res

IFSE — Independent Sample Freq. Enable. When set to 1, the extended registers X12 and X13 are used to set the sample rate, and registers I8, I10 (OSM1,0), and I22 are ignored. X12 and X13 cannot be modified unless this bit is set to 1.

RD1IM — Right DAC1 Input Mixer Mute. When set to 1, the output from the Right DAC1 is muted to the Right input mixer. See Figure 4.

LD1IM — Left DAC1 Input Mixer Mute. When set to 1, the output from the Left DAC1 is muted to the Left input mixer. See Figure 4.

Independent ADC Fs (X12)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
SRAD7	SRAD6	SRAD5	SRAD4	SRAD3	SRAD2	SRAD1	SRAD0

SRAD7-SRAD0 Sample Rate frequency select for the A/D converter. See Table 10.

Independent DAC Fs (X13)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
SRDA7	SRDA6	SRDA5	SRDA4	SRDA3	SRDA2	SRDA1	SRDA0

SRDA7-SRDA0 Sample Rate frequency select for the D/A converter. See Table 10.

Reserved, backwards compatible (X14)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

Reserved, backwards compatible (X15)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

Left Wavetable Serial Port Mute (X16)

Default = exxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LWM	res	rbc	rbc	rbc	rbc	rbc	rbc

LWM — Left Wavetable Serial Port Mute. When set, the Left Wavetable Serial Input to DAC2 is muted. The default state of this bit is the inverse of WTEN in the Hardware Configuration Data, Global Configuration byte.

Right Wavetable Serial Port Mute (X17)

Default = exxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RWM	res	rbc	rbc	rbc	rbc	rbc	rbc

RWM — Right Wavetable Serial Port Mute. When set, the Right Wavetable Serial Input to DAC2 is muted. The default state of this bit is the inverse of WTEN in the Hardware Configuration Data, Global Configuration byte.

3D and RAM Port Enable (X18)

Default = 0xeeeee0

D7	D6	D5	D4	D3	D2	D1	D0
PAE	res	AUX1R	3DEN	DSPD1	PSH	ZVEN	DLEN

DLEN — Digital Loopback Enable. When set, the input to DAC1 to comes from the ADCs. While DLEN is on, no other data is sent to DAC1. This provides a test path that is generally not used in normal operation.

ZVEN — ZVPORT Enable. When set, the ZVPORT pins are enabled and selected as input to DAC2. While the ZVPORT is enabled, no other input to DAC2 is allowed (synthesizers or DSP).

PSH — Playback Sample Hold. When set, the last sample is held in DAC1 when PEN is cleared. When clear, zero is sent to DAC1 when PEC is cleared.

DSPD1 — DSP port controls DAC1. When set, the serial DSP port controls DAC1 instead of the ISA playback FIFO.

3DEN — 3D Sound Enable. When set, 3D sound is enabled on L/ROUT. This bit is also controlled through C3.

AUX1R — AUX1 Remap. When set, writes to I18/19 (DAC2 volume) also control the AUX1 volume. When clear, I18/19 control DAC2 volume and I2/3 control AUX1 volume. This bit provides some backwards compatibil-

ity when AUX1 analog inputs are substituted for LINE analog inputs which are no longer available.

PAE — Processor Access Enable. When set, I20/21 provide access to the Processor identically to CTRLbase+5/+6 respectively.

FM Volume Scaling (X19)

Default = xeeexxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	FMS2	FMS1	FMS0	res	res	res	res

FMS2-FMS0 — FM Volume Scaling relative to wavetable digital input. These bits are provided for backwards compatibility with previous chips. These bits are initialized through Hardware Configuration data.

010 - 0 dB
011 - +6 dB
100 - -12 dB
101 - -6 dB
110 - +12 dB
111 - +18 dB

Reserved (X20)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

Reserved (X21)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

Reserved (X22)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

3D Space Control (X23)

Default = 0000xxxx

D7	D6	D5	D4	D3	D2	D1	D0
SPC3	SPC2	SPC1	SPC0	res	res	res	res

This register and C2 access the same data.

SPC3-SPC0 — Space control for 3D sound. Control's the "width" of the sound expansion with increasing numbers giving decreasing space affects. The least sigificant bit represents 1.5 dB of attenuation, with 0000 = 0 dB (full space affect).

CS9236 Wavetable Control (X24)

Default = 0exxee00

D7	D6	D5	D4	D3	D2	D1	D0
VCIE	VCF1	res	res	WTEN	VCEN	DMCLK	BRES

This register and C8 access the same data.

BRES — Force $\overline{\text{BRESET}}$ low. When set, the $\overline{\text{BRESET}}$ pin is forced low. Typically used for power management of peripheral devices.

DMCLK — Disable MCLK. When set, the MCLK pin of the CS9236 Wavetable Synthesizer serial interface is forced low providing a power savings mode.

VCEN — Volume Control Enable. When set, the UP, DOWN, and MUTE pins become active and provide hardware master volume control for the line outputs. Note that this bit can be initialized at power-up through Hardware Configuration data, Misc. Configuration Byte.

WTEN — Wavetable Serial Port Enable. When, set, the CS9236 Single-Chip Wavetable Music Synthesizer serial port pins are enabled. WTEN can be initialized in the E^2PROM Hardware Configuration data, Global Configuration byte.

VCF1 — Hardware Volume Control Format. This bit controls the format of the UP, DOWN, and MUTE pins. VCF1 is initialized in the E²PROM Hardware Configuration data, Global Configuration byte.

0 - MUTE is a momentary button. Pressing MUTE toggles between mute and un-mute. Pressing UP or DOWN will always un-mute.

1 - MUTE is not used. Pressing the up and down buttons simultaneously causes the volume to mute. Pressing up or down singularly will un-mute.

VCIE — Volume Control Interrupt Enable. When set, the hardware volume control pins cause interrupts, when pressed, on the WSSint pin. The status is available in CTRLbase+7, IMV bit. The IMV bit is cleared by reading CTRLbase+7.

Chip Version and ID (X25)

Default = 11011110

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

CID5-CID0 — Chip Identification. Distinguishes between this chip and other codec chips that support this register set. This register is identical to C1 and replaces the ID register in I25.

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V2-V0 — Version Number. As enhancements are made, the version number is changed so software can distinguish between the different versions of the same chip.

100 - Revision A
101 - Revision B
110 - Revision C

Joystick Control (X26)

Default = xx0x0x01

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	CONSW	rbc	ZERO	rbc	JR1	JR0

X26 and CTRLbase+0 access the same data with the exception that the XTAL bit in CTRLbase is replaced with ZERO in this register.

JR1,0 — Joystick rate control. Selects operating speed of the joystick (changes the trigger threshold for the X/Y coordinates).

00 - slowest speed
01 - medium slow speed
10 - medium fast speed
11 - fastest speed

ZERO — This bit MUST be written to 0. Writing this bit to 1 will disable all accesses to the WSS register space.

CONSW — controls host interrupt generation when a context switch occurs

0 - no interrupt on context switch
1 - Control interrupt generated on context switch

E²PROM Interface (X27)

CTRLbase+1, Default = 1xxxx000

D7	D6	D5	D4	D3	D2	D1	D0
ICH	rbc	rbc	rbc	rbc	DIN/ EEN	DOUT	CLK

X27 and CTRLbase+1 access the same data.

CLK — This bit is used to generate the clock for the Plug and Play E²PROM. EEN must be set to 1 to make this bit operational. A 1 sets the SCL pin high and a 0 sets the SCL pin low.

DOUT — This bit is used to output serial data to the Plug and Play E²PROM. EEN must be set to 1 to make this bit operational. A 0 causes SDA to go low. A 1 releases SDA (open-drain).

DIN/EEN — When read (DIN), this bit reflects the SDA pin, which should be serial data output from the Plug and Play E^2PROM. EEN and DOUT must be 1 for this bit to function.

When written (EEN), enables the E^2PROM interface: CLK and DOUT onto the SCL/SDA pins. Writing:

0 - E^2PROM interface disabled
1 - E^2PROM interface enabled

ICH — Interrupt polarity - CDROM. When set, the CDINT pin is an active high signal. When low, CDINT is an active low signal. This bits can be initialized through the Hardware Configuration data.

Block Power Down (X28)
Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PDWN	SRC	VREF	MIX	ADC1	DAC1	PROC	FM

This register and CTRLbase+2 access the same data. See CTRLbase+2 for a detailed description of each bit.

Power Management (X29)

Default = 0xxxx000

D7	D6	D5	D4	D3	D2	D1	D0
RESET	res	res	res	res	MIXCD	DAC2	SPORT

This register and C9 access the same data.

SPORT — Powers down the serial ports.

DAC2 — Powers down DAC2 including FM and the CS9236 serial interface.

MIXCD — Powers down the analog mixer - with the exception of MIN, AUX2, and the line outputs.

RESET — When this bit goes from a 1 to a 0, a software RESDRV is initiated causing the entire chip to be reset and placed in its default power-up configuration. Access to all registers on this chip will be lost, including this one, since the power-up state for PnP is all resources unassigned.

Global Status (X30)

CTRLbase+7, Default = 1000000

D7	D6	D5	D4	D3	D2	D1	D0
CWSS	ICTRL	ISB	IWSS	IMPU	WDT	IMV	ZVA

X30 and CTRLbase+7 access the same data.

ZVA — ZVPORT Active. When set, indicates that data is being received on the ZVPORT pins.

IMV — Hardware Master Volume Control Interrupt Status. A hardware volume control interrupt is pending when set to 1. Master Volume Interrupts are enabled through VCIE in C8/X24.

WDT — Watch-Dog Timer. If an error occurs on the ISA bus, the Processor will be reset and WDT will be set.

IMPU — MPU-401 Interrupt status. MPU interrupt pending when set to 1.

IWSS — Windows Sound System Interrupt Status. WSS interrupt pending when set to 1.

ISB — Sound Blaster Interrupt status. Sound Blaster interrupt pending when set to 1.

ICTRL — Control Logical Device 2 Interrupt status. A context switch interrupt is pending when set to 1.

CWSS — Context - WSS. Indicates the current context.

0 - Sound Blaster Emulation
1 - Windows Sound System

Reserved (X31)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

SOUND BLASTER INTERFACE

The Sound Blaster Pro compatible interface is the third physical device in logical device 0. Since the WSS Codec and the Sound Blaster are mutually exclusive, the WSS Codec interrupt and playback DMA channel are shared with the Sound Blaster interface.

Mode Switching

To facilitate switching between different functional modes (i.e. Sound Blaster and Windows Sound System), logic is included to handle the switch transparently to the host. No special software is required on the host side to perform the mode switch.

Sound Blaster Direct Register Interface

The Sound Blaster software interface utilizes 10-bit address decoding and is compatible with Sound Blaster and Sound Blaster Pro interfaces. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. This device requires 16 I/O locations located at the PnP address 'SBbase'. The following registers, shown in Table 14, are provided for Sound Blaster compatibility.

Left/Right FM Registers,
SBbase+0 - SBbase+3
These registers are mapped directly to the appropriate FM synthesizer registers.

Mixer Address Register,
SBbase+4, write only
This register is used to specify the index address for the mixer. This register must be written before any data is accessed from the mixer registers. The mixer indirect register map is shown in Table 15.

Mixer Data Register,
SBbase+5
This register provides read/write access to a particular mixer register depending on the index address specified in the Mixer Address Register.

Address	Description	Type
SBbase+0	Left FM Status Port	Read
SBbase+0	Left FM Register Status Port	Write
SBbase+1	Left FM Data Port	Write Only
SBbase+2	Right FM Status Port	Read
SBbase+2	Right FM Register Status Port	Write
SBbase+3	Right FM Status Port	Write Only
SBbase+4	Mixer Register Address	Write Only
SBbase+5	Mixer Data Port	Read/Write
SBbase+6	Reset	Write Only
SBbase+8	FM Status Port	Read Only
SBbase+8	FM Register port	Write
SBbase+9	FM Data Port	Write Only
SBbase+A	Read Data Port	Read Only
SBbase+C	Command/Write Data	Write
SBbase+C	Write Buffer Status (Bit 7)	Read
SBbase+E	Data Available Status (Bit 7)	Read

Table 14. Sound Blaster Pro Compatible I/O Interface

Reset
SBbase+6, write only
When bit D[0] of this register is set to a one and then set to a zero, a reset of the Sound Blaster interface will occur.

Read Data Port
SBbase+A, read only
When bit D[7] of the Data Available Register, SBbase+E, is set =1 then valid data is available in this register. The data may be the result of a Command that was previously written to the Command/Write Data Register or digital audio data.

Command/Write Data
SBbase+C, write only
The Command/Write Data register is used to send Sound Blaster Pro commands.

Write Buffer Status,
SBbase+C, read only
The Write Buffer Status register bit D[7] indicates when the SBPro interface is ready to accept another command to the Command/Write Data register. D[7]=1 indicates ready. D[7]=0 indicates not ready.

Sound Blaster Mixer Registers

The Sound Blaster mixer registers are shown in Table 15.

Reset Register,
Mixer Index 00H
Writing any value to this register will reset the mixer to default values.

Voice Volume Register,
Mixer Index 04H, Default = 99H
This register provides 8 steps of voice volume control each for the right and left channels.

Microphone Mixing Register,
Mixer Index 0AH, Default = 01H
This register provides 4 steps of microphone volume control.

Register	D7	D6	D5	D4	D3	D2	D1	D0
00H	DATA RESET							
02H	RESERVED							
04H	VOICE VOLUME LEFT				VOICE VOLUME RIGHT			
06H	RESERVED							
08H	RESERVED							
0AH	X	X	X	X	X	MIC MIXING		
0CH	X	X	X			INPUT SELECT		X
0EH	X	X	X	X	X	X	VSTC	X
20H	RESERVED							
22H	MASTER VOLUME LEFT				MASTER VOLUME RIGHT			
24H	RESERVED							
26H	FM VOLUME LEFT				FM VOLUME RIGHT			
28H	CD VOLUME LEFT				CD VOLUME RIGHT			
2AH	RESERVED							
2CH	RESERVED							
2EH	LINE VOLUME LEFT				LINE VOLUME RIGHT			

Table 15. SBPro Compatible Mixer Interface

Input Control Register,
Mixer Index 0CH
This register selects the input source to the ADC.

D2,D1 - 00 - Microphone
01 - CD Audio
10 - Microphone
11 - Line In

Output Control Register,
Mixer Index 0EH

VSTC - 0 - Mono Mode
1 - Stereo Mode

Master Volume Register,
Mixer Index 22H, Default = 99H
This register provides 8 steps of master volume control each for the right and left channels.

FM Volume Register,
Mixer Index 26H, Default = 99H
This register provides 8 steps of FM volume control each for the right and left channels.

CD Volume Register,
Mixer Index 28H, Default = 01H
This register provides 8 steps of CD volume control each for the right and left channels.

Line-In Volume Register,
Mixer Index 2EH, Default = 01H
This register provides 8 steps of line-in volume control each for the right and left channels.

GAME PORT INTERFACE

The Game Port logical device software interface utilizes 10-bit address decoding and is located at PnP address 'GAMEbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. For backwards compatibility, the Game Port consists of 8 I/O locations which alias to the same location, consisting of one read and one write register.

Plug and Play configuration capability will allow the joystick I/O base address, GAMEbase, to be located anywhere within the host I/O address space. Currently most games software assume that the joystick I/O port is located at 200h.

A write to the GAMEbase register triggers four timers. A read from the same register returns four status bits corresponding to the joystick fire buttons and four bits that correspond to the output from the four timers.

A button value of 0 indicates the button is pressed or active. The button default state is 1. When GAMEbase is written, the X/Y timer bits go high. Once GAMEbase is written, each timer output remains high for a period of time determined by the current joystick position. The number in parenthesis below is the joystick connector pin number.

GAMEbase+0 - GAMEbase+7

D7	D6	D5	D4	D3	D2	D1	D0
JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JACX Joystick A, Coordinate X (pin 3)

JACY Joystick A, Coordinate Y (pin 6)

JBCX Joystick B, Coordinate X (pin 11)

JBCY Joystick B, Coordinate Y (pin 13)

JAB1 Joystick A, Button 1 (pin 2)

JAB2 Joystick A, Button 2 (pin 7)

JBB1 Joystick B, Button 1 (pin 10)

JBB2 Joystick B, Button 2 (pin 14)

Two bits, JR1 and JR0, are located in the Control register space (CTRLbase+0) for defining the speed of the Game Port Interface. Four different rates are software selectable for use with various joysticks and to support older software timing loops with aliasing (roll-over) problems.

The Game Port hardware interface consists of 8 pins that connect directly to the standard game port connector. Buttons must have a 1000 pF capacitor to ground and have internal 20 kΩ pullups resistors. X/Y coordinates must have a 5.6 nF capacitor to ground and a 2.2 kΩ series resistor to the appropriate joystick connector pin. Figure 5 illustrates the schematic to the joystick connector.

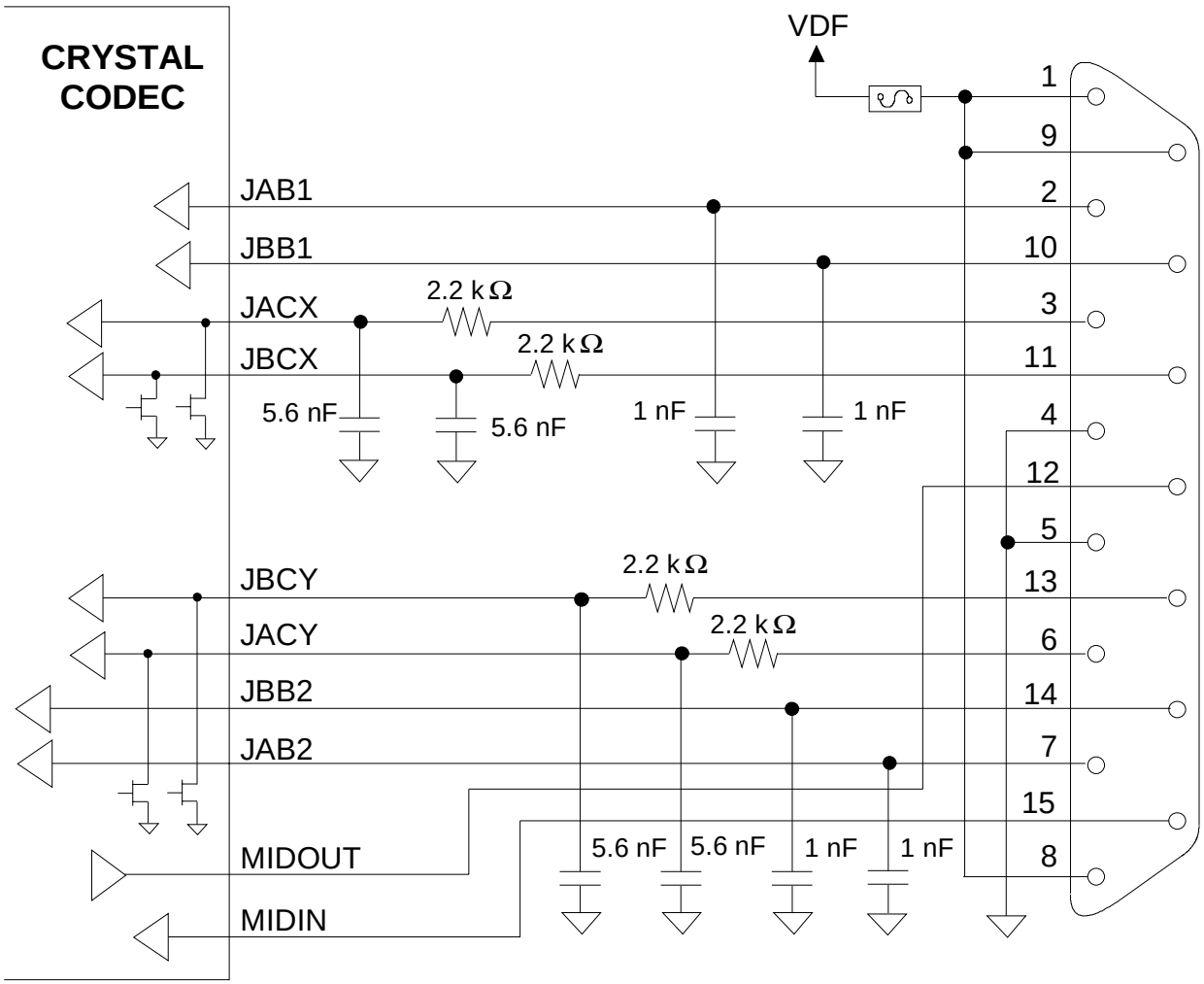


Figure 5. Joystick Logic

CONTROL INTERFACE

The Control logical device includes registers for controlling various functions of the part that are not included in the other logical device blocks. These functions include game port rate control and programmable power management, as well as extra mixing functions.

Control Register Interface

The Control logical device software interface occupies 8 I/O locations, utilizes 12-bit address decoding, and is located at PnP address 'CTRLbase'. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. This device can also support an interrupt. Table 16 lists the eight Control registers.

Address	Register
CTRLbase+0	Joystick Control
CTRLbase+1	E^2PROM Interface
CTRLbase+2	Block Power Down
CTRLbase+3	Control Indirect Address Reg.
CTRLbase+4	Control Indirect Data Register
CTRLbase+5	Control/RAM Access
CTRLbase+6	RAM Access End
CTRLbase+7	Global Status

Table 16. Control Logical Device Registers

Joystick Control
CTRLbase + 0, Default = xx0x0x01

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	CONSW	rbc	XTAL	rbc	JR1	JR0

JR1,0 — Joystick rate control. Selects operating speed of the joystick (changes the trigger threshold for the X/Y coordinates).

00 - slowest speed
01 - medium slow speed
10 - medium fast speed
11 - fastest speed

XTAL — Crystal Oscillator disable. When set, all functions are disabled except access to this register. All registers retain their values in this power-down mode.

CONSW — controls host interrupt generation when a context switch occurs

0 - no interrupt on context switch
1 - Control interrupt generated on context switch

E^2PROM Interface
CTRLbase+1, Default = 1xxxx000

D7	D6	D5	D4	D3	D2	D1	D0
ICH	rbc	rbc	rbc	rbc	DIN/ EEN	DOUT	CLK

CLK — This bit is used to generate the clock for the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational. A 1 sets the SCL pin high and a 0 sets the SCL pin low.

DOUT — This bit is used to output serial data to the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational. A 0 causes SDA to go low. A 1 releases SDA (open-drain).

DIN/EEN — When read (DIN), this bit reflects the SDA pin, which should be serial data output from the Plug and Play E^2PROM. EEN and DOUT must be 1 for this bit to function.

When written (EEN), enables the E^2PROM interface: CLK and DOUT onto the SCL/SDA pins. Writing:

0 - E^2PROM interface disabled
1 - E^2PROM interface enabled

ICH — Interrupt polarity - CDROM. When set, the CDINT pin is an active high signal. When low, CDINT is an active low signal. This bits can be initialized through the Hardware Configuration data.

Block Power Down

CTRLbase+2, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PDWN	SRC	VREF	MIX	ADC1	DAC1	PROC	FM

FM — Internal FM synthesizer powered down when set.

PROC — Processor set to idle mode. When set, places the internal processor in an idle state. This effects the PnP interface, MPU401, and SBPro devices. Any command to any one of these interfaces will cause the processor to go active.

DAC1 — DAC1 power down. When set, powers down DAC1. Playback is disabled.

ADC1 — ADC1 power down. When set, powers down the ADC1. Capture is disabled.

MIX — Mixer power down. All analog input and output channels are powered down. All outputs are centered around VREF if the VREF bit is set. A reset is not required to maintain the calibrated state if the mixer is powered down but the VREF bit is not set.

VREF — VREF power down. When set, powers down the entire mixer. Since powering down VREF, powers down the entire analog section, some audible pops can occur.

SRC — Internal Sample-Rate Converters are powered down. Only 44.1 kHz sample frequency is allowed when this bit is set.

PDWN — Global Power Down with data retention. When set, the entire chip is powered down, except reads and writes to this register. When this bit is cleared, a full calibration is initiated. All registers retain their values; therefore, normal operation can resume after calibration is completed.

NOTE: Software should mute the DACs and Mixers and FM volume when asserting any power-down modes to prevent clicks and pops.

Control Indirect Address Register

CTRLbase+3

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	CA3	CA2	CA1	CA0

CA3-CA0 — Address bits to access the Control Indirect registers C0-C9 through CTRLbase+4

Control Indirect Data Register

CTRLbase+4

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 — Control Indirect Data register. This register provides access to the indirect registers C0-C9, where CTRLbase+3 selects the actual register. See the *Control Indirect Register* section for more details.

Control/RAM Access

CTRLbase+5

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

CR7-CR0 — This register controls the loading of the part's internal RAM. RAM support includes hardware configuration and PnP default resource data, as well as program memory. See the *Hostload Procedure* section for more information. Commands are followed by address and data information.

Commands:

0x55 - Disable PnP Key

0x56 - Disable Crystal Key

0x53 - Disable Crystal Key 2

0x5A - Update Hardware Configuration Data.

0xAA - Download RAM. Address followed by data. (Stopped by writing 0 to CTRLbase+6)

RAM Access End

CTRLbase+6

D7	D6	D5	D4	D3	D2	D1	D0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

RE7-RE0 A 0 written to this location resets the previous location, CTRLbase+5, from data download mode to command mode.

Global Status

CTRLbase+7, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CWSS	ICTRL	ISB	IWSS	IMPU	WDT	IMV	ZVA

ZVA ZVPORT Active. When set, indicates that data is being received on the ZVPORT pins.

IMV Hardware Master Volume Control Interrupt Status. When set, hardware volume has changed. IMV is cleared by reading this status register. Master Volume Interrupts are enabled through VCIE in C8.

WDT Watch-Dog Timer. If an error occurs on the ISA bus, the Processor will be reset and WDT will be set.

IMPU MPU-401 Interrupt status. MPU interrupt pending when set to 1.

IWSS Windows Sound System Interrupt Status. WSS interrupt pending when set to 1.

ISB Sound Blaster Interrupt status. Sound Blaster interrupt pending when set to 1.

ICTRL Control Logical Device 2 Interrupt status. A context switch interrupt is pending when set to 1.

CWSS Context - WSS. Indicates the current context.

0 - Sound Blaster Emulation
1 - Windows Sound System

Control Indirect Registers

The Control Indirect registers are accessed through CTRLbase+3 and CTRLbase+4. CTRLbase+3 is the address register and CTRLbase+4 is the data register used to access C0 through C9 indirect registers.

Reserved (C0)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	res	res	res	res	rbc	rbc	rbc

rbc Reserved, backwards compatible.

Address	Register Name
CTRLbase+3	Control Indirect Address
CTRLbase+4	Control Indirect Data

Table 17. Control Indirect Access Registers

Index	Register Name
C0	Reserved
C1	Version / Chip ID
C2	3D Space Control
C3	3D Enable
C4	Reserved
C5	Reserved
C6	Reserved
C7	Reserved
C8	Wavetable & Volume Control
C9	Power Management

Table 18. Control Indirect Registers

Version / Chip ID (C1)

Default = 11011110

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

CID4-CID0 — Chip Identification. Distinguishes between this chip and other codec chips that support this register set. This register is identical to the WSS X25 register.

11110 - CS4239

V2-V0 — Version number. As enhancements are made, the version number is changed so software can distinguish between the different versions of the same chip.

100 - Revision A
101 - Revision B
110 - Revision C

3D Space Control (C2)

Default = 0000xxxx

D7	D6	D5	D4	D3	D2	D1	D0
SPC3	SPC2	SPC1	SPC0	rbc	rbc	rbc	rbc

SPC3-SPC0 — Space control for 3D sound. Control's the "width" of the sound expansion with increasing numbers giving decreasing space affects. The least sigificant bit represents 1.5 dB of attenuation, with 0000 = 0 dB (full space affect).

3D Enable (C3)

Default = xxxexxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	3DEN	res	res	res	res

3DEN — Enable 3D Sound. When set, 3D sound expansion is enabled on the analog outputs with the amount of 3D enhancement controlled through C2.

Reserved (C4)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	res	res	res	res

rbc — Reserved, backwards compatible.

Reserved (C5)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

Reserved (C6)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
rbc	rbc	rbc	rbc	rbc	rbc	rbc	rbc

rbc — Reserved, backwards compatible.

Reserved (C7)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Wavetable & Volume Control (C8)

Default = 0exxee00

D7	D6	D5	D4	D3	D2	D1	D0
VCIE	VCF1	res	res	WTEN	VCEN	DMCLK	BRES

BRES — Force BRESET low. When set, the BRESET pin is forced low. Typically used for power management of peripheral devices.

DMCLK — Disable MCLK. When set, the MCLK pin of the CS9236 Wavetable Synthesizer serial interface is forced low providing a power savings mode.

VCEN — Volume Control Enable. When set, the UP, DOWN, and MUTE pins become active and provide hardware master volume control for the line outputs. Note that this bit can be initialized at power-up through Hardware Configuration data, Misc. Configuration Byte.

WTEN — Wavetable Serial Port Enable. When, set, the CS9236 Single-Chip Wavetable Music Synthesizer serial port pins are enabled. WTEN can be initialized in the E^2PROM Hardware Configuration data, Global Configuration byte.

VCF1 — Hardware Volume Control Format. This bit controls the format of the UP, DOWN, and MUTE pins. VCF1 is initialized in the E^2PROM Hardware Configuration data, Global Configuration byte.

0 - MUTE is a momentary button. Pressing MUTE toggles between mute and un-mute. Pressing UP or DOWN will always un-mute.

1 - MUTE is not used. Pressing the up and down buttons simultaneously causes the volume to mute. Pressing up or down singularly will un-mute.

VCIE — Volume Control Interrupt Enable. When set, the hardware volume control pins cause interrupts, when pressed, on the WSSint pin. The status is available in CTRLbase+7, IMV bit.

Power Management (C9)

Default = 0xxxx000

D7	D6	D5	D4	D3	D2	D1	D0
RESET	res	res	res	res	MIXCD	DAC2	SPORT

SPORT — Powers down the serial ports.

DAC2 — Powers down DAC2 including FM and the CS9236 serial interface.

MIXCD — Powers down the analog mixer - with the exception of MIN, AUX2, and the line outputs.

RESET — When this bit goes from a 1 to a 0, a software RESDRV is initiated causing the entire chip to be reset and placed in its default power-up configuration. Access to all registers on this chip will be lost, including this one, since the power-up state for PnP is all resources unassigned.

MPU-401 INTERFACE

The MPU-401 is an intelligent MIDI interface that was introduced by Roland in 1984. Voyetra Technologies subsequently introduced an IBM-PC plug in card that incorporated the MPU-401 functionality. The MPU-401 has become the de-facto standard for controlling MIDI devices via IBM-PC compatible personal computers.

Although the MPU-401 does have some intelligence, a non-intelligent mode is available in which the MPU-401 operates as a basic UART.

By incorporating hardware to emulate the MPU-401 in UART mode, MIDI capability is supported.

MPU-401 Register Interface

The MPU401 logical device software interface occupies 2 I/O locations, utilizes 10-bit address decoding, and is located at PnP address 'MPUbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. The standard base address is 330h. This device also uses an interrupt, typically 9.

MPUbase+0 is the MIDI Transmit/Receive port and MPUbase+1 is the Command/Status port. In addition to I/O decodes the only additional functionality required from an ISA bus viewpoint is the generation of a hardware interrupt whenever data has been received into the receive buffer.

MIDI Transmit/Receive Port, MPUbase+0

D7	D6	D5	D4	D3	D2	D1	D0
TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

TR7-TR0 — The MIDI Transmit/Receive Port is used to send and receive MIDI data as well as status information that was returned from a previously sent command.

All MIDI transmit data is transferred through a 16-byte FIFO and receive data through a 16-byte FIFO. The FIFO gives the ISA interface time to respond to the asynchronous MIDI transfer rate of 31.25 k baud.

The Command/Status Registers occupy the same address and are used to send instructions to and receive status information from the MPU-401.

Command Register, write only MPUbase+1

D7	D6	D5	D4	D3	D2	D1	D0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CS7-CS0 — Each write to the Command/Status Register produces an appropriate acknowledge byte in the receive register.

Status Register, read only MPUbase+1

D7	D6	D5	D4	D3	D2	D1	D0
RXS	TXS	CS5	CS4	CS3	CS2	CS1	CS0

CS5-CS1 — D0-D5 are the 6 LSBs of the last command written to this port.

TXS — Transmit Buffer Status Flag.

0 - Transmit buffer not full
1 - Transmit buffer full

RXS — Receive Buffer Status Flag

0 - Data in Receive buffer
1 - Receive buffer empty

When in "UART" mode, data is received into the receive buffer FIFO and a hardware interrupt is generated. Data can be received from two sources: MIDI data via the UART serial input or acknowledge data that is the result of a write to the Command Register (MPUbase+1). The interrupt is cleared by a read of the MIDI Receive Port (MPUbase+0).

MIDI UART

The UART is used to convert parallel data to the serial data required by MIDI. The serial data rate is fixed at 31.25 k baud (±1%). The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit.

In multimedia systems, the MIDI pins are typically connected to the joystick connector as illustrated in Figure 5.

MPU-401 "UART" Mode Operation

After power-up reset, the interface is in "non-UART" mode. Non-UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are ignored.

2. All reads of the Receive Port, MPUbase+0, return the last received buffer data.

3. All writes to the Command Port, MPUbase+1, are monitored and acknowledged as follows:
   a. A write of 3Fh sets the interface into UART operating mode. An acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.
   b. A write of A0-A7, ABh, ACh, ADh, AFh places an FEh into the receive buffer FIFO (which generates an interrupt) followed by a one byte write to the receive buffer FIFO of 00h for A0-A7, and ABh commands, 15h for ACh, 01h for ADh, and 64h for AFh commands.
   c. All other writes to the Command Port are ignored and an acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.

UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the next byte is read from the buffer and sent out the MIDOUT pin. The Status Register, MPUbase+1, bit 6, TXS is updated to reflect the transmit buffer FIFO status.

2. All reads of the Receive Port, MPUbase+0, return the next byte in the receive buffer FIFO. When serial data is received from the MIDIN pin, it is placed in the next receive buffer FIFO location. If the buffer is full, the last location is overwritten with the new data. The Status Register, MPUbase+1, bit 7, RXS is updated to reflect the new receive buffer FIFO state.

3. A write to the Command Register, MPUbase+1, of FFh will return the interface to non-UART mode.

4. All other writes to the Command Register, MPUbase+1, are ignored.

FM SYNTHESIZER

This part contains a games-compatible internal FM synthesizer. When enabled, this internal FM synthesis engine responds to both the SBPro FM synthesis addresses as well as the SYNbase addresses.

To enable the internal FM synthesis engine, the IFM bit in the Hardware Configuration data, byte 8 (Global Configuration Byte) must be set. This bit is also available in WSS register X4.

Volume control for the internal FM synthesizer is supported through I18 and I19 in the WSS extended register space.

The synthesizer interface is compatible with the Adlib and Sound Blaster standards. The typical Adlib I/O address is SYNbase = 388h.

Standard Synthesizer I/O Map

Address	Name	Type
SYNbase+0	FM Status	Read Only
SYNbase+0	FM Address 0	Write Only
SYNbase+1	FM Data 0	Read/Write
SYNbase+2	FM Address 1	Write Only
SYNbase+3	FM Data 1	Read/Write

CDROM INTERFACE

An IDE CDROM controller interface is provided that supports Enhanced as well as Legacy IDE CDROM drives. This interface includes two programmable chip selects and on-chip hardware to map DMA and interrupt signals to the ISA bus. Use of the CDROM interface requires an external 1k E^2PROM to support PnP, Hardware Configuration, and firmware patch data.

There are five pins that make up the CDROM interface which consist of:

$\overline{\text{CDCS}}$ - chip select, COMbase address
CDINT - interrupt, COMint
CDRQ - DMA request, COMdma
$\overline{\text{CDACK}}$ - DMA acknowledge, COMdma
$\overline{\text{ACDCS}}$ - alternate chip select, ACDbase

The four basic CDROM interface pins are multifunction pins that default to the upper address bits SA12 - SA15. To use the pins as a CDROM interface, a 10 kΩ pulldown resistor must be placed on MCLK.

The fifth CDROM pin $\overline{\text{ACDCS}}$ is multiplexed with XCTL1/SINT/$\overline{\text{DOWN}}$. This chip select supports the alternate CDROM chip select used for status. The volume control pin $\overline{\text{DOWN}}$ has the highest precedence; therefore, the VCEN bit must be zero to use this pin for the CDROM interface. Given that VCEN is zero, a 10 kΩ pulldown resistor on SDOUT converts this pin to $\overline{\text{ACDCS}}$. The range of addresses that $\overline{\text{ACDCS}}$ will respond to is programmable via the Hardware Configuration data, byte 5, from one to eight bytes (default = 1 byte).

To make the CDROM interface more flexible, one global bit, located in the Hardware Configuration data section - byte 7, allow control over the polarity of the CDROM interrupt pin CDINT. IHC defaults to 1 indicating that CDINT is an active high interrupt. IHC is also controllable through CTRLbase+1.

CS4610 DSP SERIAL DATA PORT

The WSS Codec includes a CS4610 DSP serial audio interface for transferring digital audio data between the part and the CS4610 DC '97 Audio Accelerator serial device. When SPE is set (MCE must be 1 to change SPE), the serial port pins are enabled; otherwise, they are high-impedance pins.

The DSP audio serial port is software enabled via the SPE bit in the WSS Codec indirect register I16 or from the Hardware Configuration data in the EEPROM. The ISA interface is fully active in this mode. The serial port data format is always two's complement 16-bit linear.

FSYNC and SCLK are always output from the part when the serial port is enabled. The serial port can be configured in one of four serial port formats, shown in Figures 6-9. SF1 and SF0 in I16 select the particular format. MCE in R0 must be set to change SF1/0. Both left and right audio words are always 16 bit two's complement. When the mono audio format is selected, the right channel output is set to zero and the left channel input is sent to both DAC channels.

The first format - SPF0, shown in Figure 6, is called 64-bit enhanced. This format has 64 SCLKs per frame with a one bit period wide FSYNC that precedes the frame. The first 16 bits occupy the left word and the second 16 bits oc-

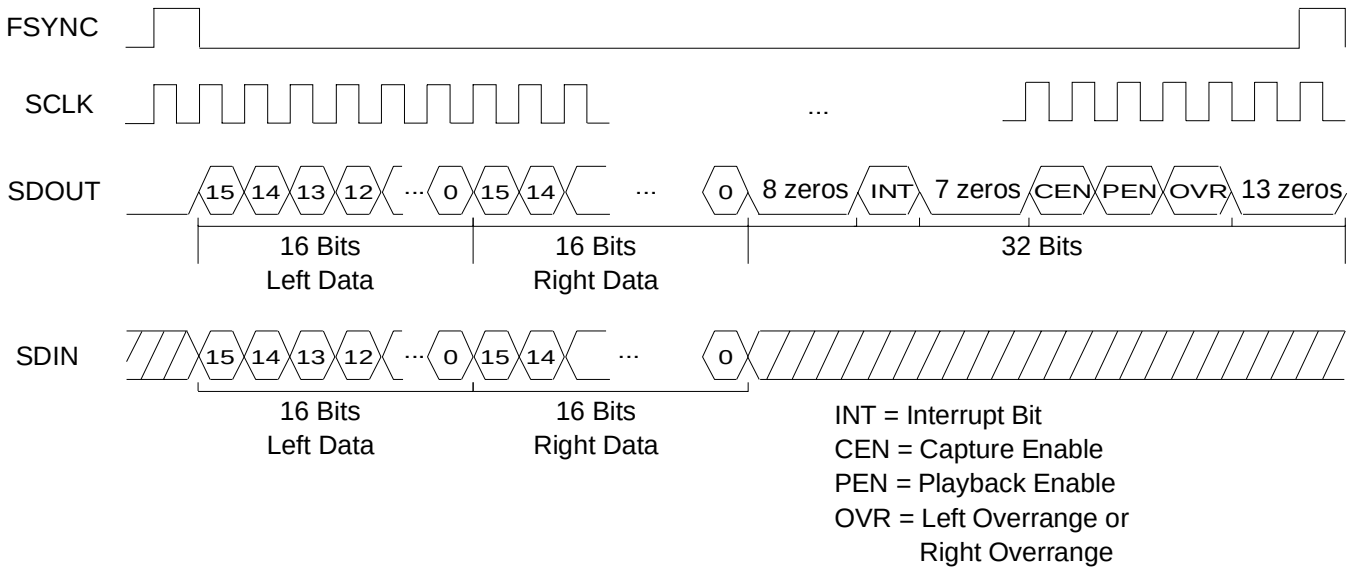


Figure 6. 64-bit Enhanced Mode (SF1,0 = 00)

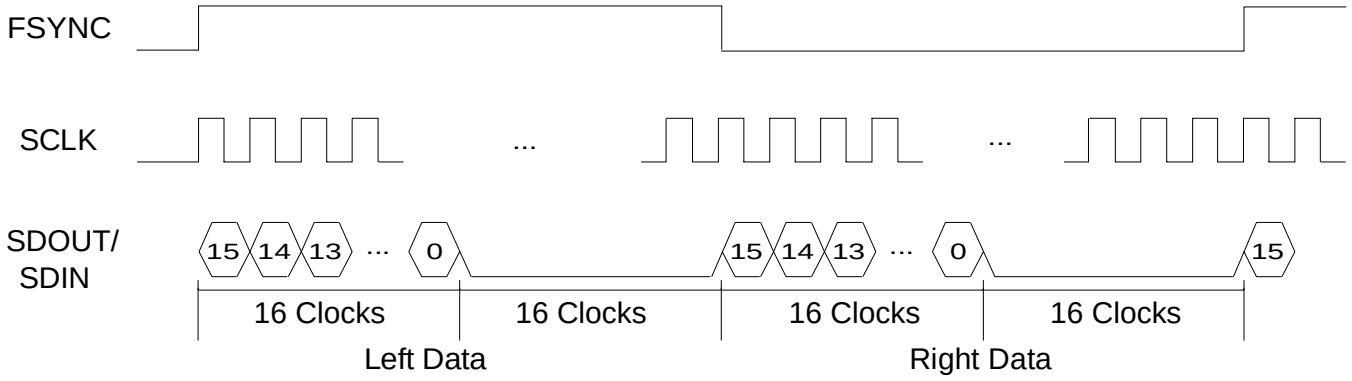


Figure 7. 64-bit Mode (SF1,0 = 01)

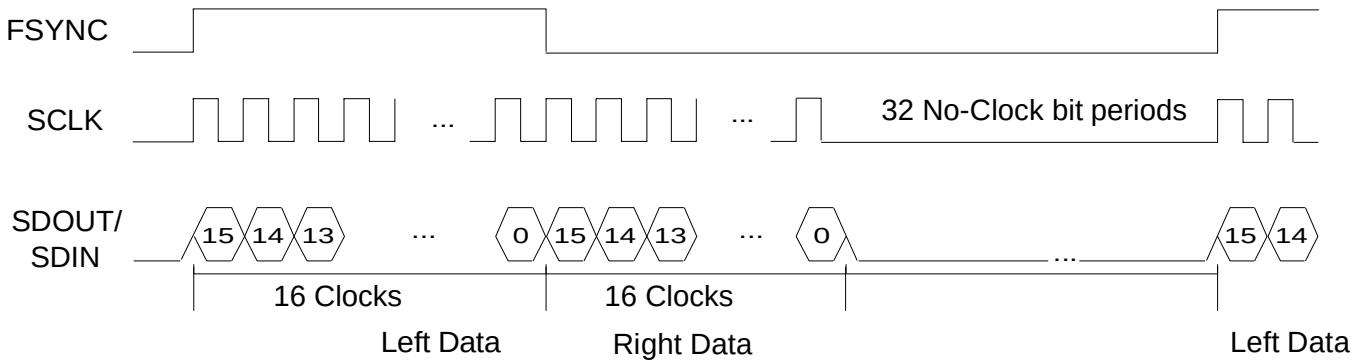


Figure 8. 32-bit Mode (SF1,0 = 10)

cupy the right word. The last 32 bits contain four status bits and 28 zeros. This is the only mode that contains status information.

The second serial format - SPF1, shown in Figure 7, is called 64-bit mode. This format has 64 SCLKs per frame, with FSYNC high transitions at the start of the left data word and low transitions at the start of the right data word. Both the left and right data words are followed by 16 zeros.

The third serial format - SPF2, shown in Figure 8, is called 32-bit mode. This format has 32 SCLKs per frame and FSYNC is high for the left channel and low for the right channel. The absolute time is similar to the other two modes but SCLK is stopped after the right channel is finished. SCLK is held stopped until the start of the next frame (stopped for 32 bit period times). This mode is useful for DSPs that do not want the interrupt overhead of the 32 unused bit periods. As an example, if a DSP serial word length is 16 bits, then four interrupts will occur in SPF0 and SPF1 modes. In mode SPF2 the DSP will only be interrupted twice.

The fourth serial format - SPF3, shown in Figure 9, is called ADC/DAC mode. This format has 64 SCLKs per frame, with FSYNC high transitions at the start of the left ADC data word and low transitions at the start of the right ADC data word. For serial data in, SDIN, both the left and right 16-bit DAC data word should be followed by zeros. For serial data out, SDOUT, both the left and right ADC data words are followed by 16 bits of the DAC data words. The DAC data words are tapped off the data stream right before the data enters the Codec DACs. Having the ADC and DAC data on the SDOUT allows external modem DSPs to cancel the local audio source from the local microphone signal.

CS9236 WAVETABLE SERIAL PORT

A digital interface to the CS9236 Single-Chip Wavetable Music Synthesizer is provided that allows the CS9236 PCM audio data to be summed digitally into the output digital mixer. This serial port is enabled via the WTEN bit located in Control register C8/X24 or in the Global Configuration byte in the Hardware Configuration data. The hardware connections to the CS9236 are illustrated in Figure 11.

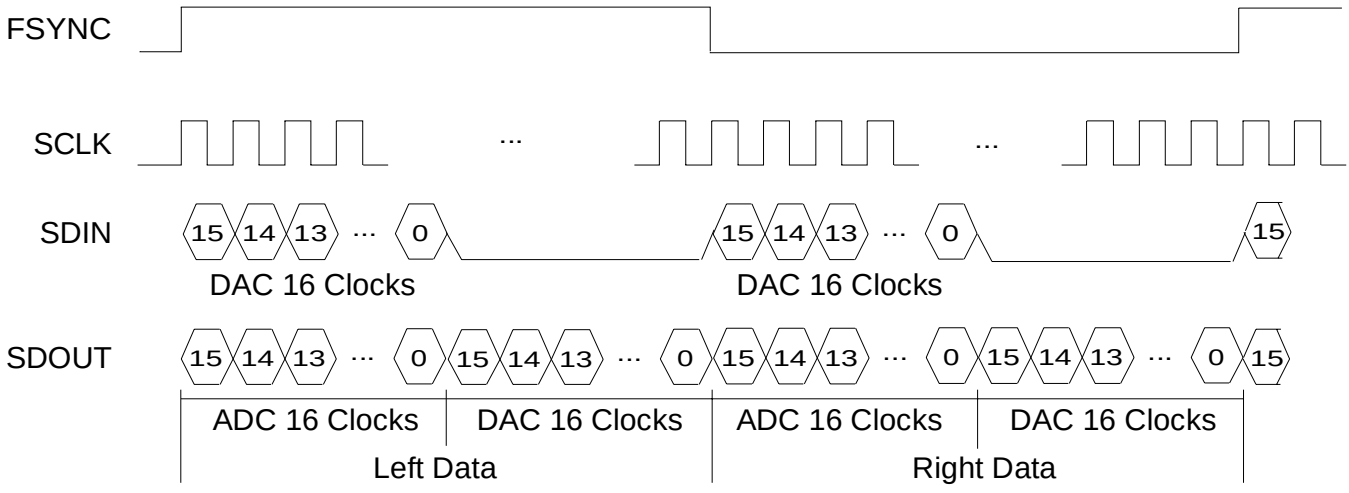


Figure 9. ADC/DAC Mode (SF1,0 = 11)

The CS9236 data is sent to DAC2 which can be summed into the input or output mixer. Volume control for the serial port is supported through I18 and I19 in the WSS register space.

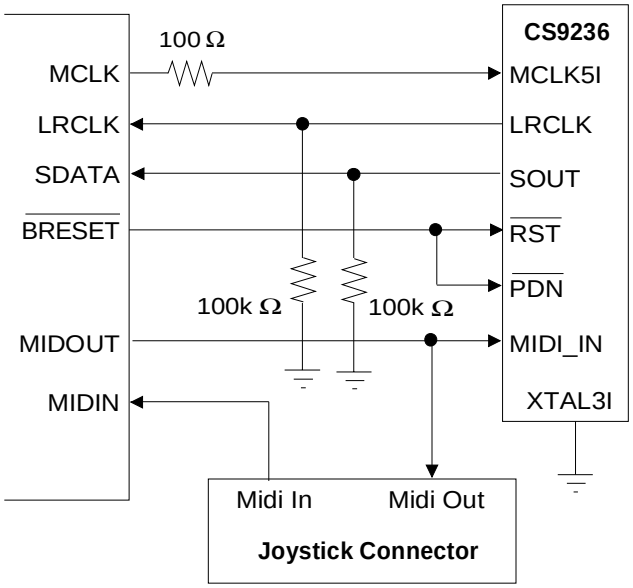


Figure 11. CS9236 Wavetable Serial Port Interface

ZVPORT SERIAL INTERFACE

The ZVPORT interface consists of three input pins: ZLRCK, ZSCLK, and ZSDATA. ZLRCK is the Left/Right clock indicating which channel is currently being received. ZSCLK is the serial bit clock where ZLRCK and ZSDATA change on the falling edge and serial data is internally latched on the rising edge. Note that the serial data starts one ZSCLK period after ZLRCK transitions. Figure 10 illustrates the clocking on the ZVPORT pins.

The ZVPORT interface is enabled by setting ZVEN in X18. The initial state of ZVEN on power-up can be set from the Hardware Configuration, Global Configuration Byte 2. Once enabled, the ZVPORT interface is connected to DAC2. When DAC2 is being used for ZVPORT, it cannot be used for other devices such as CS9236 Wavetable serial interface, CS4610 DSP serial interface, or internal FM synthesizer. Volume control for the ZVPORT is supported through I18 and I19 in the WSS register space.

An activity bit, ZVA, exists in the Global Status register, CTRLbase+7 (or X30 in WSS space) which is high when activity exists on the ZVPORT. When the ZVPORT is enabled (ZVEN = 1), the CS4239 automatically detects a clock on the ZLRCK pin and switches to the ZVPORT interface when the clock is present. When the ZLRCK is not present, the CS4239 automatically switches back to FM/Wavetable.

WSS CODEC SOFTWARE DESCRIPTION

The WSS Codec must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9) or the Sample Frequency (lower four bits) in the Fs & Playback Data Format registers (I8) are allowed. The actual audio data formats, which are the upper four bits of I8 for playback and I28 for capture, can be changed by setting MCE (R0) or PMCE/CMCE (I16) high. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

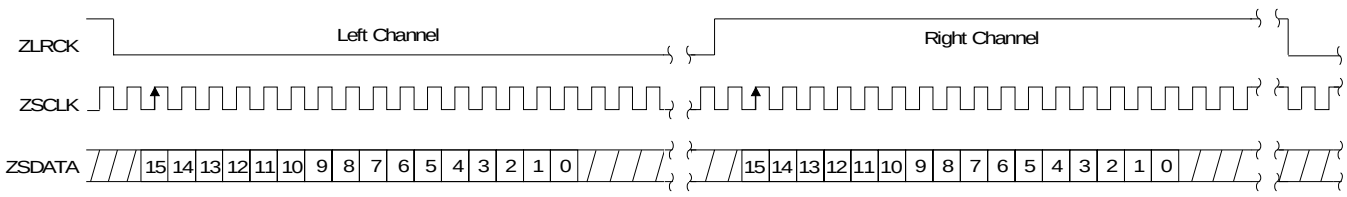


Figure 10. ZVPORT Clocking Format

Calibration

The WSS Codec has four different calibration modes. The selected calibration occurs whenever the Mode Change Enable (MCE, R0) bit goes form 1 to 0.

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. Transfers enabled during calibration will not begin until the calibration cycle has completed. Since the part always operates at 44.1 kHz internally, all calibration times are based on 44.1 kHz sample periods.

The Calibration procedure is as follows:

1) Place the WSS Codec in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) Set the CAL1,0 bits in the Interface Configuration register (I9).

3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).

4) Wait until 80h NOT returned

5) Wait until ACI (I11) cleared to proceed

NO CALIBRATION (CAL1,0 = 00)

This is the fastest mode since no calibration is performed. This mode is useful for games which require the sample frequency be changed quickly. This mode is also useful when the codec is operating full-duplex and an ADC data format change is desired. This is the only calibration mode that does not affect the DACs (i.e. mute the DACs). The No Calibration mode takes zero sample periods.

CONVERTER CALIBRATION (CAL1,0 = 01)

This calibration mode calibrates the ADCs and the DACs, but does not calibrate any of the analog mixing channels. This is the second longest calibration mode, taking 321 sample periods at 44.1 kHz. Because the analog mixer is not calibrated in this mode, any signals fed through the mixer will be unaffected. The calibration sequence is as follows:

The DACs are muted
The ADCs are calibrated
The DACs are calibrated
The DACs are unmuted

DAC CALIBRATION (CAL1,0 = 10)

This calibration mode only clears the DACs (playback) interpolation filters leaving the ADC unaffected. This is the second fastest calibration mode (no cal. is the fastest) taking 120 sample periods at 44.1 kHz to complete. The calibration sequence is as follows:

The DACs are muted
The DAC filters are cleared
The DACs are unmuted

FULL CALIBRATION (CAL1, 0 = 11)

This calibration mode calibrates all offsets, ADCs, DACs, and analog mixers. Full calibration will automatically be initiated on power up or anytime the WSS Codec exits from a full power down state. This is the longest calibration mode and takes 450 sample periods at 44.1 kHz to complete. The calibration sequence is as follows:

All outputs are muted (DACs and mixer)
The mixer is calibrated
The ADCs are calibrated
The DACs are calibrated
All outputs are unmuted

Changing Sampling Rate

The internal states of the WSS Codec are synchronized by the selected sampling frequency. The sample frequency can be set in one of three fashions. The standard WSS Codec method uses the Fs & Playback Data Format register (I8) to set the sample frequency. The changing of either the clock source or the clock frequency divide requires a special sequence for proper WSS Codec operation:

1) Place the WSS Codec in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock 2 Base Select (C2SL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)

3) The WSS Codec resynchronizes its internal states to the new frequency. During this time the WSS Codec will be unable to respond. Writes to the WSS Codec will not be recognized and reads will always return the value 80 hex.

4) The host now polls the WSS Codec's Index Address register (R0) until the value 80 hex is no longer returned. On slow processor systems, 80h may occur faster than software is able to read (80h may never occur).

5) Once the WSS Codec is no longer responding to reads with a value of 80 hex, normal operation can resume and the WSS Codec can be removed from MCE.

A second method of changing the sample frequency is to disable the sample frequency bits in I8 (lower four bits) by setting SRE in I22. When this bit is set, OSM1 and OSM0 in I10, along with the rest of the bits in I22, are used to set the sample frequency. Once enabled, these bits can be changed without doing an MCE cycle.

The third method supports independent sample frequencies (Fs) for capture and playback. The independent sample frequency mode is enabled by setting IFSE in X11. Once enabled, the other two methods for setting Fs (I8, I10, and I22) are disabled. The capture (ADC) Fs is set in X12 and the playback (DAC) Fs is set in X13.

Changing Audio Data Formats

In MODE 1, MCE must be used to select the audio data format in I8. Since MCE causes a calibration cycle, it is not ideal for full-duplex operation. In MODE 2 and 3, individual Mode Change Enable bits for capture and playback are provided in register I16. MCE (R0) must still be used to select the sample frequency, but PMCE (playback) and CMCE (capture) allow changing the respective data formats without causing a calibration to occur. Setting PMCE (I16) clears the playback FIFO and allows the upper four bits of I8 to be changed. Setting CMCE (I16) clears the capture FIFO and allows the upper four bits of I28 to be changed.

Audio Data Formats

The sample frequency is always selected in the Fs & Playback Data Format register (I8). In MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2 and 3, I8 only selects the playback data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The WSS Codec always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size.

There are two data formats supported by the WSS Codec: 16-bit signed (little Endian) and 8-bit unsigned. See Figures 13-16.

16-BIT SIGNED

The 16-bit signed data format is "little endian". This format defines the byte ordering of a multi-byte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent maximum negative analog amplitude, 0 for center scale, and 32767 (7FFFh) to represent maximum positive analog amplitude.

8-BIT UNSIGNED

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent maximum negative analog amplitude, 128 for center scale, and 255 (FFh) to represent maximum positive analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 12.

DMA Registers

The DMA registers allow easy integration of this part into ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register causes both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the Current Count register until zero is reached. The next sample after zero generates an interrupt and reloads the Current Count registers with the values in the Base registers.

For all data formats the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". A sample is one to four bytes wide and is defined as all data taken at one instant in time. Stereo and mono data contain the same number of samples, and 8-bit data and 16-bit data contain the same number of samples.
Symbolically:

$$\text{DMA Base register}_{16} = N_S - 1$$

Where N_S is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

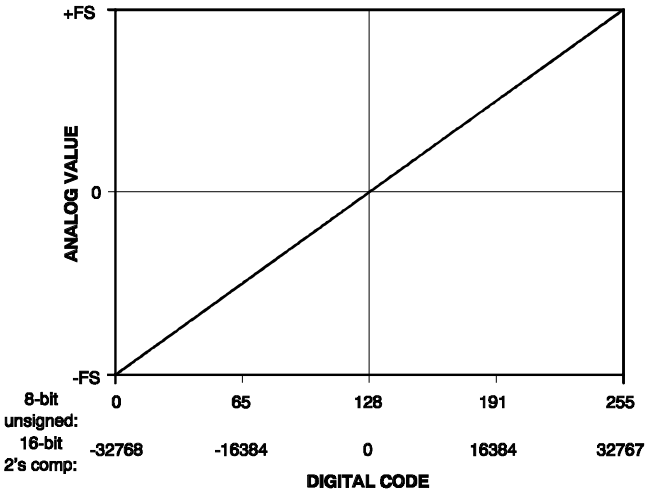


Figure 12. Linear Transfer Functions

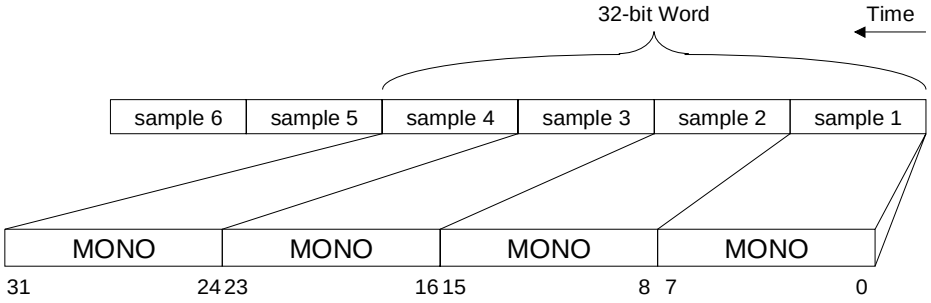


Figure 13. 8-bit Mono, Unsigned Audio Data

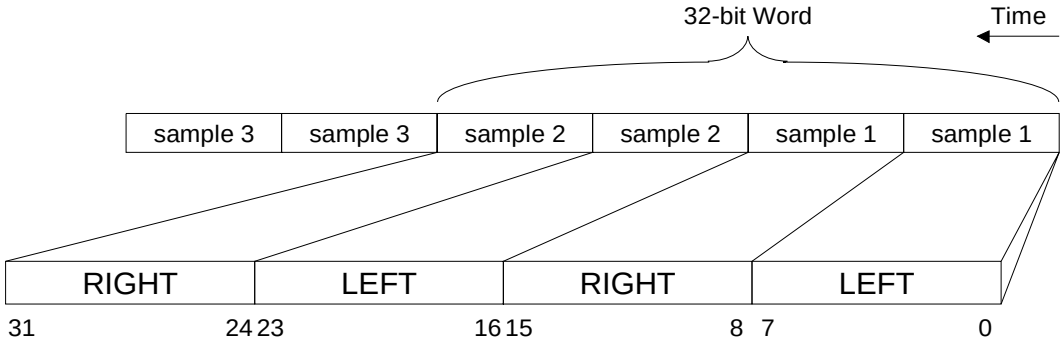


Figure 14. 8-bit Stereo, Unsigned Audio Data

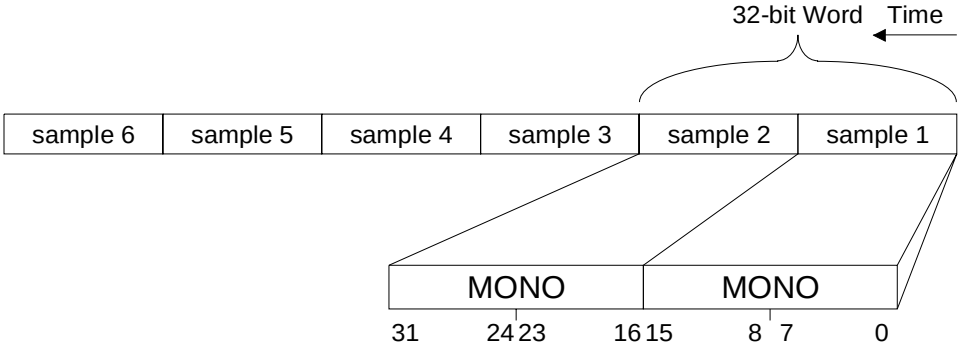


Figure 15. 16-bit Mono, Signed Little Endian Audio Data

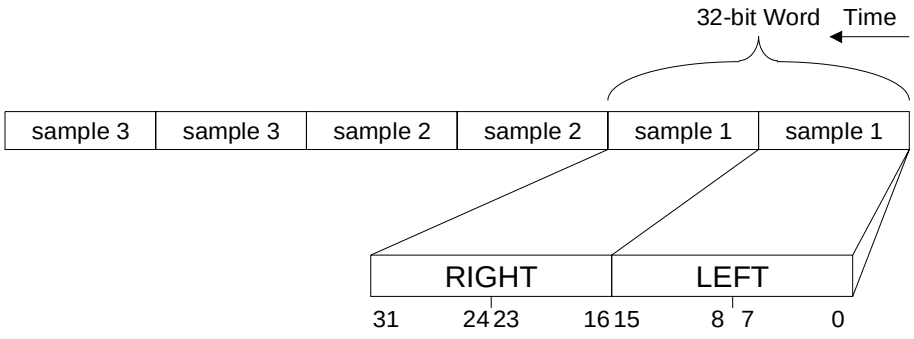


Figure 16. 16-bit Stereo, Signed Little Endian Audio Data

PLAYBACK DMA REGISTERS

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2 and 3. In MODE 1, these registers (I14/15) are used for both playback and capture; therefore, full-duplex DMA operation is not possible.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24).

CAPTURE DMA REGISTERS

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation capture and playback can occur simultaneously. These registers are provided in MODE 2 and 3 only.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Capture Interrupt bit, CI (I24).

WSS Codec Interrupt

The INT bit of the Status register (R2) always reflects the status of the WSS Codec's internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI) in the Alternate Feature Status register (I24).

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt assigned to the WSS Codec responds to the interrupt event. When the IEN bit is low, the interrupt is masked and the IRQ pin assigned to the WSS Codec is held low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the WSS Codec in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the WSS Codec.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output (assuming DACZ = 0) to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

The overrun and underrun error bits in the *Alternate Feature Status* register, I24, are cleared by first clearing the condition that caused the overrun or underrun error, followed by writing the particular bit to a zero. As an example, to clear the playback underrun bit PU, first a sample must be sent to the WSS Codec, and then the PU bit must be written to a zero.

DIGITAL HARDWARE DESCRIPTION

The best example of hardware connection for the different sections of this part is the *Reference Design* Data Sheet. The *Reference Design* Data Sheet contains all the schematics, layout plots and a Bill of Materials; thereby providing a complete example.

Bus Interface

The ISA bus interface is capable of driving a 24 mA data bus load and therefore does not require any external data bus buffering. See the *Reference Design* Data Sheet for a typical connection diagram.

Volume Control Interface

Three hardware master volume control pins are supported: volume up, volume down, and mute. Hardware volume control is enabled by setting the VCEN bit in the Hardware Configuration data, byte 7 (Misc. Config. Byte). Once VCEN is set, the XTAL1/ACDCS/DOWN pin converts to the volume down function. The volume control pins affect the master volume control output after the analog output mixer. The UP and DOWN pins, when low, increment and decrement the master volume. These two pins would use SPST momentary switches. The MUTE pin can either be momentary or non-existent where pressing up and down simultaneously mutes the output volume. The circuit in Figure 17, contains optional resistors for EMI and ESD protection; however, the capacitors are required for switch debounce.

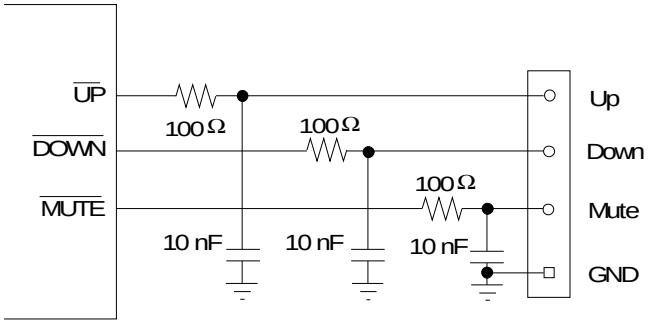


Figure 17. Volume Control Circuit

Pressing the up button, increments the volume. Pressing the down button, decrements the volume. Holding either of these buttons in the low state causes the volume to to continue changing.

The formats are selected using the VCF1 bit in the Hardware Configuration data, Global Config. byte.

In the first format, where VCF1 = 0, the mute function is a momentary switch (similar to up and down). When MUTE goes low the master out volume mutes if it was un-muted and vise-versa (the mute button alternates between mute and un-mute). If the master volume is muted and up or down is pressed, the volume automatically un-mutes.

In the second format, where VCF1 = 1, the MUTE pin is not used. This is a two-button format where pressing up and down simultaneously mutes the master volume. If the master volume is muted and up or down is individually pressed, the volume automatically un-mutes.

The two formats listed above as illustrated in Figure 18.

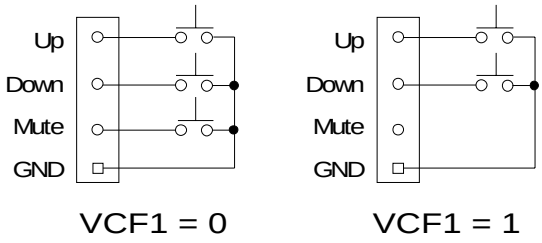


Figure 18. Volume Control Formats

Crystal / Clock

Two pins have been allocated to allow the interfacing of a crystal oscillator: XTALI and XTALO. The crystal should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors connected to each of the crystal pins should be twice the load capacitance specified to the crystal manufacturer.

An external CMOS clock may be connected to the crystal input XTALI in lieu of the crystal.

When using an external CMOS clock, the XTALO pin must be left floating with no trace or external connection of any kind.

General Purpose Output Pins

Two general purpose outputs are provided to enable control of external circuitry (i.e. mute function). XCTL1 and XCTL0 in the WSS Codec register I10 are output directly to the appropriate pin when enabled.

Pin XCTL1/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$ is initially controlled by the VCEN bit in the Hardware Configuration data. If VCEN is zero, this pin becomes XCTL1 if the SDOUT pin is sampled high during a high-to-low transition of RESDRV. This pin can also output $\overline{\text{ACDCS}}$ if the SDOUT pin is sampled low during a high-to-low transition of the RESDRV pin. SDOUT has an internal pullup resistor. VCEN has the highest precedence and will cause this pin to convert to the $\overline{\text{DOWN}}$ function whenever VCEN is set.

Reset and Power Down

A RESDRV pin places the part into maximum power conservation mode. When RESDRV goes high, the PnP registers are reset - all logical devices are disabled, all analog outputs are muted, and the voltage reference then slowly decays to ground. When RESDRV is brought low, an initialization procedure begins which causes a full calibration cycle to occur. When initialization is completed, the registers will contain their reset value and the part will be isolated from the bus. RESDRV is required whenever the part is powered up. The initialization time varies based on whether an E^2PROM is present or not and the size of the data in the E^2PROM. After RESDRV goes low, the part should not be written to for approximately 200 ms to guarantee that the part is ready to respond to commands. The exact timing is specified in the *Timing Section* in the front of this data sheet.

Software low-power states are available through bits in the Control or WSS logical device register space. See the *CONTROL INTERFACE* section for more information.

Address Port Configuration

The part provides a method for motherboards to hide the part from standard PnP (or traditional Crystal Key) software. BIOSes can use this method to set the part at a unique address, and report the device as a System Dev. Node to the operating system.

On the high to low transition of the RESDRV pin, the part samples the state of the APSEL and SCL, which have internal 100 kΩ pullups to +5 V. APSEL selects the Address Port used to configure the part. When APSEL is left high, the Address Port is 0x279 and backwards compatible to previous chips and standard PnP software. When APSEL is externally tied to SGND, the Address Port is moved to one of two locations, selected by a strapping option on the SCL pin. If SCL is sampled high (default), then the Address Port is moved to 0x308. If SCL is strapped low with an external 10 kΩ resistor to SGND, the Address Port is moved to 0x388.

If the Address Port is moved (APSEL = 0) then the device is no longer PnP compliant; however, it will still respond to all the standard PnP commands using the new Address Port. In addition, the new Address Port supports the traditional Crystal Key or the new Crystal Key 2.

Multiplexed Pin Configuration

On the high to low transition of the RESDRV pin, the part samples the state of the MCLK and SDOUT which have internal 100 kΩ pullups to +5 V.

The state of MCLK at the time RESDRV is brought low determines the function of the CDROM interface pins. If MCLK is sampled high, then $\overline{\text{CDCS}}$, $\overline{\text{CDACK}}$, CDINT, CDRQ are

used to input SA12, SA13, SA14, SA15 respectively. If MCLK is sampled low (external pulldown) then $\overline{\text{CDCS}}$, $\overline{\text{CDACK}}$, CDINT, CDRQ become the standard CDROM interface pins.

The XCTL1/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$ pin state is first determined by VCEN. If VCEN is set this pin is forced to the $\overline{\text{DOWN}}$ volume control pin. If VCEN is zero, then a strapping option on SDOUT determines the pin function. If SDOUT is high (default) on powerup, the pin is forced to the XCTL1 general purpose output that tracks the bit by the same name in I10 in the WSS space. If SDOUT is externally pulled low through a 10 kΩ resistor, then the pin is forced to the alternate CDROM chip select function, $\overline{\text{ACDCS}}$.

ANALOG HARDWARE DESCRIPTION

The analog hardware consist of an MPC Level 3-compatible mixer. This section describes the analog hardware needed to interface with these pins.

Line-Level Inputs

The analog inputs consist of three stereo analog inputs, and one mono input. As shown in Figure 4, the input to the ADCs comes from the Input Mixer that selects any combination of the following: AUX1, AUX2, MIC, DAC1, DAC2, and the output from the analog output mixer. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

The analog input interface is designed to accommodate two stereo inputs and two mono inputs. Three of these sources are mixed to the ADC. These inputs are: a mono microphone input (MIC), a stereo CD-ROM input (AUX2), and a stereo auxiliary line-level input (AUX1). The MIC, AUX1, and AUX2 inputs have paths after their volume controls, to the output mixer. The output mixer has the additional input of a mono input channel. All audio inputs should be capacitively coupled.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 19 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs.

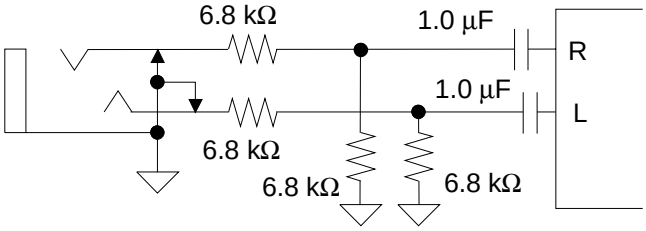


Figure 19. Line Inputs

The AUX2 line-level inputs have an extra pin, CMAUX2, which provides a pseudo-differential input for both LAUX2 and RAUX2. This pin takes the common-mode noise out of the AUX2 inputs when connected to the ground coming from the AUX2 analog source. Connecting the AUX2 pins as shown in Figure 20 provides extra noise attenuation coming from the CDROM drive, thereby producing a higher quality signal. Since the better the resistors match, the better the common-mode attenuation, one percent resistors are recommended. If CMAUX2 is not used, it should be connected through an AC cap to analog ground.

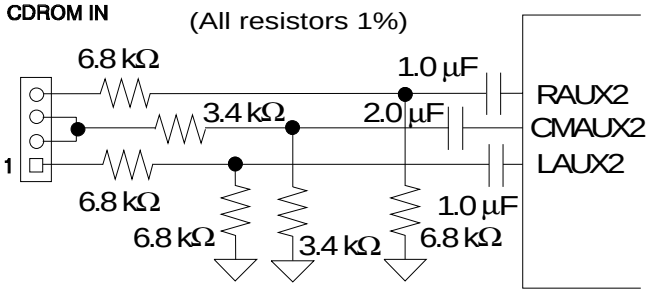


Figure 20. Differential CDROM In

Microphone Level Input

The microphone level input, MIC, include a selectable -22.5 dB to +22.5 dB gain stage for interfacing to an external microphone. An additional 20 dB gain block is also available. The 20 dB gain block can be switched off to provide another mono line-level input. Figure 21 illustrates a single-ended microphone input buffer circuit that will support lower gain mics. The circuit in Figure 21 supports dynamic mics and phantom-powered mics that use the ring portion of the jack for power.

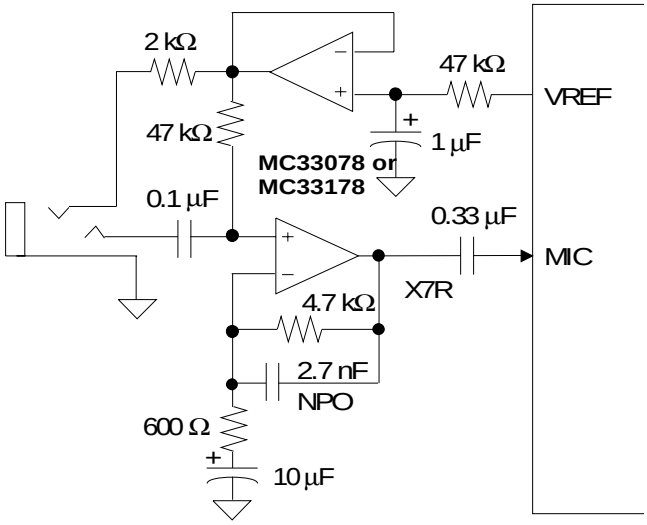


Figure 21. Microphone Input

Mono Input

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. The MIN pin can be mixed into the output mixer with at a 0 or -9 dB level. Also, the MIM and MIMR bits support muting the input to the left and right channels respectively. Figure 22 illustrates a typical input circuit for the Mono In. If MIN is driven from a CMOS gate, the 4.7 kΩ should be tied to AGND instead of VA+. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes.

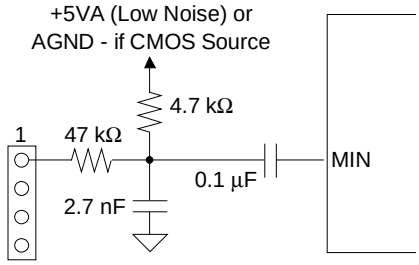


Figure 22. Mono Input

Line Level Outputs

The analog output section provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry. Both LOUT and ROUT need 1000 pF NPO capacitors between the pin and AGND.

Miscellaneous Analog Signals

The VREF pin is typically 2.2 V and provides a common mode signal for single-supply external circuits. VREF only supports light DC loads and should be buffered if AC loading is needed. For typical use, a 0.1 µF in parallel with a 10 µF capacitor should be connected to VREF.

GROUNDING AND LAYOUT

Figure 23 is a suggested layout for motherboard designs and Figure 24 is a suggested layout for add-inn cards. For optimum noise performance, the device should be located across a split analog/digital ground plane. The digital ground plane should extend across the ISA bus pins as well as the internal digital interface pins. DGND1 is ground for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus interface due to transient currents during bus switching. SGND1-4 should also be connected to the digital ground plane to minimize coupling into the analog section. Figure 25 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the part. The vias shown

go through to the ground and power plane layers. Vias and power supply traces should be as large as possible to minimize the impedance.

POWER SUPPLIES

The power supply providing analog power should be as clean as possible to minimize coupling into the analog section and degrading analog performance.

The VD1 is isolated from the rest of the power supply pins and provide digital power for the asynchronous parallel ISA bus. The VD1 pin can be connected directly to the system digital power supply.

VDF1 through VDF3 provide power to internal digital sections of the codec and should be quieter than VD1. This can be achieved by using a ferrite bead to the VD1 supply.

VA provides power to the sensitive analog sections of the chip and should have a clean, regulated supply to minimize power supply coupled noise in the analog inputs and outputs.

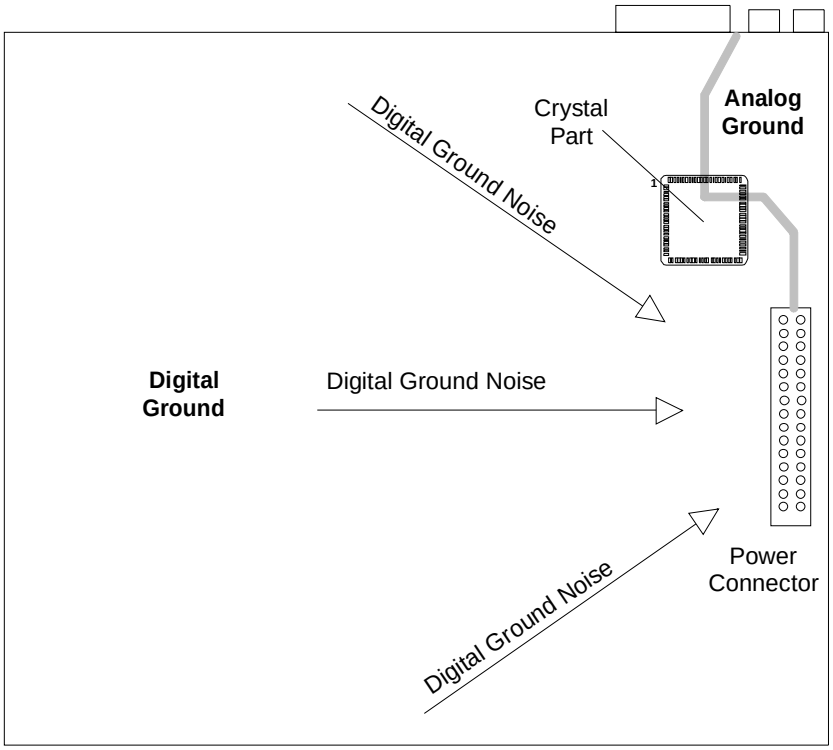


Figure 23. Suggested Motherboard Layout

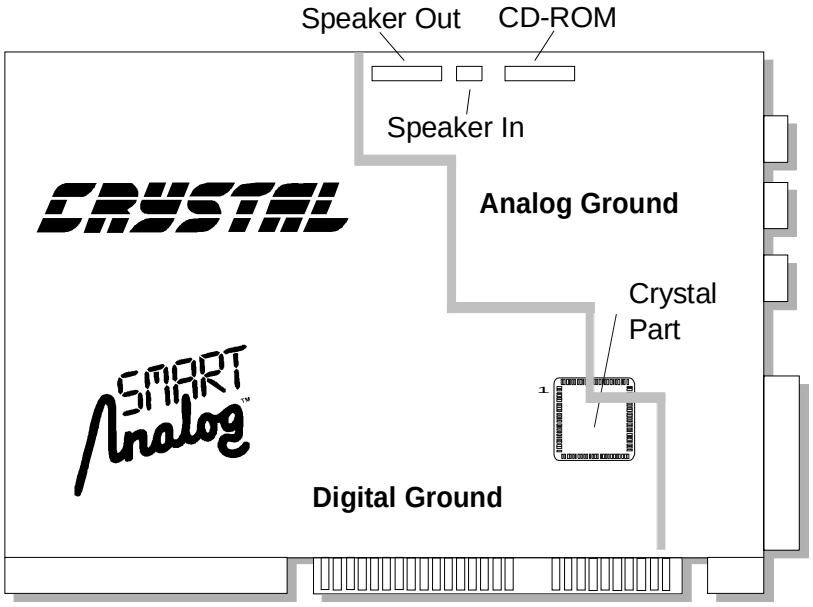


Figure 24. Suggested Add-In Card Layout

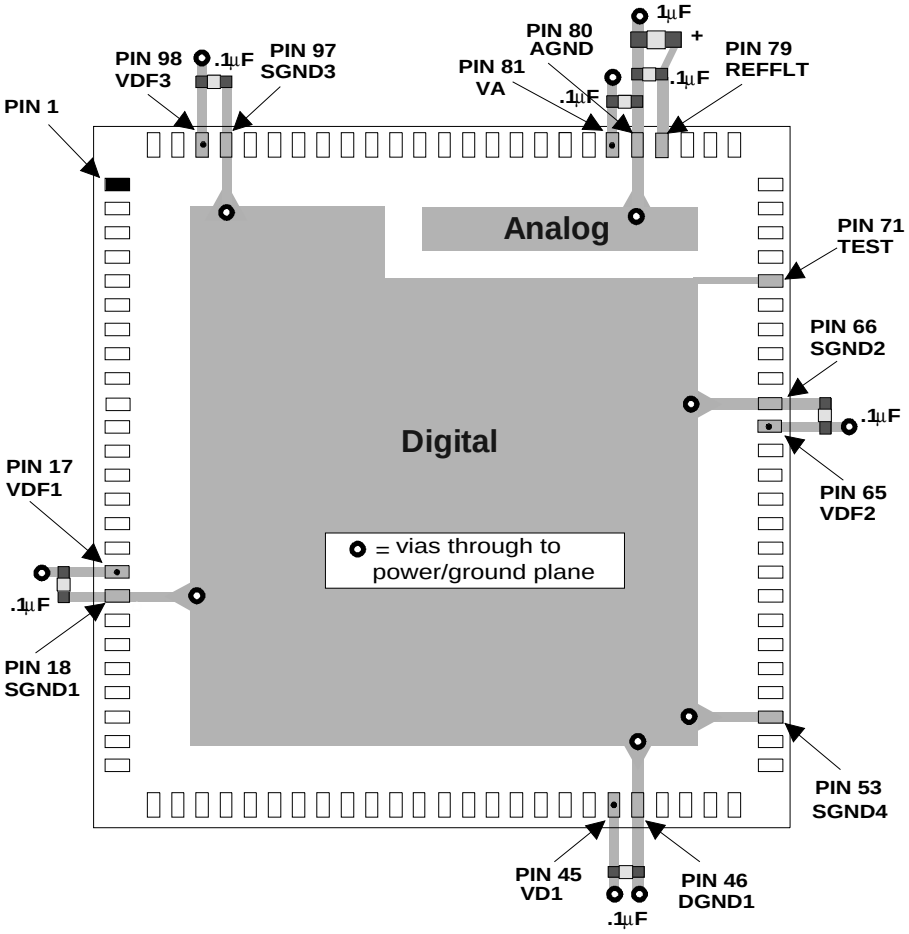


Figure 25. Recommended Decoupling Capacitor Positions

ADC/DAC FILTER RESPONSE PLOTS

Figures 26 through 31 show the overall frequency response, passband ripple, and transition band for the ADCs and DACs. Figure 32 shows the DACs' deviation from linear phase. Since the filter response scales based on sample frequency selected, all frequency response plots x-axis are shown from 0 to 1, where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.

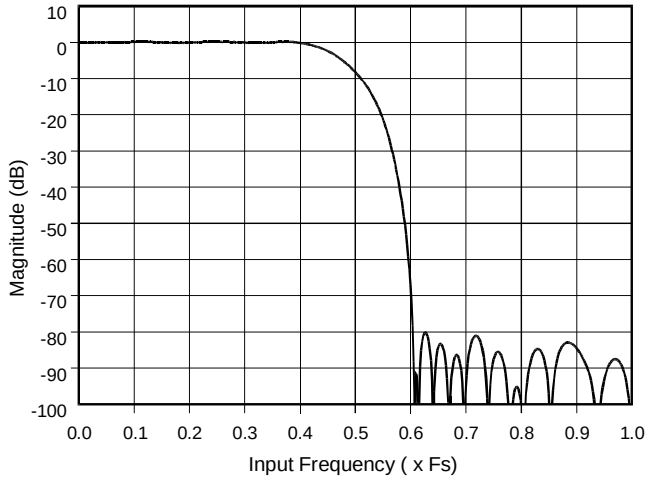


Figure 26. ADC Filter Response

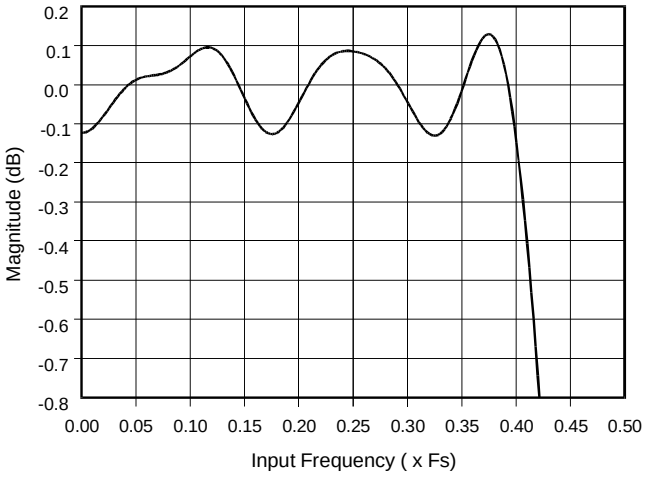


Figure 27. ADC Passband Ripple

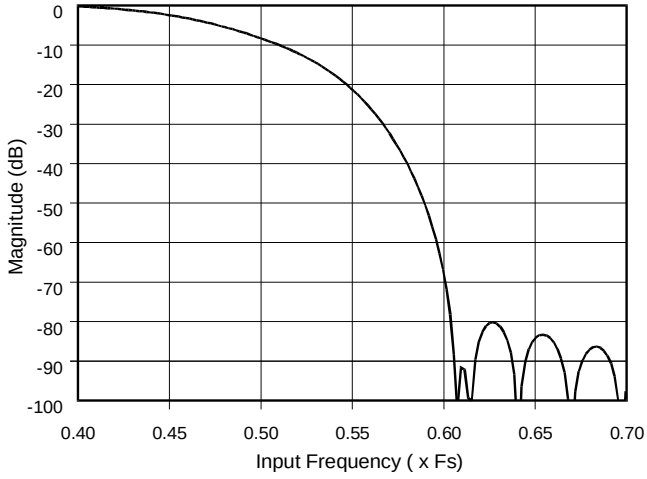


Figure 28. ADC Transition Band

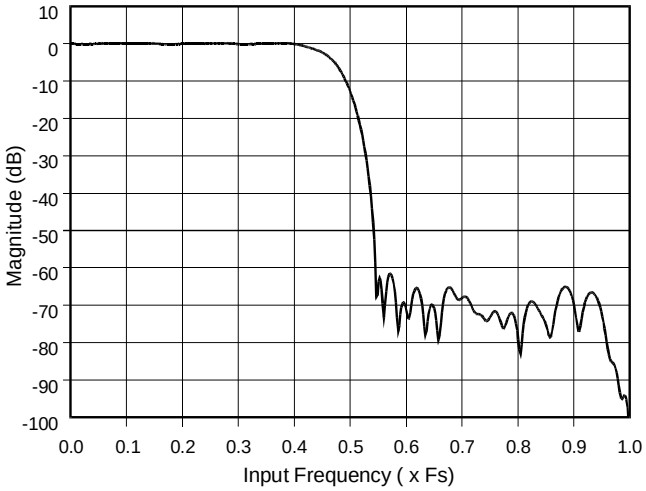


Figure 29. DAC Filter Response

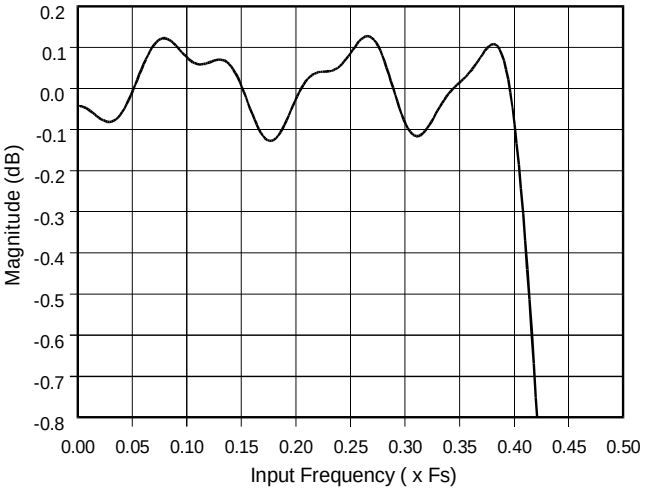


Figure 30. DAC Passband Ripple

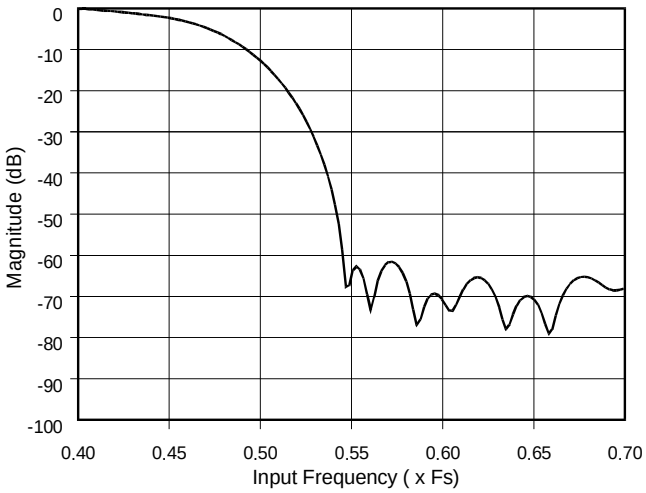


Figure 31. DAC Transition Band

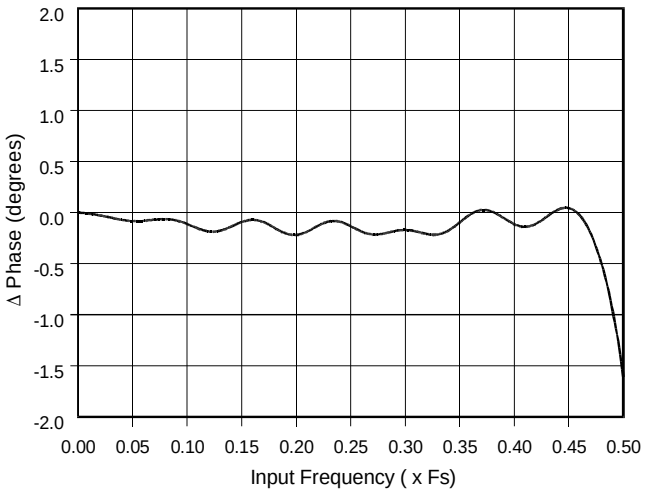
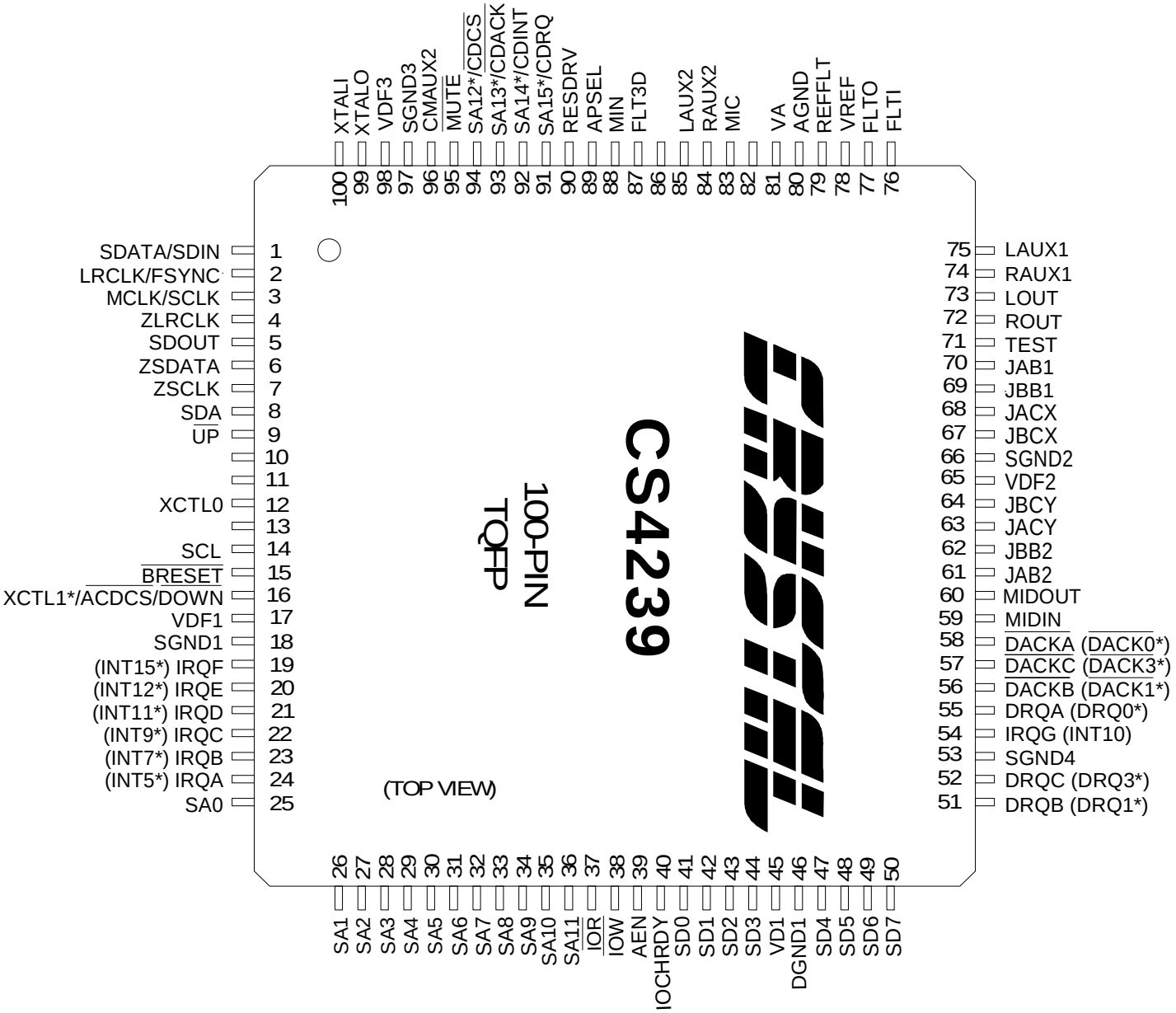


Figure 32. Deviation from Linear Phase

PIN DESCRIPTIONS



* **Defaults** - See individual pin descriptions for more details

ISA Bus Interface Pins

SA<11:0> - System Address Bus, Inputs

These signals are decoded during I/O cycles to determine access to the various functional blocks within the part as defined by the configuration data written during a Plug and Play configuration sequence.

SA<15:12> - Upper System Address Bus, Inputs

These signals are multi-function pins, shared with the CDROM, that default to the upper address bits SA12 through SA15. These pins are generally used for motherboard designs that want to eliminate address decode aliasing. Using these pins as upper address bits forces the part to only accept valid address decodes when A12-A15 = 0. If these pins are not used for address decodes or for CDROM support, they should be tied to SGND. These pins are forced to the CDROM interface when a 10 kΩ resistor is placed on pin MCLK/SCLK to SGND.

SD<7:0> - System Data Bus, Bi-directional, 24 mA drive

These signals are used to transfer data to and from the part.

AEN - Address Enable, Input

This signal indicates whether the current bus cycle is an I/O cycle or a DMA cycle. This signal is low during an I/O cycle and high during a DMA cycle.

$\overline{\text{IOR}}$ - Read Command Strobe, Input

This active low signal defines a read cycle to the part. The cycle may be a register read or a read from the part's DMA registers.

$\overline{\text{IOW}}$ - Write Command Strobe, Input

This active low signal indicates a write cycle to the part. The cycle may be a write to a control register or a DMA register.

IOCHRDY - I/O Channel Ready, Open Drain Output, 8 mA drive

This signal is driven low by the part during ISA bus cycles in which the part is not able to respond within a minimum cycle time. IOCHRDY is forced low to extend the current bus cycle. The bus cycle is extended until IOCHRDY is brought high.

DRQ<A,B,C> - DMA Requests, Outputs, 24 mA drive

These active high outputs are generated when the part is requesting a DMA transfer. This signal remains high until all the bytes have been transferred as defined by the current transfer data type. The DRQ<A,B,C> outputs must be connected to 8-bit DMA channel request signals only. The defaults on the ISA bus are DRQA = DRQ0, DRQB = DRQ1, and DRQC = DRQ3. The defaults can be changed by modifying the Hardware Resource data.

$\overline{\text{DACK}}$<A,B,C> - DMA Acknowledge, Inputs

The assertion of these active low signals indicate that the current DMA request is being acknowledged and the part will respond by either latching the data present on the data bus (write) or putting data on the bus (read). The $\overline{\text{DACK}}$<A,B,C> inputs must be connected to 8-bit DMA channel acknowledge lines only. The defaults on the ISA bus are $\overline{\text{DACKA}}$ = $\overline{\text{DACK0}}$, $\overline{\text{DACKB}}$ = $\overline{\text{DACK1}}$, and $\overline{\text{DACKC}}$ = $\overline{\text{DACK3}}$. The defaults can be changed by modifying the Hardware Resource data.

IRQ <A:G>- Host Interrupt Pins, Outputs, 24 mA drive

These signals are used to notify the host of events which need servicing. They are connected to specific interrupt lines on the ISA bus. The IRQ<A:G> are individually enabled as per configuration data that is generated during a Plug and Play configuration sequence. The defaults on the ISA bus are IRQA = INT5, IRQB = INT7, IRQC = INT9, IRQD = INT11, IRQE = INT12, IRQF = INT15. IRQG is new to the CS4239 and defaults to unconnected for compatibility reasons. For new designs, IRQG is typically connected to IRQ10. The defaults can be changed by modifying the Hardware Configuration data loaded from the E^2PROM.

RESDRV - Reset Drive, Input

Places the part in lowest power consumption mode. All sections of the part are shut down and consuming minimal power. The part is reset and in power down mode when this pin is logic high. The falling edge also latches the state of MCLK and SCLK to determine the functionality of dual mode pins, and SCL to determine the Address Port. This signal is typically connected to the ISA bus signal RESDRV. RESDRV must be asserted whenever the part is powered up to initialize the internal registers to a known state. This pin, when high, also drives the $\overline{\text{BRESET}}$ pin low.

Analog Inputs

MIC - Mic Input

Microphone input centered around VREF. A programmable gain block provides volume control and is located in X2 with mutes located in X2 and X3.

LAUX1 - Left Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. A programmable gain block provides volume control and is located in I2. Typically used for an external Left line-level input.

RAUX1 - Right Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. A programmable gain block provides volume control and is located in I3. Typically used for an external Right line-level input.

LAUX2 - Left Auxiliary #2 Input

Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block provides volume control and is located in I4. Typically used for the Left channel CDROM input.

RAUX2 - Right Auxiliary #2 Input

Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block provides volume control and is located in I5. Typically used for the Right channel CDROM input.

CMAUX2 - Common Mode Auxiliary #2 Input

Common mode ground input for the LAUX2 and RAUX2 inputs. Typically connected to the CDROM ground input to provide common-mode noise rejection. The impedance on this pin should be one half the impedance on the LAUX2 and RAUX2 inputs.

MIN - Mono Input

Nominally 1 V_{RMS} max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the output mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system.

REFFLT - Reference Filter, Input

Voltage reference used internal to the part. A 0.1 µF and a 1 µF capacitor with short fat traces must be connected between this pin and AGND. No other connections should be made to this pin.

Analog Outputs

LOUT - Left Line Level Output

Analog output from the mixer for the left channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

ROUT - Right Line Level Output

Analog output from the mixer for the Right channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

FLT3D - 3D Filter

This pin needs a 0.01 µF capacitor attached and tied to analog ground.

FLTO - Filter Output

This pin needs a 1000 pF NPO capacitor attached and tied to FLTI.

FLTI - Filter Input

This pin needs a 1000 pF NPO capacitor attached and tied to FLTO.

VREF - Voltage Reference, Output

All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered.

MIDI Interface

MIDOUT - MIDI Out Transmit Data, Output, 4 mA drive

This output is used to send MIDI data serially out to a external MIDI device. Normally connected to pin 12 of the joystick connector for use with breakout boxes, as well as on-board synthesizers.

MIDIN - MIDI In Receive Data, Input - Internal Pullup

This input is used to receive serial MIDI data from an external MIDI device. This pin should be connected to pin 15 of the joystick connector for use with breakout boxes.

External Peripheral Signals

SDA - E^2PROM Data Pin, Bi-directional, Open Drain, 4 mA sink

This open-drain pin must have an external pullup (3.3 kΩ) and is used in conjunction with SCL to access an external serial E^2PROM. When an E^2PROM is used, the SDA pin should be connected to the data pin of the E^2PROM device and provides a bi-directional data port. The E^2PROM is used to set the Plug and Play resource data.

XCTL0 - External Control, Output, 4 mA drive

This pin is a general purpose output pin controlled by the XCTL0 bit in the WSS register I10.

SCL - E^2PROM Serial Clock, Output, 4 mA drive (Address Port Selection)

When E^2PROM access is enabled, via EEN in CTRLbase+1, then SCL is used as a clock output to the E^2PROM. At power-up, this pin is an input (with an internal 100 kΩ pullup) that selects between two alternate addresses for the Address Port used to configure the chip. Assuming APSEL is strapped low, SCL high selects 308h as the Address Port, and when SCL is tied low (with a 10 kΩ resistor to ground), the Address Port is 388h.

$\overline{\text{BRESET}}$ - Buffered Reset, Output, 4 mA drive

This active low signal goes low whenever the RESDRV pin goes high. This pin is also software controllable through the BRES bit in register C8 in the Control Logical Device space. BRES provides a software power down and reset control over devices connected to the CS4239 such as the CS9236 Single-Chip Wavetable Music Synthesizer.

Joystick Interface

JACX, JACY - Joystick A Coordinates, Input

These pins are the X/Y coordinates for Joystick A. They should have a 5.6 nF capacitor to ground and a 2.2 kΩ resistor to the joystick connector pins 3 and 6, respectively.

JAB1, JAB2 - Joystick A Buttons, Input - Internal Pullups

These pins are the switch inputs for Joystick A. They should be connected to joystick connector pins 2 and 7, respectively; as well as have a 1 nF capacitor to ground.

JBCX, JBCY - Joystick B Coordinates, Input

These pins and are the X/Y coordinates for the second joystick, Joystick B. They should have a 5.6 nF capacitor to ground and a 2.2 kΩ resistor to the joystick connector pins 11 and 13, respectively.

JBB1, JBB2 - Joystick B Buttons, Input - Internal Pullups

These pins are the switch inputs for the second joystick, Joystick B. They should be connected to joystick connector pins 10 and 14, respectively; as well as have a 1 nF capacitor to ground.

CS4610 DSP Serial Port Interface

The CS4610 DSP serial port pins are shared with the CS9236 Wavetable serial port. When the serial port is enabled, SPE = 1 in I16, these pins are forced to the CS4610 DSP interface.

FSYNC - Frame Sync, Output

When the serial port is enabled, SPE = 1 in I16, this pin is the serial frame sync output.

SCLK - Serial Clock, Output (CDROM Enable)

When the serial port is enabled, SPE = 1 in I16, this pin is the serial clock output. At power-up, this pin is an input (with an internal 100 kΩ pullup) that, when pulled low with a 10 kΩ resistor to SGND, enables the CDROM interface (over the upper 4 ISA address pins). Loading must be limited to CMOS inputs if this pin has the 10 kΩ resistor attached.

SDOUT - Serial Data Output, Output (Alternate CDROM Chip Select Enable)

When the serial port is enabled, SPE = 1 in I16, this pin is the serial data output. At power-up, this pin is an input (with an internal 100 kΩ pullup) that, when pulled low with a 10 kΩ resistor to SGND, enables the alternate CDROM chip select pin $\overline{\text{ACDCS}}$. Loading must be limited to CMOS inputs if this pin has the 10 kΩ resistor attached.

SDIN - Serial Data Input, Input

When the serial port is enabled, SPE = 1 in I16, this pin is the serial data input.

CS9236 Wavetable Serial Port Interface

A digital interface to the CS9236 Single-Chip Wavetable Music Synthesizer is provided that allows the CS9236 PCM audio data to be summed on the CS4239 without the need for an external DAC. This serial port is enabled via the WTEN bit which is located in the Global Configuration byte in the E^2PROM Hardware Configuration data, or C8. The CS9236 Wavetable serial port pins are shared with the CS4610 DSP serial interface. If the CS4610 serial interface is enabled, the CS9236 interface is not available (SPE takes precedence over WTEN).

SDATA - Wavetable Serial Audio Data, Input

This input supplies the serial audio PCM data to be mixed on the CS4239. The data consists of left and right channel 16-bit data delineated by LRCLK. This pin should be connected to the SOUT output pin on the CS9236. This pin should also have a weak pull-down resistor of approx. 100 kΩ to minimize power-down currents and allow for stuffing options.

LRCLK - Wavetable Serial Left/Right Clock, Input

This input supplies the serial data alignment signal that delineates left from right data. This pin should be connected to the LRCLK output pin on the CS9236. This pin should also have a weak pull-down resistor of approx. 100 kΩ to minimize power-down currents and allow for stuffing options.

MCLK - Wavetable Master Clock, Output (CDROM Enable)

This output supplies the 16.9344 MHz master clock that controls all the timing on the CS9236. This pin should be connected to the MCLK5I input pin on the CS9236. MCLK can be disabled in software using the DMCLK bit in C8 in the Control logical device space. DMCLK provides a partial software power-down mode for the CS9236. At power-up, this pin is an input (with an internal 100 kΩ pullup) that, when pulled low with a 10 kΩ resistor to SGND, enables the CDROM interface (in lieu of the upper four ISA address pins). Loading must be limited to CMOS inputs if this pin has the 10 kΩ resistor attached.

ZVPORT Serial Port Interface

ZSDATA - ZV Port Serial Data, Input

When the ZV port is enabled, ZVEN = 1 in X18, this pin is the serial data input.

ZLRCLK - ZV Port Left/Right Clock, Input

When the ZV port is enabled, ZVEN = 1 in X18, this pin is the Left/Right channel delineation clock input.

ZSCLK - ZV Port Serial Clock, Input

When the ZV port is enabled, ZVEN = 1 in X18, this pin is the serial data bit clock input.

CDROM Interface

The four CDROM pins are multi-function and default to ISA upper address bits SA12-SA15. To enable the CDROM port, an external 10 kΩ resistor must be tied between MCLK/SCLK and SGND. MCLK/SCLK is sampled on the falling edge of RESDRV. The alternate CDROM chip select has its own strapping option to enable ACDCS. Use of the CDROM interface requires a 1 k E^2PROM to support the Plug-and-Play data as well as firmware patch data.

CDCS - CDROM Chip Select, Output, 4 mA drive

This output goes low whenever an address is decoded that matches the value programmed into the CDROM base address register.

ACDCS - Alternate CDROM Chip Select, Output, 4 mA drive

This pin, XCTL1/ACDCS/DOWN, is multiplexed with two other functions, and defaults to the XCTL1 output which is controlled by the XCTL1 bit in the WSS I10. This pin can also be configured at a second CDROM Chip Select, ACDCS, to support the alternate IDE CDROM decode. To force this pin to the CDROM alternate chip select, an external 10 kΩ resistor must be tied between SDOUT and SGND. ACDCS output then goes low whenever an address is decoded that matches the value programmed into the CDROM alternate base address register, ACDbase. This pin can also be used as the volume up pin DOWN by setting VCEN in Control register C0 or the Hardware Configuration data. VCEN has the highest precedence over the other pin functions.

CDINT - CDROM Interrupt, Input

This pin is used to input an interrupt signal from the CDROM interface. The part can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus interrupt line. The polarity if this input can be programmed through CTRLbase+1 register, bit ICH, or the Hardware Configuration data; the default is active high.

CDRQ - CDROM DMA Request, Input

This pin can be used to input the DMA request signal from the CDROM interface. The part can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus DRQ line.

CDACK- CDROM DMA Acknowledge, Output, 4 mA drive

This pin can be used to output the ISA bus-generated DMA acknowledge signal to the CDROM interface.

Volume Control

The volume control pins are enabled by setting VCEN in the Hardware Configuration data, Misc. Hardware Config. byte. The VCF1 bit in the Hardware Configuration data, Global Configuration byte, set the format for the volume control pins. Typically a 100 Ω series resistor and a 10 nF capacitor (required) to ground, capacitor on the switch side of the series resistor, would be included on each pin for ESD protection and to help with EMI emissions.

$\overline{\text{UP}}$ - Volume Up - Internal Pullup

This pin is enabled when VCEN is set. When $\overline{\text{UP}}$ is low, the master volume output for left and right channels are incremented. A 10 nF capacitor to ground is required for switch debounce.

$\overline{\text{DOWN}}$ - Volume Down - Internal Pullup

The XCTL1/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$ is a multiplexed pin that can be used as XCTL1, the alternate CDROM chip select, or the Volume Down pin. This pin is switched to the $\overline{\text{DOWN}}$ function when VCEN is set. When $\overline{\text{DOWN}}$ is low, the master volume output for left and right channels are decremented. A 10 nF capacitor to ground is required for switch debounce.

$\overline{\text{MUTE}}$ - Volume Mute - Internal Pullup

The $\overline{\text{MUTE}}$ pin function can be momentary, or non-existent based on the VCF1 bit. The $\overline{\text{MUTE}}$ function is enabled when VCEN is set. A 10 nF capacitor to ground is required for switch debounce.

Miscellaneous

XTALI - Crystal Input

This pin will accept either a crystal, with the other pin attached to XTALO, or an external CMOS clock. XTAL must have a crystal or clock source attached for proper operation. The crystal frequency must be 16.9344 MHz and designed for fundamental mode, parallel resonance operation.

XTALO - Crystal Output

This pin is used for a crystal placed between this pin and XTALI. If an external clock is used on XTALI, this pin must be left floating with no traces or components connected to it.

APSEL - Address Port Select, Input

This pin has an internal pull-up of approximately 100 kΩ. Leaving this pin in its default condition, places the PnP/Crystal Key Address Port at the standard PnP address of 279h (hex). For Motherboard applications, APSEL can be tied to SGND, which will change the Address Port to one of two other addresses, chosen by a strapping option on pin SCL. When RESDRV goes inactive, pin SCL is forced to an input and sampled. When SCL is sampled high (default), the Address Port changes to address 308h. When SCL is sampled low, the Address Port changes to 388h. Add-in cards should leave APSEL unconnected.

TEST - Test

This pin must be tied to ground for proper operation.

Power Supplies

VA - Analog Supply Voltage

Supply to the analog section of the codec.

AGND - Analog Ground

Ground reference to the analog section of the codec. This pin should be placed on an analog ground pin separate from other chip grounds.

VD1 - ISA Digital Supply Voltage

Digital supply for the parallel data bus pins. This pin can be connected to either 3.3 V or 5 V power supply. When connected to a 3.3 V supply, all ISA bus pins must also be at 3.3 V.

DGND1 - ISA Digital Ground

Digital ground reference for the parallel data bus pins. These pins are isolated from the other grounds and should be connected to the digital ground section of the board (see Figure 25).

VDF1, VDF2, VDF3 - Digital Filtered Supply Voltage

Digital supply for the internal digital section of the codec (except for the parallel data bus). These pins should be filtered, using a ferrite bead, from VD1.

SGND1, SGND2, SGND3, SGND4 - Internal Digital Ground

Ground reference for the internal digital section of the codec. Optimum layout is achieved by placing SGND1/2/3/4 on the digital ground plane with the DGND pin as shown in Figure 25.

PARAMETER DEFINITIONS

Frequency Response

Frequency Response is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

Total Dynamic Range

TDR is the ratio of the RMS sum of the lowest obtainable noise floor, in the presence of a signal, divided by the RMS full-scale signal level. The lowest obtainable noise floor is defined as the noise floor measured with the attenuation bits for the volume control at full attenuation - without muting. Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A. (dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.)

Instantaneous Dynamic Range or Dynamic Range

IDR or DR is the ratio of the RMS sum of the noise floor, in the presence of a signal, divided by the RMS full-scale signal level, available at any instant in time (no change in gain settings between measurements). Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A. (dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.)

Total Harmonic Distortion plus Noise

THD+N is the ratio of the RMS sum of all non-fundamental frequency components, divided by the RMS full-scale signal level. Tested using a -3 dB FS input signal. Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A. (dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.)

Interchannel Isolation

The ratio of signal level on the tested channel divided by the stimulus channel level. For inputs, the tested input channel is terminated with 50 Ω. For outputs, the tested channel is fed digital zeros. Units in dB.

Interchannel Gain Mismatch

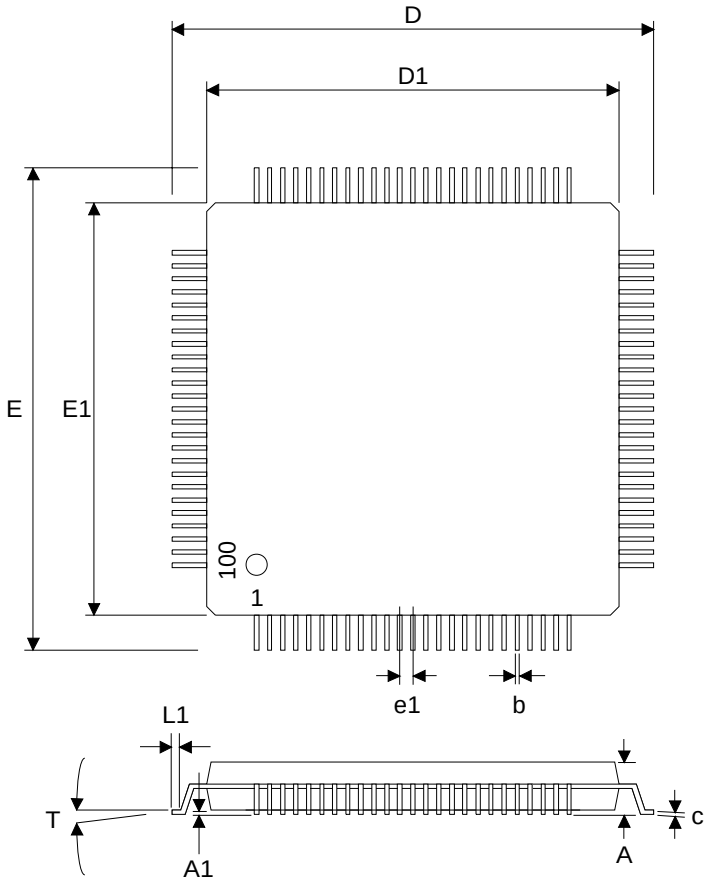
For the ADCs, the difference in input voltage to get an equal code on both channels. For the DACs, the difference in output voltages for each channel when both channels are fed the same code. Units in dB.

PATHS:

A-D-PC: Analog in, through ADC, onto PC bus
PC-D-A: PC bus, through DAC, to analog out
A-A: Analog in to Analog out (analog output mixer)

Detailed information on audio testing and paths can be found in *Personal Computer Audio Quality Measurements* document by Dr. Steven Harris and Clif Sanchez, located at the following web address: http://www.cirrus.com/products/papers/meas/meas.html.

PACKAGE PARAMETERS



100-pin TQFP - Package Code 'Q'

Symbol	Description	MIN	NOM	MAX
N	Lead Count		100	
A	Overall Height			1.66
A1	Stand Off	0.00		
b	Lead Width	0.14	0.20	0.26
c	Lead Thickness	0.077	0.127	0.177
D	Terminal Dimension	15.70	16.00	16.30
D1	Package Body		14.0	
E	Terminal Dimension	15.70	16.00	16.30
E1	Package Body		14.0	
e1	Lead Pitch	0.40	0.50	0.60
L1	Foot Length	0.30	0.50	0.70
T	Lead Angle	0.0°		12.0°

Notes:
1) Dimensions in millimeters.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm.
3) Coplanarity is 0.004 in.
4) Lead frame material is AL-42 or copper, and lead finish is solder plate.
5) Pin 1 identification may be either ink dot or dimple.
6) Package top dimensions can be smaller than bottom dimensions by 0.20 mm.
7) The "lead width with plating" dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
8) Ejector pin marks in molding are present on every package.

APPENDIX A: DEFAULT PnP DATA

```
; EEPROM Validation Bytes
  DB       055H, 0BBH                ; EEPROM Validation Bytes: CS4239

  DB       001H                       ; EEPROM data length upper byte
  DB       014H                       ; lower byte, Listed Size = 276

; Hardware Configuration Data
  DB       000H                       ; ACDbase Addr. Mask Length = 1 bytes
  DB       003H                       ;
  DB       080H                       ; MCB: IHCD
  DB       080H                       ; GCB1: IFM
  DB       005H                       ; Code Base Byte
  DB       020H                       ; FM Scaling 0 dB
  DB       004H                       ; RESERVED
  DB       008H                       ; RESERVED
  DB       010H                       ; RESERVED
  DB       080H                       ; M+DSP: MIM
  DB       000H                       ;
  DB       000H                       ; GCB2: No Bits Set

; Hardware Mapping Data
  DB       004H                       ; CDbase Length = 4
  DB       048H                       ; RESERVED
  DB       075H                       ; IRQ selection A & B - B= 7,  A=5
  DB       0B9H                       ; IRQ selection C & D - D=11,  C=9
  DB       0FCH                       ; IRQ selection E & F - F=15,  E=12
  DB       010H                       ; DMA selection A & B - B= 1,  A=0
  DB       003H                       ; DMA C,IRQ G select. - G= 0,  C=3

; PnP Resource Header - PnP ID for CS4236 IC, OEM ID = 42
  DB       00EH, 063H, 042H, 036H, 0FFH,0FFH,0FFH,0FFH,0A9H  ; CSC4236 FFFFFFFF
  DB       00AH, 010H, 005H          ; PnP version 1.0, Vendor version 0.5
  DB       082H, 00EH, 000H, 'Crystal Codec', 000H ; ANSI ID

; LOGICAL DEVICE 0 (Windows Sound System & SBPro)
  DB       015H, 00EH, 063H, 000H, 000H, 000H ; EISA ID: CSC0000

  DB       082H, 007H, 000H, 'WSS/SB', 000H ; ANSI ID
  DB       031H, 000H                 ; DF Best Choice
  DB       02AH, 002H, 028H          ; DMA: 1   - WSS & SBPro
  DB       02AH, 009H, 028H          ; DMA: 0,3  - WSS & SBPro capture
  DB       022H, 020H, 000H          ; IRQ: 5  Interrupt Select 0
  DB       047H, 001H, 034H, 005H, 034H, 005H, 004H, 004H ;16b WSSbase: 534
  DB       047H, 001H, 088H, 003H, 088H, 003H, 008H, 004H ;16b SYNbase: 388
  DB       047H, 001H, 020H, 002H, 020H, 002H, 020H, 010H ;16b SBbase: 220

  DB       031H, 001H                 ; DF Acceptable Choice 1
  DB       02AH, 00AH, 028H          ; DMA: 1,3  - WSS & SBPro
  DB       02AH, 00BH, 028H          ; DMA: 0,1,3  - WSS & SBPro capture
  DB       022H, 0A0H, 09AH          ; IRQ: 5,7,9,11,12,15  Interrupt Select 0
```

```
  DB       047H, 001H, 034H, 005H, 0FCH, 00FH, 004H, 004H ;16b WSSbase: 534-FFC
  DB       047H, 001H, 088H, 003H, 088H, 003H, 008H, 004H ;16b SYNbase: 388
  DB       047H, 001H, 020H, 002H, 060H, 002H, 020H, 010H ;16b SBbase: 220-260

  DB       031H, 002H                ; DF Suboptimal Choice 1
  DB       02AH, 00BH, 028H          ; DMA: 0,1,3  - WSS & SBPro
  DB       022H, 0A0H, 09AH          ; IRQ: 5,7,9,11,12,15  Interrupt Select 0
  DB       047H, 001H, 034H, 005H, 0FCH, 00FH, 004H, 004H ;16b WSSbase: 534-FFC
  DB       047H, 001H, 088H, 003H, 0F8H, 003H, 008H, 004H ;16b SYNbase: 388-3F8
  DB       047H, 001H, 020H, 002H, 000H, 003H, 020H, 010H ;16b SBbase: 220-300

  DB       038H                      ; End of DF for Logical Device 0


; LOGICAL DEVICE 1 (Game Port)
  DB       015H, 00EH, 063H, 000H, 001H, 000H ; EISA ID: CSC0001

  DB       082H, 005H, 000H, 'GAME', 000H ; ANSI ID
  DB       031H, 000H                ; DF Best Choice
  DB       047H, 001H, 000H, 002H, 000H, 002H, 008H, 008H ;16b GAMEbase: 200

  DB       031H, 001H                ; DF Acceptable Choice 1
  DB       047H, 001H, 008H, 002H, 008H, 002H, 008H, 008H ;16b GAMEbase: 208

  DB       038H                      ; End of DF for Logical Device 1


; LOGICAL DEVICE 2 (Control)
  DB       015H, 00EH, 063H, 000H, 010H, 000H ; EISA ID: CSC0010

  DB       082H, 005H, 000H, 'CTRL', 000H ; ANSI ID
  DB       047H, 001H, 020H, 001H, 0F8H, 00FH, 008H, 008H ;16b CTRLbase: 120-FF8

; LOGICAL DEVICE 3 (MPU-401)
  DB       015H, 00EH, 063H, 000H, 003H, 000H ; EISA ID: CSC0003

  DB       082H, 004H, 000H, 'MPU', 000H ; ANSI ID
  DB       031H, 000H                ; DF Best Choice
  DB       022H, 000H, 002H          ; IRQ: 9  Interrupt Select 0
  DB       047H, 001H, 030H, 003H, 030H, 003H, 008H, 002H ;16b MPUbase: 330

  DB       031H, 001H                ; DF Acceptable Choice 1
  DB       022H, 000H, 09AH          ; IRQ: 9,11,12,15  Interrupt Select 0
  DB       047H, 001H, 030H, 003H, 060H, 003H, 008H, 002H ;16b MPUbase: 330-360

  DB       031H, 002H                ; DF Suboptimal Choice 1
  DB       047H, 001H, 030H, 003H, 0E0H, 003H, 008H, 002H ;16b MPUbase: 330-3E0

  DB       038H                      ; End of DF for Logical Device 3


  DB       079H, 09AH                ; End of Resource Data, Resource Size = 280
```

APPENDIX B: DIFFERENCES BETWEEN THE CS423xB AND THE CS4239

This part is designed to be hardware backwards compatible with some CS423xB designs, primarily motherboard applications. New drivers will be needed to support this part.

Hardware Pin Differences:

1. RFILT and LFILT capacitors are no longer needed and should be removed. On the CS4239, these pins are renamed FLTI and FLTO and should have a capacitor placed between them. They are used for the Crystal 3D Sound circuitry. Not populating this capacitor will not have any adverse affects on the part, but will result in non-optimum 3D Sound.
2. The external L/RLINE analog inputs are no longer supported. LLINE is now FLT3D and is used for the 3D Sound function. A 0.01 µF capacitor should be placed between this pin and analog ground. When external analog wavetable is desired, the AUX1 analog inputs should be used.
3. The analog microphone inputs are now mono. LMIC is changed to MIC, and RMIC has been removed.
4. Mono Out, MOUT, has been removed. The pin is redefined as APSEL and used to change the Address Port. APSEL has an internal pullup, setting the Address Port to 0x279 for backwards compatibility.
5. VDF4 has been changed to IRQG - a seventh interrupt (typically used for INT 10). The default is disabled to provide backwards compatibility.
6. The Modem Logical Device has been removed. This includes $\overline{\text{MCS}}$ and $\overline{\text{MINT}}$.
7. Support for an external synthesizer has been removed. This includes $\overline{\text{SCS}}$ and $\overline{\text{SINT}}$.
8. The peripheral port has been removed. This includes XD<7:0>, $\overline{\text{XIOR}}$, $\overline{\text{XIOW}}$, XA<0:2>. CDROM applications must now drive the ISA bus directly or through buffers.
9. The hardware strap enable for the CDROM has been moved. CS423xB designs have a pulldown on $\overline{\text{XIOR}}$. To support the CDROM interface on the CS4239, the pulldown must be moved to the MCLK/SCLK pin. Also, to enable the alternate CDROM chip select pin $\overline{\text{ACDCS}}$, a pulldown must be added to pin SDOUT.
10. The DSP serial port is no longer supported as an option on the 2nd Joystick connector or on pins 4 through 7. The DSP port has moved to pins 1, 2, 3, 5 and is multiplexed with the CS9236 wavetable pins.
11. The consumer IEC-958 (S/PDIF) output, supported on the CS4237B and CS4238B, has been removed.
12. Only two modes of Hardware Volume Control are supported: 2-button, and 3-button with momentary mute. In addition, a 10 nF capacitor to ground is required for switch debounce on the CS4239.
13. Pullup resistors for the Joystick buttons, Hardware Volume Control pins, and the MIDIN pin are no longer required as they are internal to the CS4239.

• Notes •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