1.25-W Mono Fully Differential Audio Power Amplifier with 1.8V Input Logic Thresholds

DESCRIPTION

The EUA6205 is a mono fully-differential audio amplifier, capable of delivering 1.25W of continuous average power to an 8Ω BTL load with less than 1% THD+N from a 5V power supply, and 630mW to an 8Ω load from a 3.6V power supply. The Shutdown pin is fully compatible with 1.8V logic GPIO, such as are used on low power cellular chipsets.

Features like 85-dB PSRR from 90 Hz to 5 kHz, improved RF-rectification immunity, and small PCB area makes the EUA6205 ideal for wireless handsets.

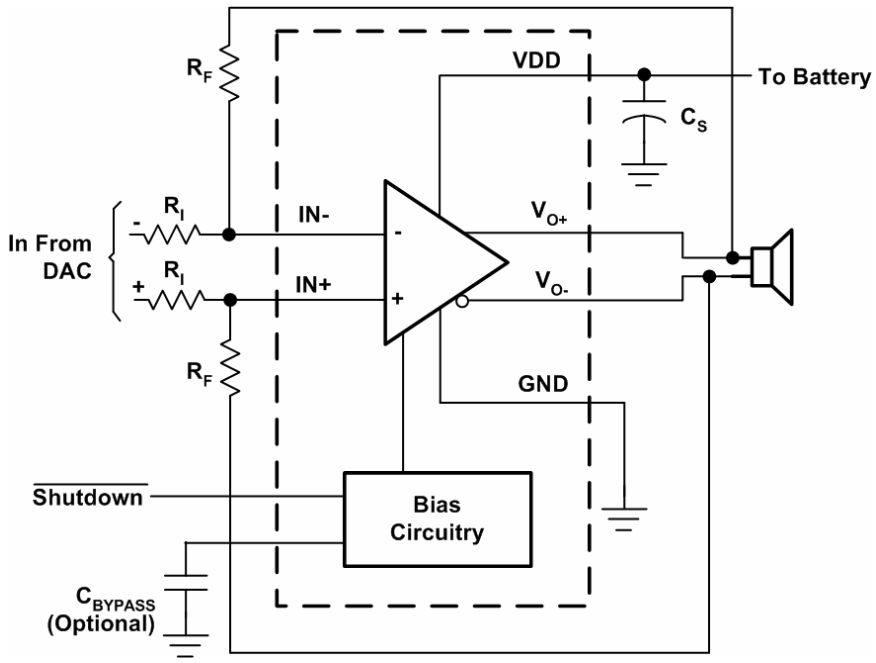
FEATURES

- Supply Voltage 2.5V to 5.5V
- 1.25W into 8Ω from a 5-V Supply at THD=1% (typ)
- Shutdown Pin has 1.8V Compatible Thresholds
- Low Supply Current: 3.4mA Typical
- Shutdown Current < 10μA
- Only Five External Components
  - Improved PSRR (87dB) for Direct Battery Operation
  - Full Differential Design Reduces RF Rectification
  - Improved CMRR Eliminates Two Input Coupling Capacitors
- Available in 3mm*3mm TDFN-8 and Thermally Enhanced MSOP-8 Packages
- RoHS Compliant and 100% Lead (Pb)-Free

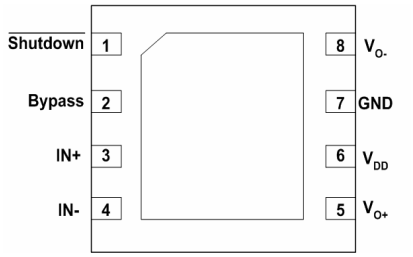
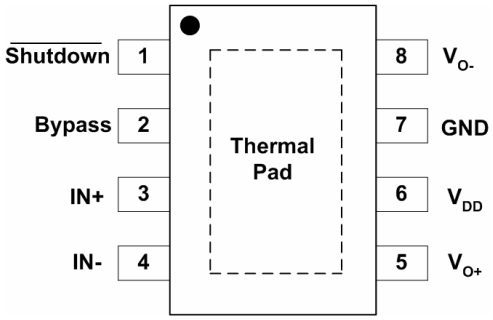
APPLICATIONS

- Wireless Handsets, PDAs, and other mobile devices

Typical Application Circuit



Pin Configurations

Package Type	Pin Configurations
TDFN-8	
MSOP-8 (FD)	

Pin Description

PIN	PIN	DESCRIPTION
$\overline{\text{Shutdown}}$	1	Shutdown terminal (active low logic)
Bypass	2	Mid-supply voltage. Adding a bypass capacitor improves PSRR
IN+	3	Positive differential input
IN-	4	Negative differential input
VO+	5	Positive BTL output
VDD	6	Supply voltage terminal
GND	7	High-current ground
VO-	8	Negative BTL output

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA6205JIR1	TDFN-8	xxxx 6205	-40°C to 85°C
EUA6205MIR1	MSOP-8	xxxx 6205	-40°C to 85°C

EUA6205 □ □ □ □

Lead Free Code
1: Lead Free 0: Original

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TDFN
M: MSOP

Absolute Maximum Ratings

- Supply Voltage, V_{DD} ---------- -0.3 V to 6V
- Input Voltage, V_I ---------- -0.3 V to V_{DD} + 0.3V
- Storage Temperature rang, T_{stg} ---------- -65°C to 85°C
- ESD Susceptibility ---------- 2kV
- Junction Temperature ---------- -40°C to 125°C
- Thermal Resistance

  θ_{JA} (MSOP-FD) ---------- 56°C/W

  θ_{JA} (TDFN) ---------- 50°C/W

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	2.5		5.5	V
High-level input voltage, V_{IH}	1.15			V
Low-level input voltage, V_{IL}			0.5	V
Common-mode input voltage, V_{IC}	0.5		V_{DD}-0.8	V
Operating free-air temperature, T_A	-40		85	°C

Electrical Characteristics, T_A=25°C Gain=1V/V

Symbol	Parameter	Conditions		EUA6205			Unit
				Min	Typ	Max.	
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_I = 0V, V_{DD} = 2.5V to 5.5V				9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5V to 5.5V			-84	-67	dB
CMRR	Common mode rejection range	V_{DD} = 5.5V, V_{IC} = 0.5V to V_{DD}-0.8			-79	-57	dB
		V_{DD} = 3.6V, V_{IC} = 0.5V to V_{DD}-0.8			-79	-60	
		V_{DD} = 2.5V, V_{IC} = 0.5V to V_{DD}-0.8			-66		
V_{OL}	Low-level output voltage	R_L = 8Ω, V_{IN+} = V_{DD}, V_{IN-} = 0V or V_{IN+} = 0V, V_{IN-} = V_{DD}	V_{DD}=5.5V		0.29	0.46	V
			V_{DD}=3.6V		0.21		
			V_{DD}=2.5V		0.17	0.26	
V_{OH}	High-level output voltage	R_L = 8Ω, V_{IN+} = V_{DD}, V_{IN-} = 0V or V_{IN+} = 0V, V_{IN-} = V_{DD}	V_{DD}=5.5V	4.8	5.1		V
			V_{DD}=3.6V		3.3		
			V_{DD}=2.5V	2.1	2.25		
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5V, V_I = 5.8V				1.2	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5V, V_I = -0.3V				1.2	µA
I_{DD}	Supply current	V_{DD} = 2.5V to 5.5V, no load, $\overline{\text{Shutdown}}$ = V_{IH}			3.4		mA
$I_{DD\,(SD)}$	Supply current in shutdown mode	$\overline{\text{Shutdown}}$ = V_{IL}, VDD = 2.5V to 5.5V, No load			0.02		µA

Operating Characteristics, T_A=25°C, Gain=1V/V, R_L = 8Ω

Symbol	Parameter	Conditions		EUA6205			Unit
				Min	Typ	Max.	
P_O	Output power	THD + N = 1%, f = 1kHz	V_{DD} = 5.5V		1.25		W
			V_{DD} = 3.6V		0.63		
			V_{DD} = 2.5V		0.3		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5V, P_O = 1W, f = 1kHz			0.067		%
		V_{DD} = 3.6V, P_O = 0.5W, f = 1kHz			0.065		
		V_{DD} = 2.5V, P_O = 200mW, f = 1kHz			0.077		
K_{SVR}	Supply ripple rejection ratio	$C_{(BYPASS)}$ = 0.47µF, V_{DD} = 5.5V C_I = 2µF	f = 217 Hz to 2 kHz		-87.1		dB
		$C_{(BYPASS)}$ = 0.47µF, V_{DD} = 3.6V C_I = 2µF	f = 217 Hz to 2 kHz		-86.5		
		$C_{(BYPASS)}$ = 0.47µF, V_{DD} = 2.5V C_I = 2µF	f = 217 Hz to 2 kHz		-64		
SNR	Signal-to-noise ratio	V_{DD} = 5V, P_O = 1W			108		dB
Vn	Output voltage noise	f = 20 Hz to 20 kHz	No weighting		10		μV_{RMS}
			A weighting		8		
CMRR	Common mode rejection ratio	V_{DD} = 5.5V,Gain = 4V/V, V_{ICM} = 200mVpp	f = 20 Hz to 1 kHz		-71.6		dB
		V_{DD} = 3.6V,Gain = 4V/V, V_{ICM} = 200mVpp	f = 20 Hz to 1 kHz		-71.9		
		V_{DD} = 2.5V,Gain = 4V/V, V_{ICM} = 200mVpp	f = 20 Hz to 1 kHz		-60		
Z_I	Input impedance				2		MΩ
Z_O	Output impedance	Shutdown mode		>10k			
	Shutdown attenuation	f = 20 Hz to 20 kHz, R_F = R_I = 20 kΩ			-79		dB

Typical Operating Characteristics

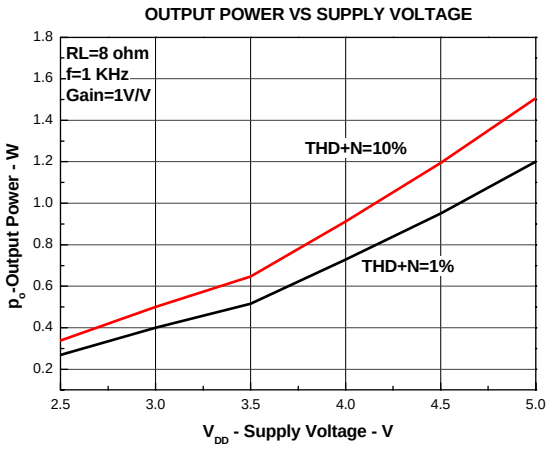


Figure 1.

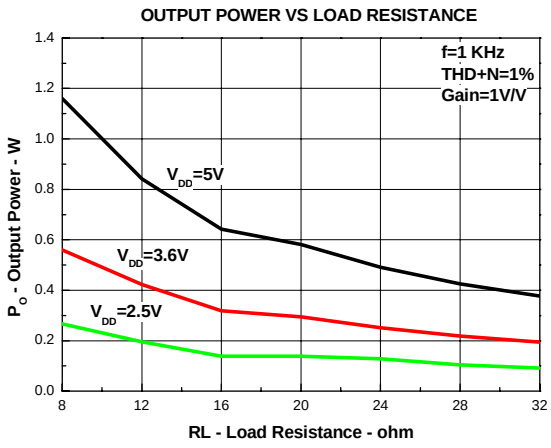
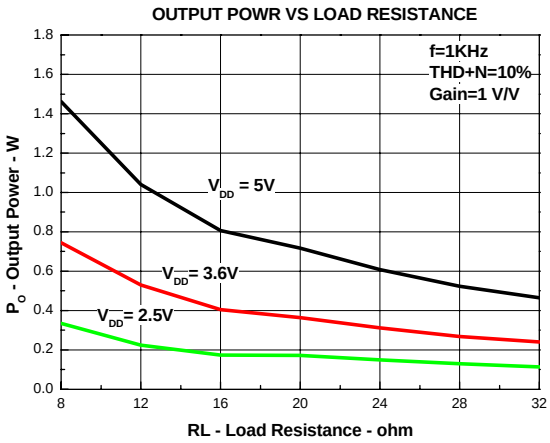


Figure 2.



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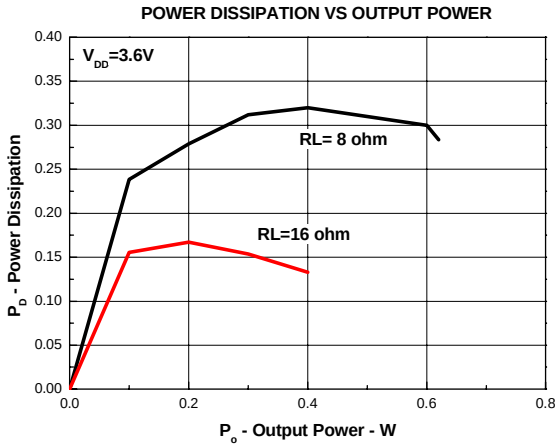

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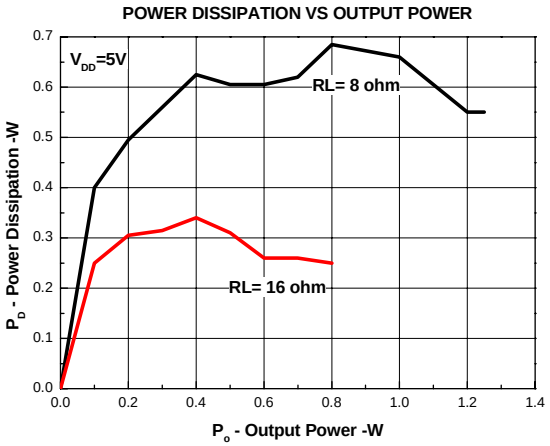

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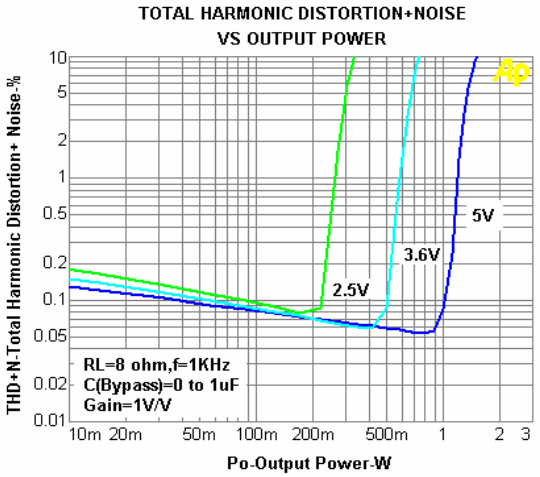

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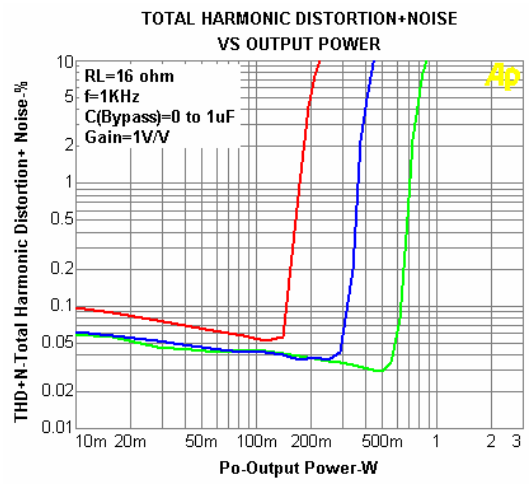

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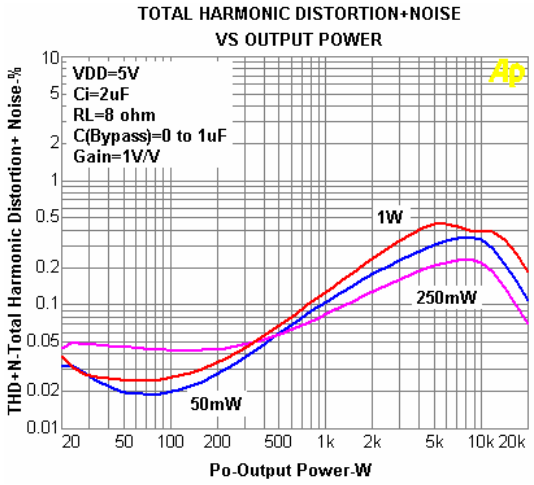

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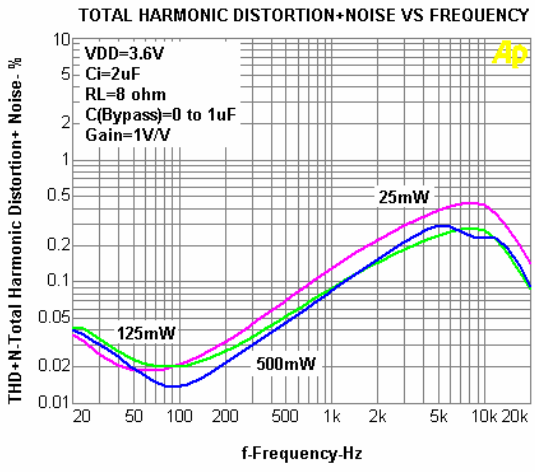

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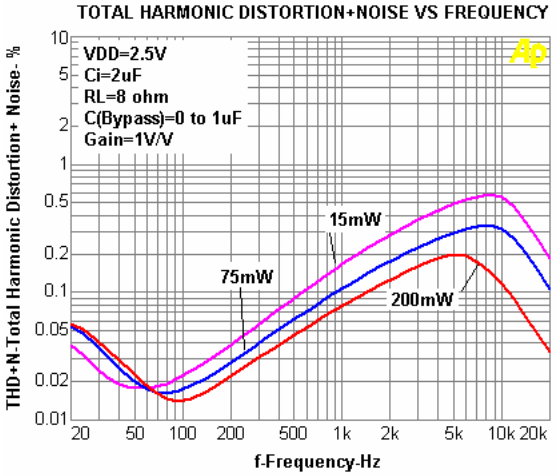

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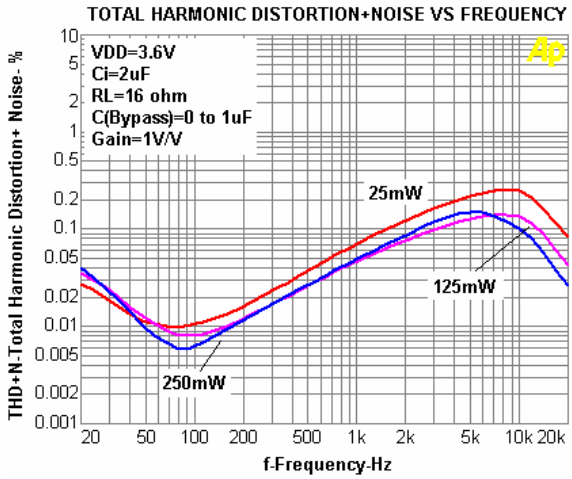

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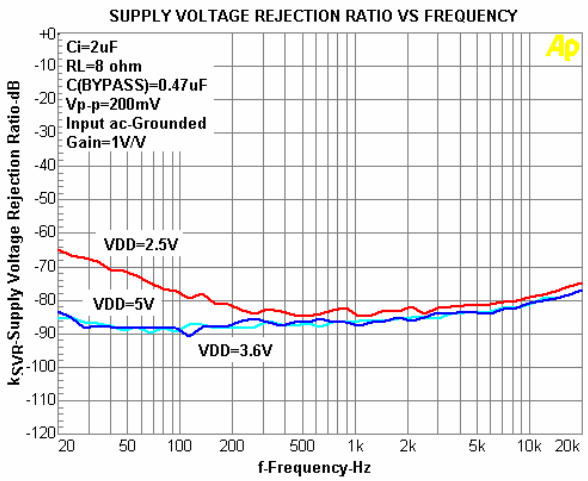

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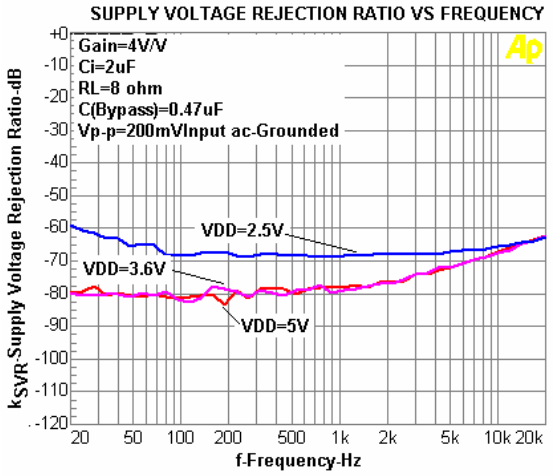

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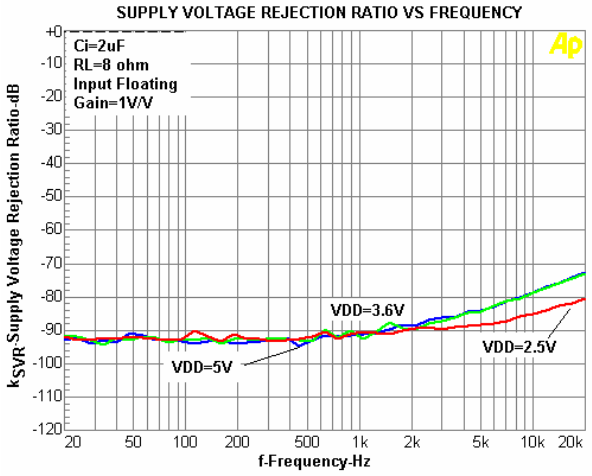

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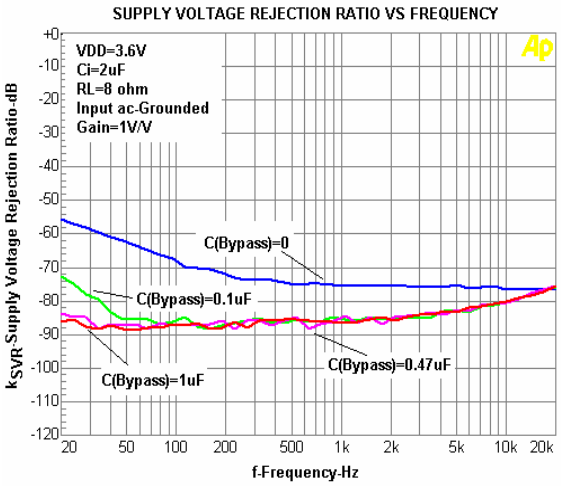

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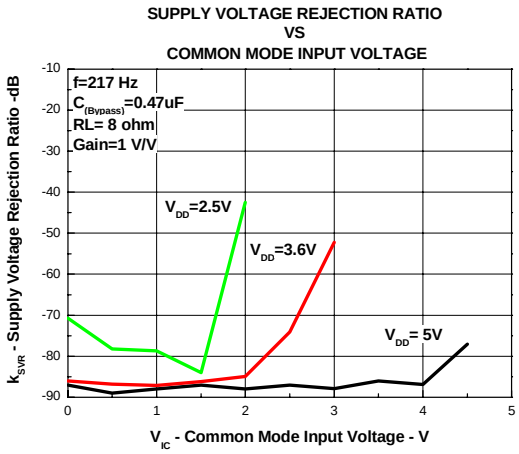

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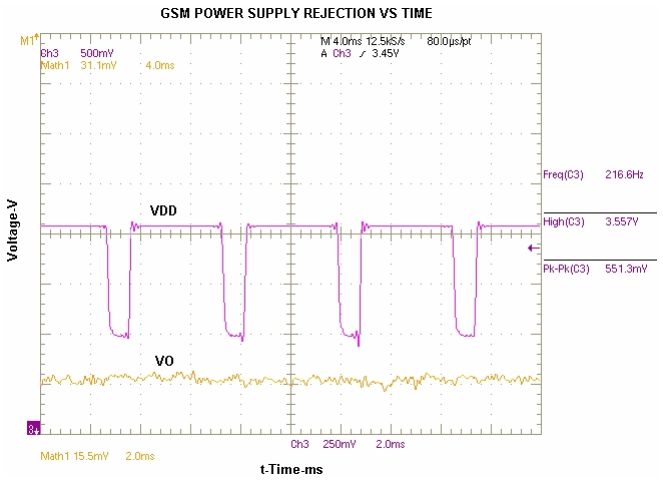

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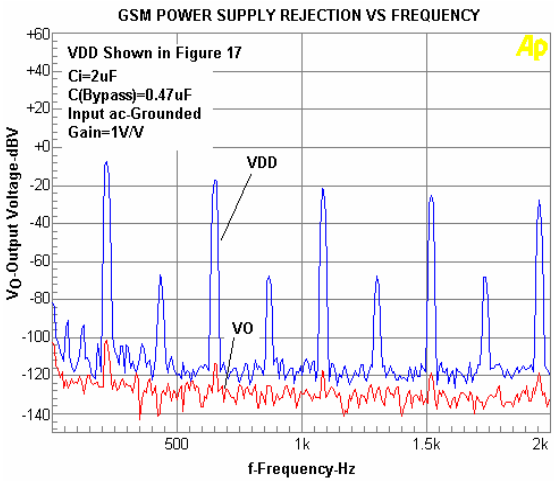
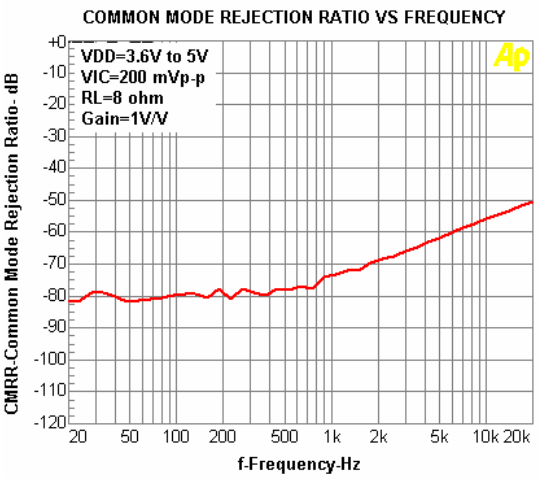


Figure 18.



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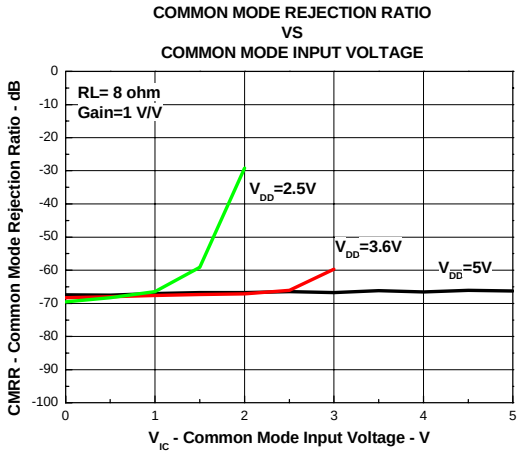

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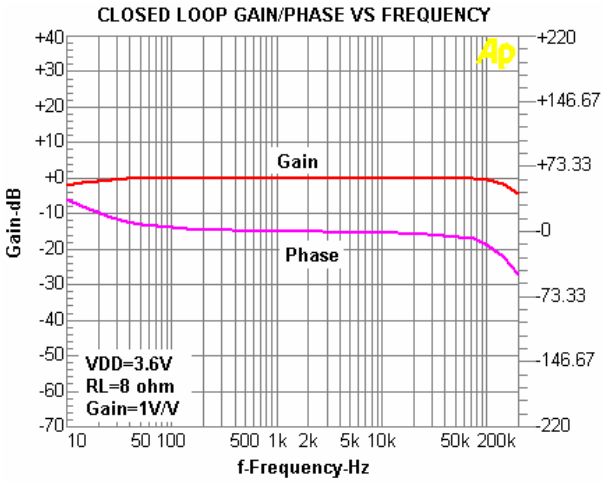

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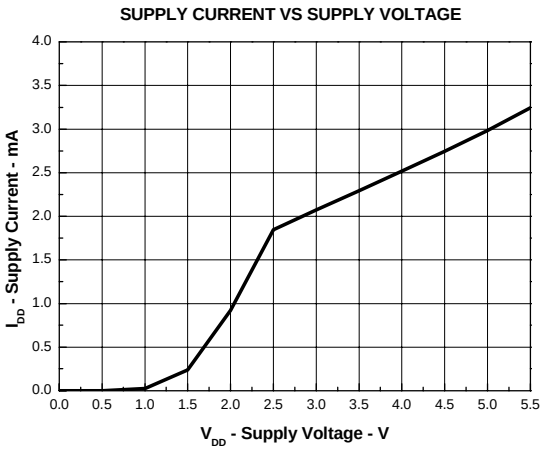


Figure 22.

Application Information

Application Schematics

Figure23 through Figure26 show application schematics for differential and single-ended inputs. Typical values are shown in Table1.

Table1. Typical Component Value

Component	Value
R_I	10kΩ
R_F	10kΩ
$C_{(BYPASS)}$	0.22μF
C_S	1μF
C_I	0.22μF

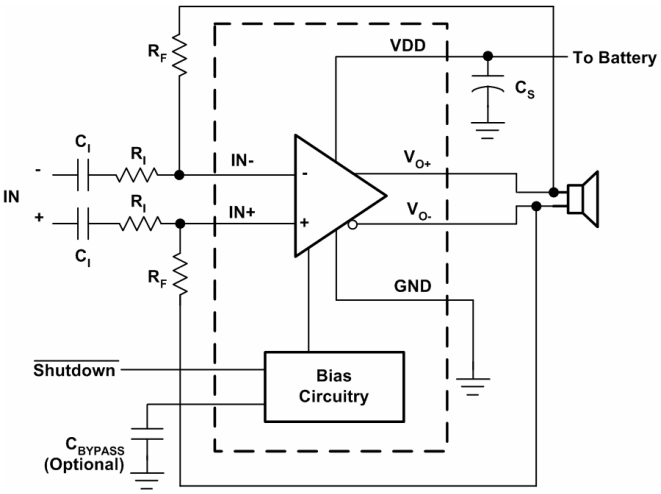


Figure 23. Differential Input Application Schematic Optimized With Input Capacitors

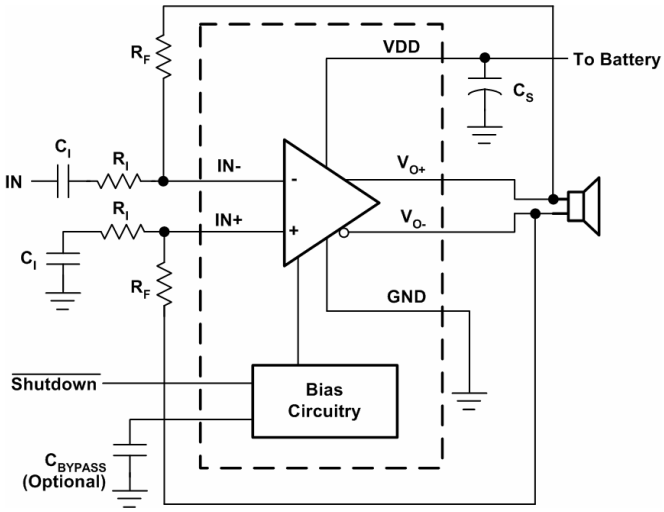


Figure 24. Single-Ended Input Application Schematic

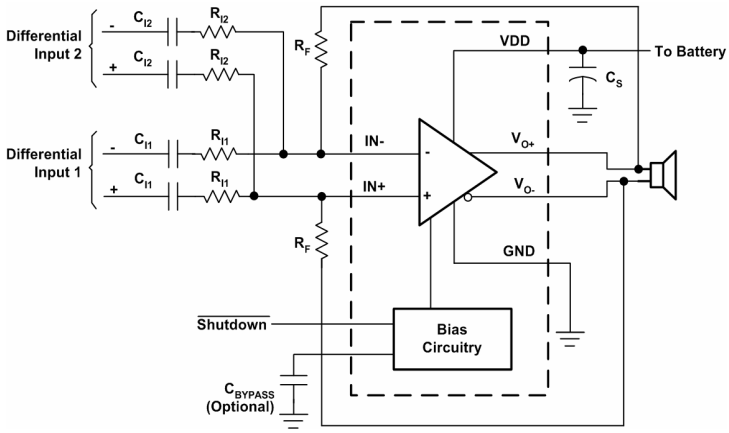


Figure 25. Application Schematic With Summing Two Differential Inputs

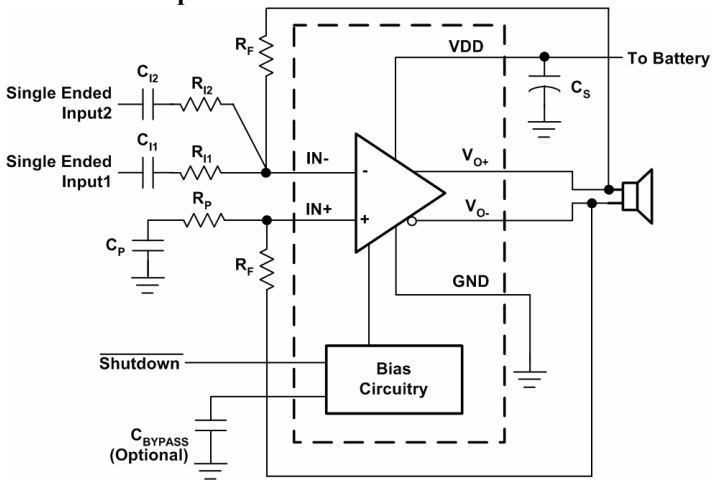


Figure 26. Application Schematic With Summing Two Single-Ended Inputs

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the EUA6205 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs of from equation1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \text{ ----------(1)}$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determine from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the

thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the EUA6205. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

Selection Components

Resistors (R_F and R_I)

The input (R_I) and feedback resistors (R_F) set the gain of the amplifier according to Equation 2.

$$Gain = R_F/R_I \quad \text{----------(2)}$$

R_F and R_I should range from 1kΩ to 100kΩ. Most graphs were taken with R_F=R_I=20 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched rations of resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

Bypass Capacitor (C_{BYPASS}) and Start-Up Time

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases the k_{SVR}. $C_{(BYPASS)}$also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Although the output rise time depends on the bypass capacitor value, the device passes audio 4 µs after taken out of shutdown and the gain is slowly ramped up based
on $C_{(BYPASS)}$.

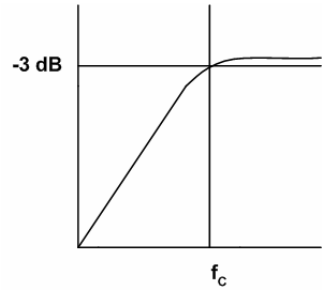
To minimize pops and clicks, design the circuit so the impedance (resistance and capacitance) detected by both inputs, IN+ and IN-, is equal.

Input Capacitor (C_I)

The EUA6205 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to V_{DD} - 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 3.

$$f_C = \frac{1}{2\pi R_I C_I} \quad \text{---------- (3)}$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 2 is reconfigured as Equation 4.

$$C_I = \frac{1}{2\pi R_I f_C} \quad \text{---------- (4)}$$

In this example, C_I is 0.16µF, so one would likely choose a value in the range of 0.22µF to 0.47µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load.

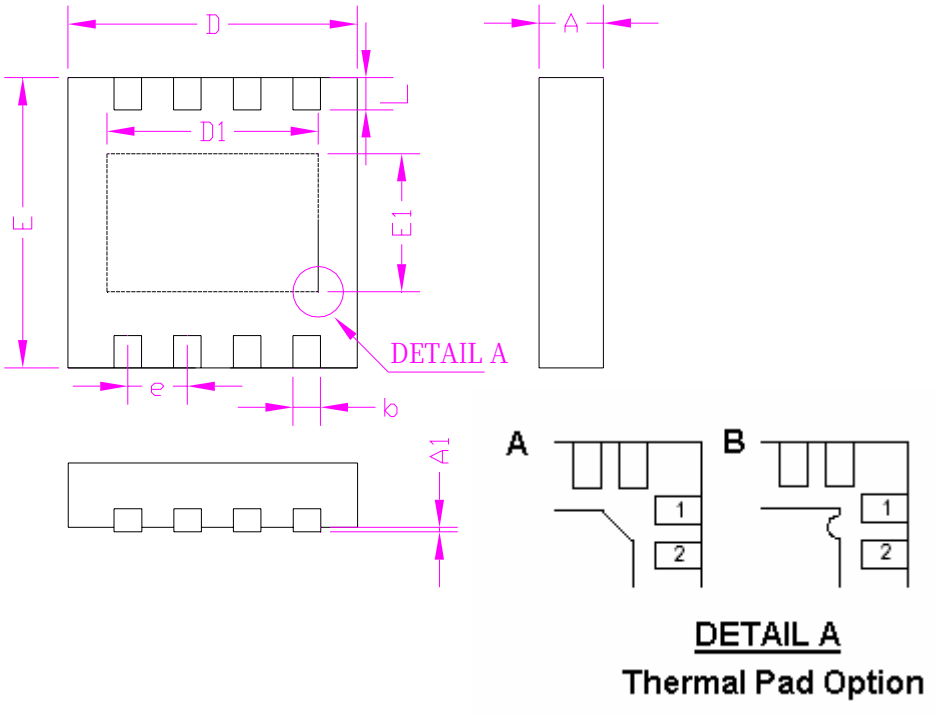
This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The EUA6205 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1 µF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

Package Information

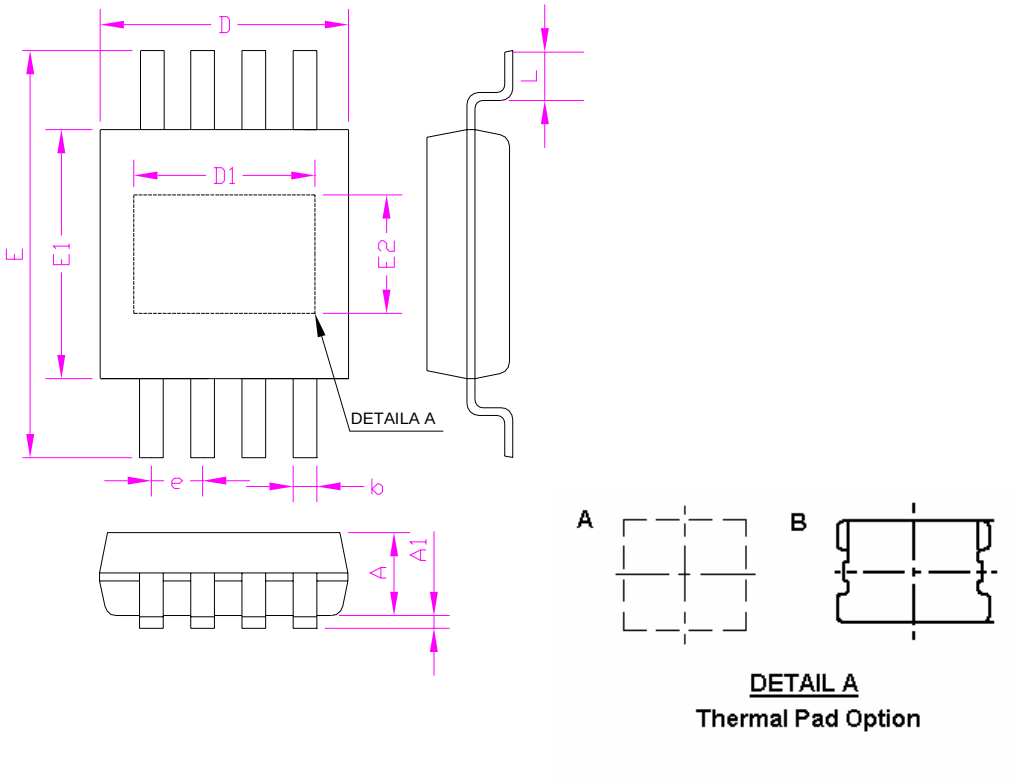
TDFN-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.40	0.008	0.016
D	2.90	3.10	0.114	0.122
D1	2.30		0.090	
E	2.90	3.10	0.114	0.122
E1	1.50		0.059	
e	0.65		0.026	
L	0.25	0.45	0.010	0.018

Package Information (continued)

MSOP-8 (FD)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
D	3.00		0.118	
E	4.70	5.10	0.185	0.201
E1	3.00		0.118	
D1	1.70		0.067	
E2	1.70		0.067	
L	0.40	0.80	0.016	0.031
b	0.22	0.38	0.008	0.015
e	0.65		0.026	