TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC4027BP,TC4027BF,TC4027BFN

### TC4027B Dual J-K Master-Slave Flip Flop

 $\rm TC4027B$  is J-K master-slave flip-flop having RESET and SET functions.

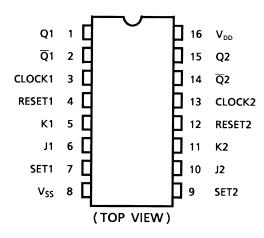
In the case of J-K made, when the clock input is given with both RESET and SET at "L", the output changes at rising edge of the clock according to the states of J and K.

When SET input is placed at "H", and RESET input is placed at "L", outputs become Q = "H", and  $\overline{Q} =$  "L".

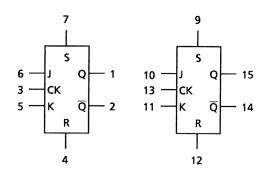
When RESET input is placed at "H", and SET input is placed at "L", outputs become Q = "L", and  $\overline{Q} = "H$ ".

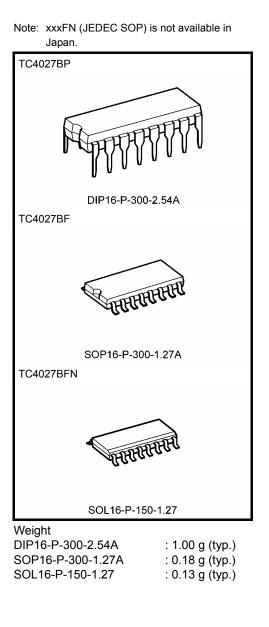
When both of RESET input and SET input are at "H", outputs become Q = "H" and  $\overline{Q} =$  "H".

### **Pin Assignment**



### **Block Diagram**





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### **Truth Table**

		Outputs					
RESET	SET	J	К	CLOCK∆	$Q_{n + 1}$	$\overline{Q}_{n+1}$	
L	Н	*	*	*	Н	L	
н	L	*	*	*	L	Н	
н	Н	*	*	*	Н	Н	
L	L	L	L		Q <sub>n*</sub>	Q <sub>n*</sub>	
L	L	L	Н		L	Н	
L	L	Н	L		Н	L	
L	L	Н	Н		Q <sub>n **</sub>	Q <sub>n**</sub>	
L	L	*	*		Q <sub>n*</sub>	Qn *	

\*: Don't care

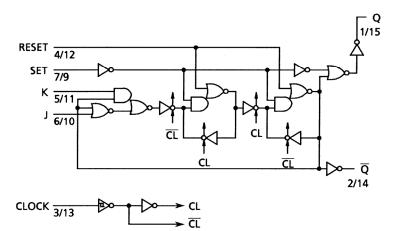
 $\Delta$ : Level change

\*: No change

\*\*: Change

### Logic Diagram

### 1/2 TC4027B



### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V <sub>DD</sub>	$V_{SS}{-}0.5$ to $V_{SS}{+}20$	V
Input voltage	VIN	$V_{\mbox{\scriptsize SS}}-0.5$ to $V_{\mbox{\scriptsize DD}}+0.5$	V
Output voltage	Vout	$V_{\mbox{\scriptsize SS}}-0.5$ to $V_{\mbox{\scriptsize DD}}+0.5$	V
DC input current	l <sub>IN</sub>	±10	mA
Power dissipation	PD	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C
Storage temperature range	T <sub>stg</sub>	–65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V<sub>SS</sub> = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V <sub>DD</sub>	—	3	_	18	V
Input voltage	V <sub>IN</sub>		0		V <sub>DD</sub>	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{DD}$  or  $V_{SS}$ .

### Static Electrical Characteristics ( $V_{SS} = 0 V$ )

Characteristics Symbol		Sym-	Test Condition		-40°C		25°C			85°C		
		bol		V <sub>DD</sub> (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit
			I <sub>OUT</sub>   < 1 μΑ V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	_	4.95	5.00		4.95	_	
High-level output voltage	V <sub>OH</sub>	10		9.95	—	9.95	10.00	_	9.95	—	V	
			VIN - VSS, VDD	15	14.95	_	14.95	15.00		14.95	_	
			I <sub>OUT</sub>   < 1 μΑ	5	_	0.05	_	0.00	0.05		0.05	
Low-level ov voltage	output	V <sub>OL</sub>	$V_{IN} = V_{SS}, V_{DD}$	10	—	0.05	—	0.00	0.05	—	0.05	V
Ŭ			VIN - VSS, VDD	15		0.05		0.00	0.05		0.05	
			V <sub>OH</sub> = 4.6 V	5	-0.61	—	-0.51	-1.0	_	-0.42	—	
			$V_{OH} = 2.5 V$	5	-2.50	—	-2.10	-4.0	_	-1.70	—	mA
Output hig	h current	IOH	V <sub>OH</sub> = 9.5 V	10	-1.50	—	-1.30	-2.2	_	-1.10	—	
			V <sub>OH</sub> = 13.5 V	15	-4.00	—	-3.40	-9.0	_	-2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$									
			V <sub>OL</sub> = 0.4 V	5	0.61	_	0.51	1.2	_	0.42	_	mA
Output lou	ourrent		$V_{OL} = 0.5 V$	10	1.50	—	1.30	3.2	_	1.10	—	
Output low current	I <sub>OL</sub>	V <sub>OL</sub> = 1.5 V	15	4.00	—	3.40	12.0	_	2.80	—	mA	
		$V_{IN} = V_{SS}, V_{DD}$										
		VIH	V <sub>OUT</sub> = 0.5 V, 4.5 V	5	3.5	_	3.5	2.75		3.5	_	v
la a chiada			V <sub>OUT</sub> = 1.0 V, 9.0 V	10	7.0	_	7.0	5.50	_	7.0	_	
Input high	voltage		V <sub>OUT</sub> = 1.5 V, 13.5 V	15	11.0	_	11.0	8.25	_	11.0	_	
			$ I_{OUT}  < 1 \ \mu A$									
			V <sub>OUT</sub> = 0.5 V, 4.5 V	5	_	1.5	_	2.25	1.5	_	1.5	
			V <sub>OUT</sub> = 1.0 V, 9.0 V	10	_	3.0	_	4.50	3.0		3.0	
Input low voltage	VIL	V <sub>OUT</sub> = 1.5 V, 13.5 V	15	_	4.0	_	6.75	4.0		4.0	V	
			$ I_{OUT}  < 1 \ \mu A$									
Input	"H" level	I <sub>IH</sub>	V <sub>IH</sub> = 18 V	18	_	0.1		10 <sup>-5</sup>	0.1		1.0	
current	"L" level	١ <sub>IL</sub>	$V_{IL} = 0 V$	18	_	-0.1		-10 <sup>-5</sup>	-0.1		-1.0	μA
Ouiococci	oupple				_	1		0.002	1		30	
Quiescent supply		I <sub>DD</sub>	$V_{IN} = V_{SS}, V_{DD}$	10	_	2	_	0.004	2		60	μA
current			(Note)	15		4	—	0.008	4		120	

Note: All valid input combinations.

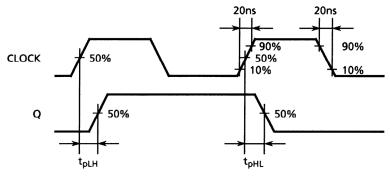
### Dynamic Electrical Characteristics (Ta = $25^{\circ}$ C, V<sub>SS</sub> = 0 V, C<sub>L</sub> = 50 pF)

Characteristics	Symbol	Test Condition	Min	Turn	Max	Unit	
Charactenstics	Symbol		V <sub>DD</sub> (V)	IVIII	Тур.	wax	Unit
Output transition time			5		70	200	
Output transition time	t <sub>TLH</sub>	—	10	—	35	100	ns
(low to high)			15		30	80	
Outrast transition time			5		70	200	
Output transition time	t <sub>THL</sub>	—	10		35	100	ns
(high to low)			15	—	30	80	
Propagation delay time	<b>t</b>		5		150	300	
(CLOCK-Q, $\overline{Q}$ )	t <sub>pLH</sub>	—	10		75	130	ns
	<sup>t</sup> pHL		15		60	90	
Propagation delay time	+		5	_	120	300	
(SET, RESET-Q, $\overline{Q}$ )	<sup>t</sup> pLH t	—	10		60	130	ns
(SET, RESET-Q, Q)	t <sub>pHL</sub>		15		45	90	
	f <sub>CL</sub>	_	5	3.5	8		
Max clock frequency			10	8.0	16		MHz
			15	12.0	20		
Max clock input rise time	to		5				
Max clock input fall time	t <sub>rCL</sub>	—	10	10 No limit 15			μS
	t <sub>fCL</sub>		15				
Min pulse width			5	_	60	180	
(SET, RESET)	t <sub>W</sub>	—	10		35	80	ns
			15	—	25	50	
			5		60	140	
Min clock pulse width	t <sub>W</sub>	—	10	_	35	60	ns
			15	—	25	40	
Min set-up time			5		30	140	
(J, K-CLOCK)	tsu	—	10		10	50	ns
			15	—	5	35	
Min hold time			5	—	—	140	
(J, K-CLOCK)	t <sub>H</sub>	—	10	—	—	50	ns
			15			35	
Min removal time			5	_	_	40	
(SET, RESET-CLOCK)	t <sub>rem</sub>	—	10	—	—	20	ns
			15		—	15	
Input capacitance	C <sub>IN</sub>	_		—	5	7.5	pF

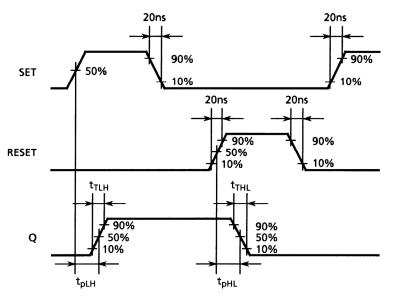
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### Waveforms for Measurement of Dynamic Characteristics

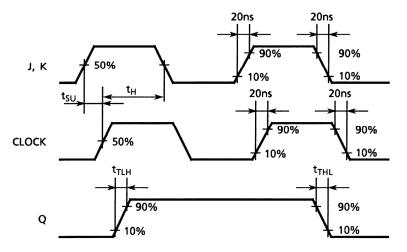
### Waveform 1



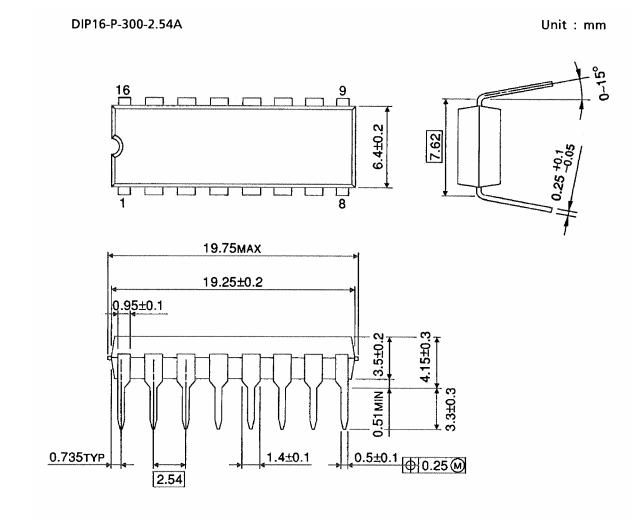
### Waveform 2



### Waveform 3



### **Package Dimensions**



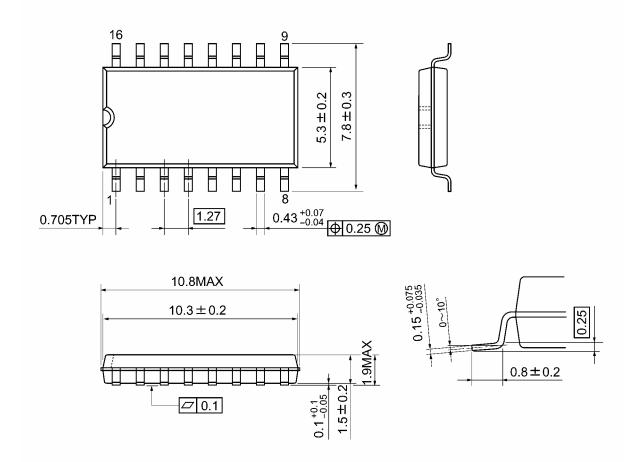
Weight: 1.00 g (typ.)



### **Package Dimensions**

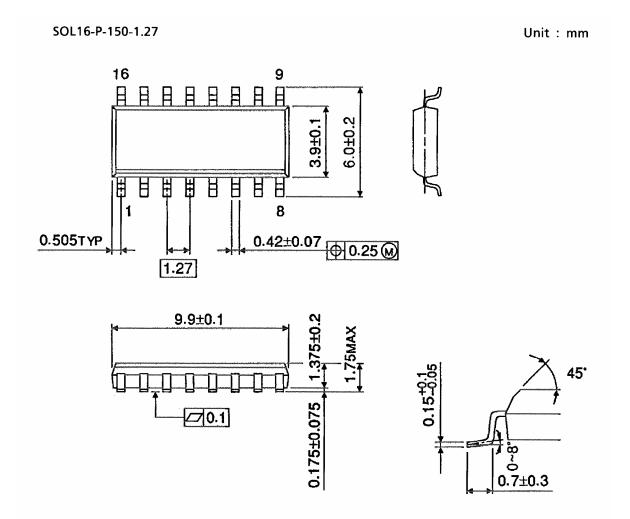
SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

### Package Dimensions (Note)



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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