

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N03FE

High Speed Switching Applications

Analog Switch Applications

- Input impedance is high. Driving current is extremely low.
- Can be directly driven by a CMOS device even at low voltage due to low gate threshold voltage.
- High-speed switching.
- Housed in a ultra-small package which is suitable for high density mounting.

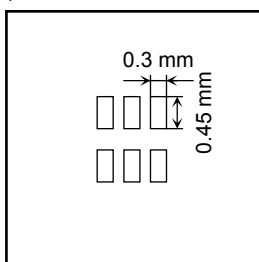
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V _{DS}	20	V
Gate-source voltage	V _{GSS}	10	V
Drain current	I _D	100	mA
Drain power dissipation	P _D (Note 1)	150	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55~150	°C

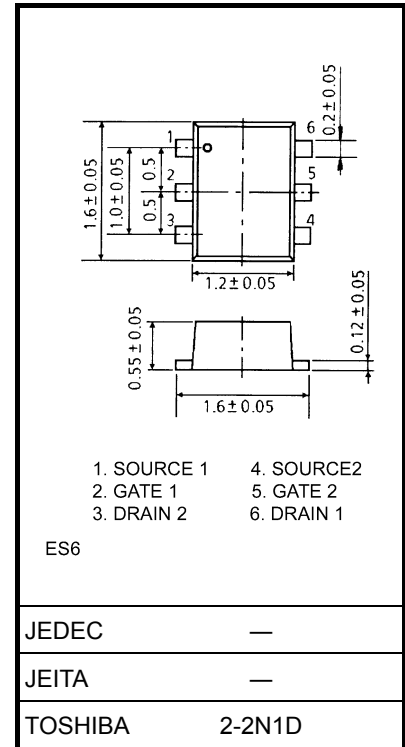
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.135 mm² × 6)

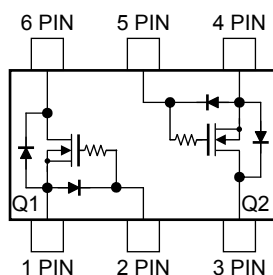


Unit: mm

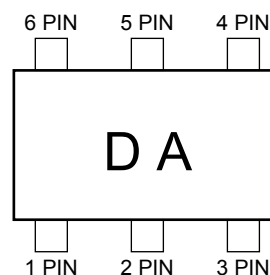


Weight: g (typ.)

Equivalent Circuit (top view)



Marking

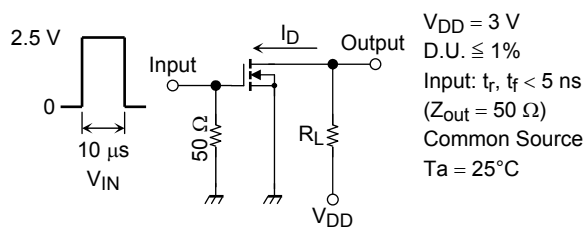


Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I_{GSS}	$V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	1	μA	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 100 \mu\text{A}, V_{GS} = 0 \text{ V}$	20	—	—	V	
Drain cut-off current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.7	—	1.3	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 10 \text{ mA}$	25	60	—	mS	
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$	—	4	12	Ω	
Input capacitance	C_{iss}	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	11.0	—	pF	
Reverse transfer capacitance	C_{rfs}	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	3.3	—	pF	
Output capacitance	C_{oss}	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	9.3	—	pF	
Switching time	Turn-on time	t_{on}	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0 \sim 2.5 \text{ V}$	—	0.16	—	μs
	Turn-off time	t_{off}	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0 \sim 2.5 \text{ V}$	—	0.19	—	

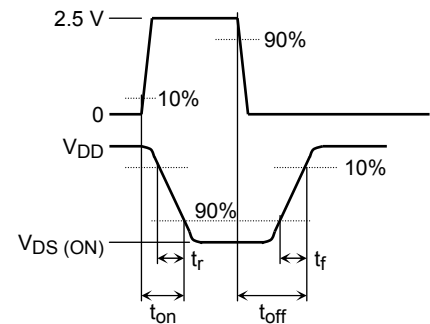
Switching Time Test Circuit

(a) Test circuit



(b) V_{IN}
 V_{GS}

(c) V_{OUT}
 V_{DS}

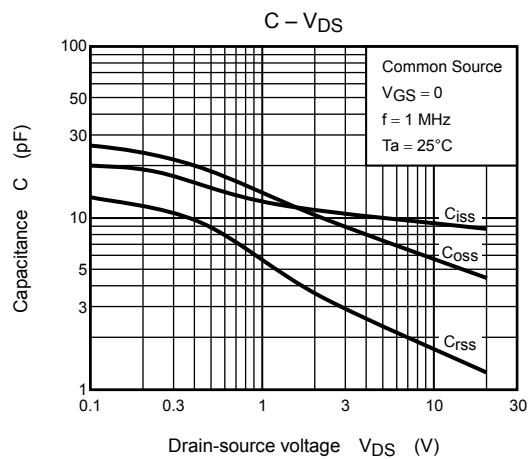
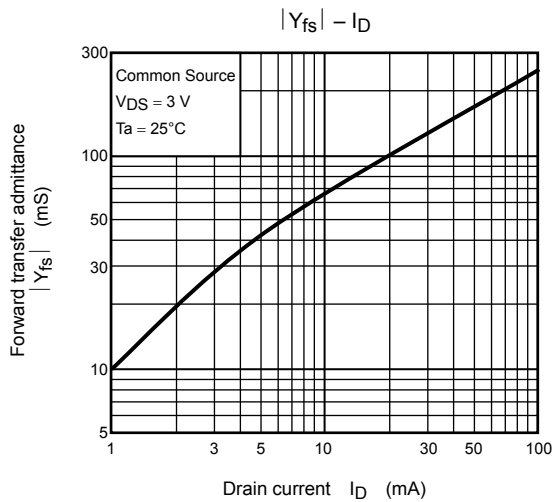
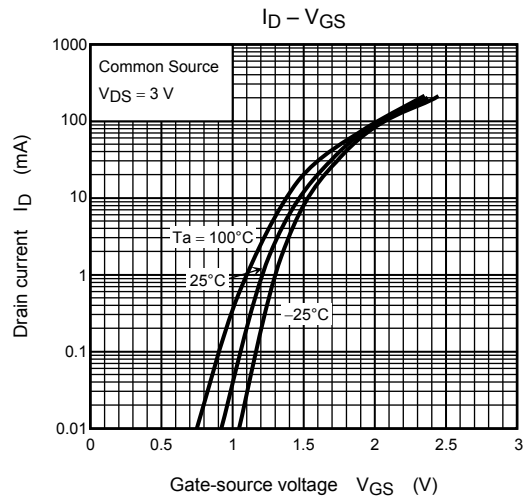
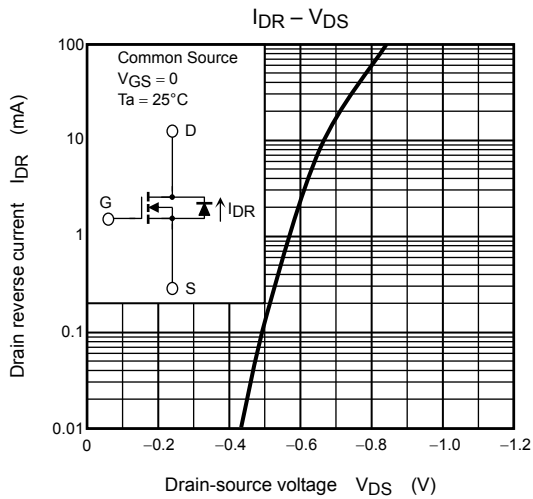
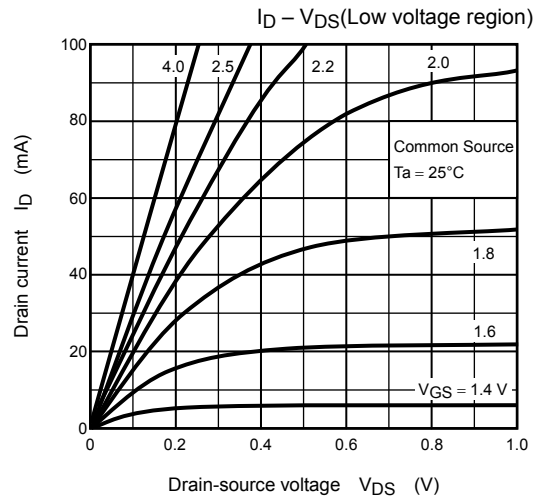
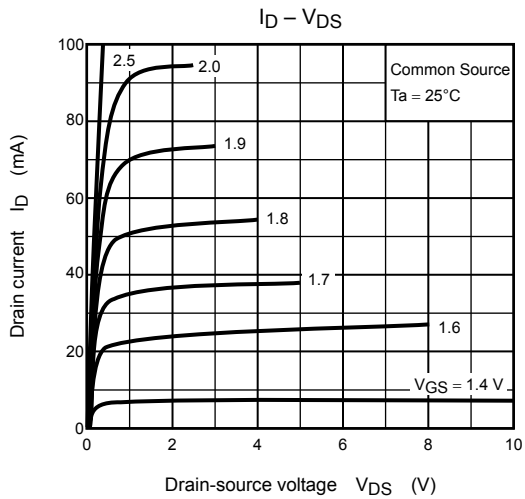


Precaution

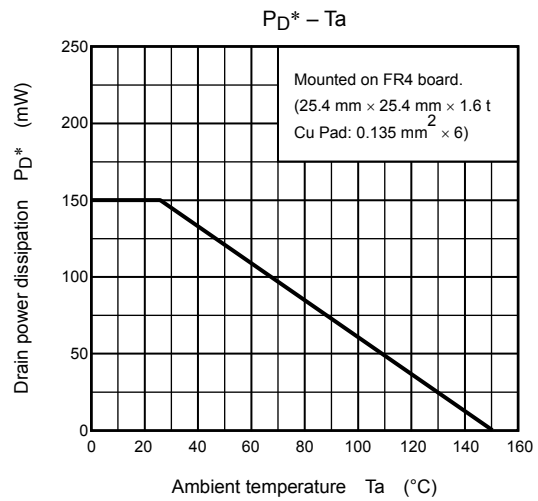
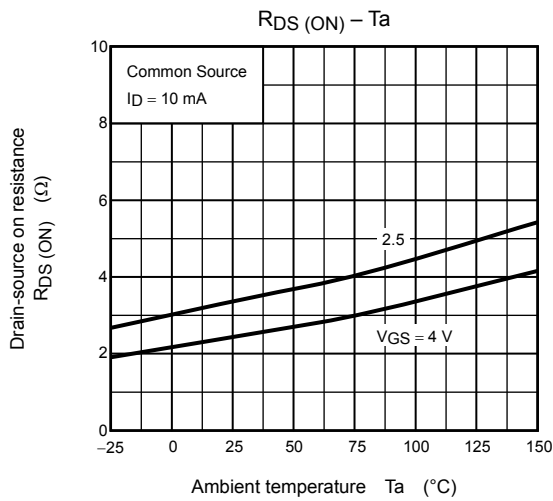
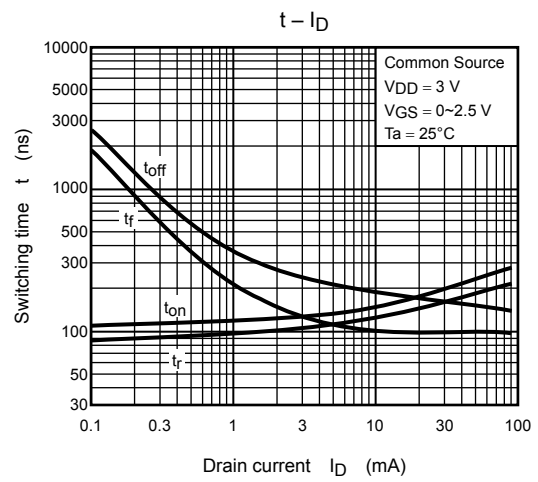
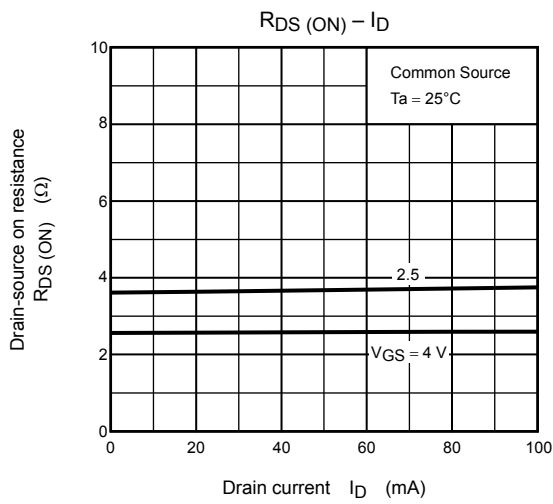
V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(on)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$)

Please take this into consideration for using the device.

(Q1, Q2 Common)



(Q1, Q2 Common)



*: Total rating

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20070701-EN GENERAL

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