# 1.8 nV/√Hz, 36 V Precision Quad Amplifier

# ADA4004-4

## FEATURES

**Very low voltage noise: 1.8 nV/√Hz**
**Low input bias current: 100 nA maximum**
**Offset voltage: 100 µV maximum**
**High gain: 120 dB**
**Wide bandwidth: 12 MHz**
**±5 V to ±15 V operation**

## APPLICATIONS

**Precision instrumentation**
**Filter blocks**
**Microphone preamplifier**
**Industrial control**
**Thermocouples and RTDs**
**Reference buffers**

## GENERAL DESCRIPTION

The ADA4004-4 is a 1.8 nV/√Hz precision quad amplifier in a 16-lead, 4 mm × 4 mm LFCSP package featuring 40 µV offset, 0.7 µV/°C drift, 12 MHz bandwidth, and low 1.7 mA per amplifier supply current.

The ADA4004-4 is designed on the high performance *i*Polar™ process, enabling improvements such as reduced noise and power consumption, increased speed and stability, and smaller footprint size. Novel design techniques enable the ADA4004-4 to achieve 1.8 nV/√Hz voltage noise density and a low 6 Hz 1/f noise corner frequency while consuming just 1.7 mA per amplifier. The small package saves board space, reduces cost, and improves layout flexibility.

Applications for these amplifiers include high precision controls, PLL filters, high performance precision filters, medical and analytical instrumentation, precision power supply controls, ATE, and data acquisition systems.

The high performance ADA4004-4 is offered in the very small 16-lead, 4 mm × 4 mm LFCSP and the 14-lead, narrow SOIC, RoHS compliant, surface-mount packages. Operation is fully specified from ±5 V to ±15 V from −40°C to +125°C.

## PIN CONFIGURATIONS

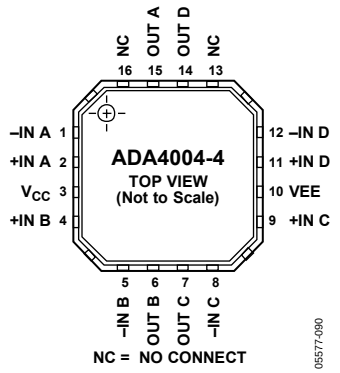


*Figure 1. 16-Lead LFCSP (CP-16-4 Suffix)*

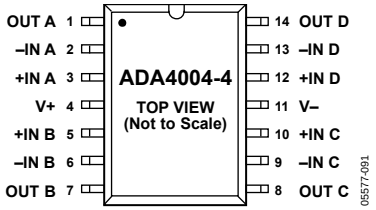


*Figure 2. 14-Lead SOIC (R-14 Suffix)*

**Rev. B**



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**1/06—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{SY}$ = ±5.0 V, $V_{CM}$ = 0 V, $T_A$ = 25°C, unless otherwise specified.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | 40 | 140 | µV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 300 | µV |
| Input Bias Current | $I_B$ | | | 40 | 85 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 165 | nA |
| Input Offset Current | $I_{OS}$ | | | 40 | 85 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 100 | nA |
| Input Voltage Range | | | −3.5 | | +3.5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = −3.0 V to +3.0 V | 105 | 111 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 95 | 110 | | dB |
| Open-Loop Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = −2.5 V to +2.5 V | 250 | 400 | | V/mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | 170 | | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C ≤ $T_A$ ≤ +125°C | | 0.7 | 1 | µV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 2 kΩ to ground | 3.7 | 3.9 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 3.4 | 3.6 | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 2 kΩ to ground | | −3.6 | −3.55 | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | | −3.6 | −3.5 | V |
| Short-Circuit Limit | $I_{SC}$ | | | 25 | | mA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | | mA |
| Output Current | $I_O$ | $V_{OUT}$ = ±3.6 V | | ±10 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = ±5.0 V to ±15.0 V | 110 | 118 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 110 | | | dB |
| Supply Current per Amplifier | $I_{SY}$ | | | | 1.8 | mA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 2.1 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ to ground | | 2.7 | | V/µs |
| Gain Bandwidth Product | GBP | | | 12 | | MHz |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 0.1 | | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 1.8 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10 Hz | | 3.5 | | pA/√Hz |
| Current Noise Density | $i_n$ | f = 200 Hz | | 1.2 | | pA/√Hz |

$V_{SY}$ = ±15 V, $V_{CM}$ = 0 V, $T_A$ = 25°C, unless otherwise specified.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | 40 | 125 | µV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 270 | µV |
| Input Bias Current | $I_B$ | | | 40 | 90 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 165 | nA |
| Input Offset Current | $I_{OS}$ | | | | 60 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 100 | nA |
| Input Voltage Range | | | −12.5 | | +12.5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = −12.5 V to +12.5 V | 110 | 113 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 100 | 104 | | dB |
| Open-Loop Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = −12.0 V to +12.0 V | 500 | 1200 | | V/mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | 250 | 500 | | V/mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C ≤ $T_A$ ≤ +125°C | | 0.7 | 1 | µV |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 2 kΩ to ground | 13.4 | 13.6 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 13.1 | 13.3 | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 2 kΩ to ground | | −13.3 | −13.2 | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | | −13.25 | −13.18 | V |
| Short-Circuit Limit | $I_{SC}$ | | | 25 | | mA |
| Output Current | $I_O$ | $V_{OUT}$ = ±13.6 V | | ±10 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = ±5.0 V to ±15.0 V | 110 | 118 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 110 | | | dB |
| Supply Current per Amplifier | $I_{SY}$ | | | | 2.0 | mA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 2.3 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ to ground | | 2.7 | | V/µs |
| Gain Bandwidth Product | GBP | | | 12 | | MHz |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{n\ p-p}$ | 0.1 Hz to 10 Hz | | 0.15 | | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 1.8 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10 Hz | | 3.5 | | pA/√Hz |
| Current Noise Density | $i_n$ | f = 200 Hz | | 1.2 | | pA/√Hz |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage | ±18 V or +36 V |
| Input Voltage | ±V supply |
| Differential Input Voltage | ±V supply |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 14-Lead SOIC (R-14) | 120 | 36 | °C/W |
| 16-Lead LFCSP (CP-16-4) | 44 | 31.5 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

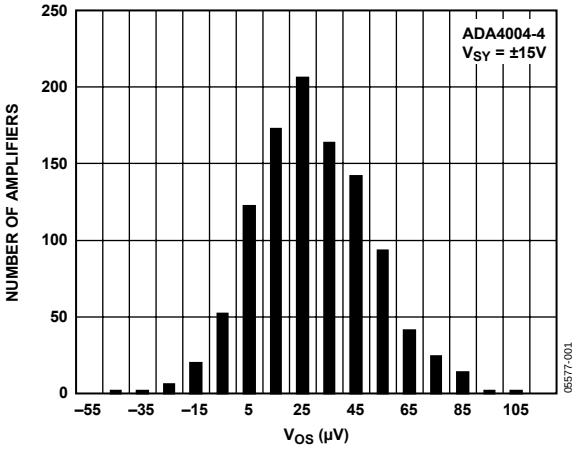



*Figure 3. Number of Amplifiers vs. Input Offset Voltage*

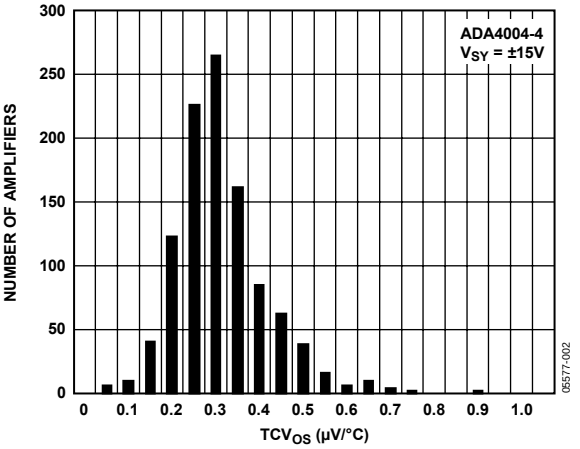



*Figure 6. Number of Amplifiers vs. $TCV_{OS}$*

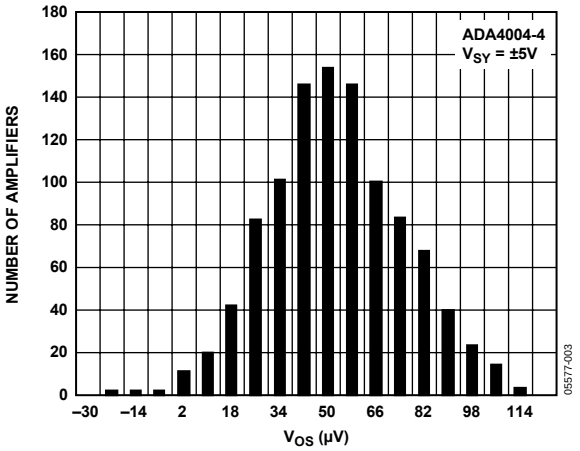



*Figure 4. Number of Amplifiers vs. Input Offset Voltage*

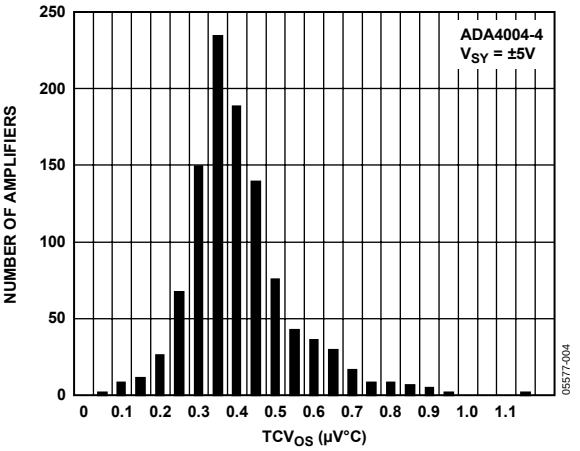



*Figure 7. Number of Amplifiers vs. $TCV_{OS}$*

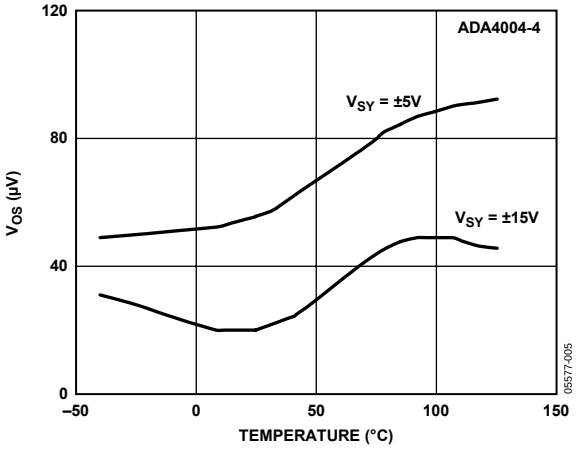



*Figure 5. Input Offset Voltage vs. Temperature*

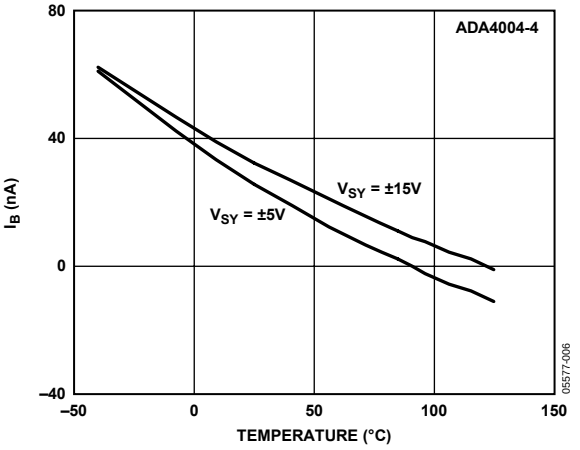



*Figure 8. Input Bias Current vs. Temperature*

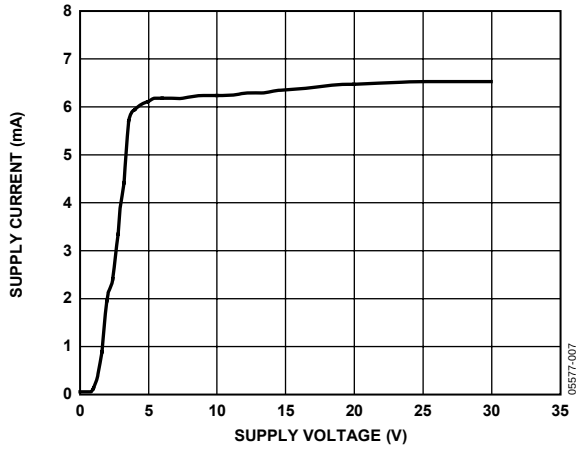



Figure 9. Supply Current vs. Total Supply Voltage

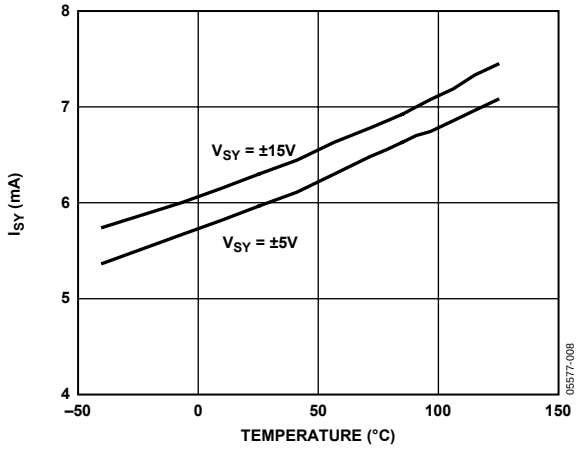



Figure 12. Supply Current vs. Temperature

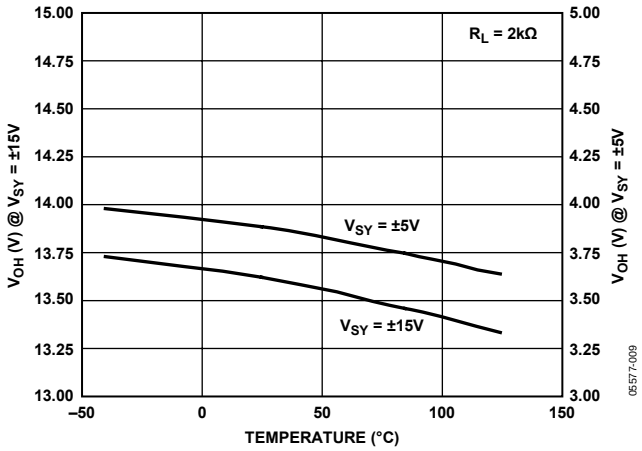



Figure 10. $V_{OH}$ vs. Temperature

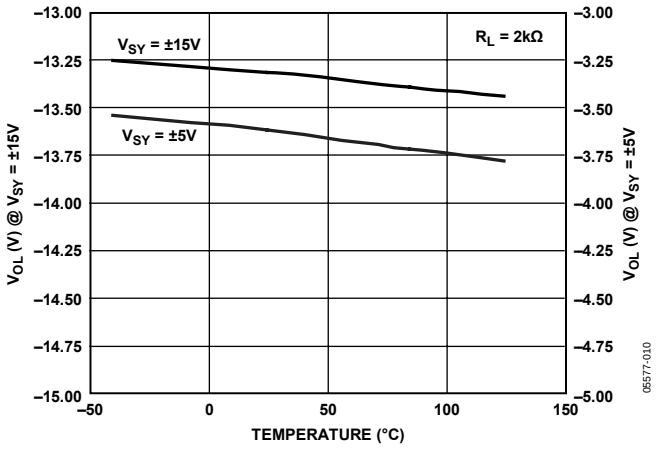



Figure 13. $V_{OL}$ vs. Temperature

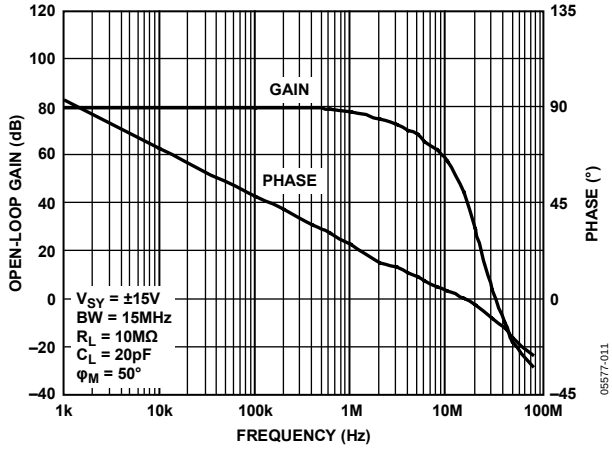



Figure 11. Open-Loop Gain and Phase vs. Frequency

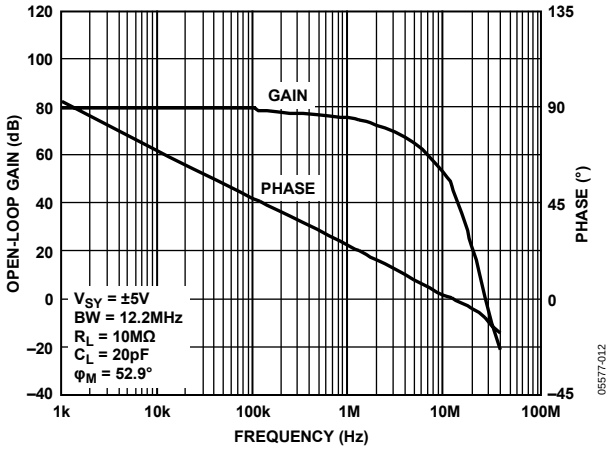



Figure 14. Open-Loop Gain and Phase vs. Frequency

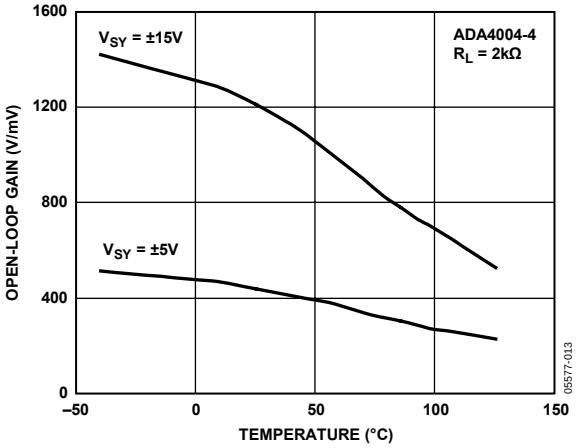



Figure 15. Open-Loop Gain vs. Temperature

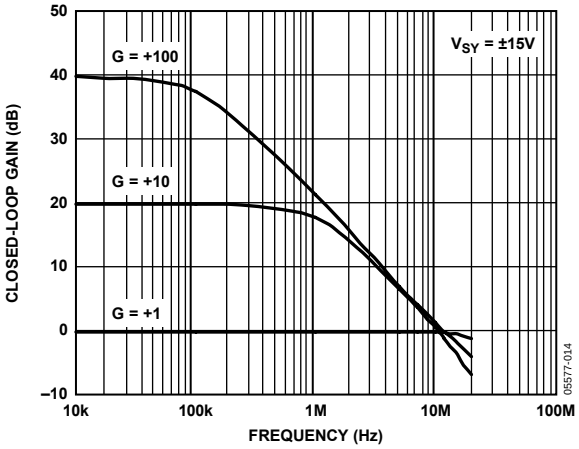



Figure 18. Closed-Loop Gain vs. Frequency

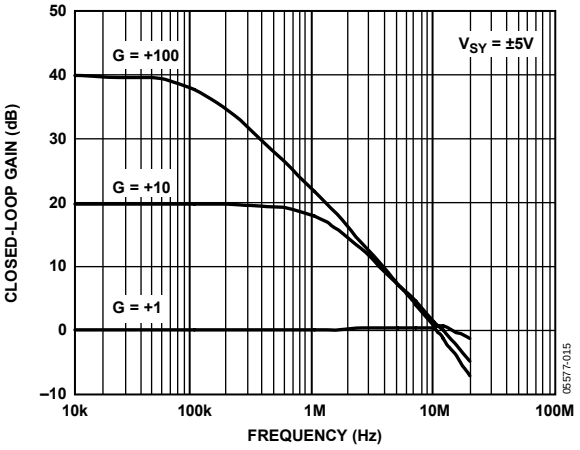



Figure 16. Closed-Loop Gain vs. Frequency

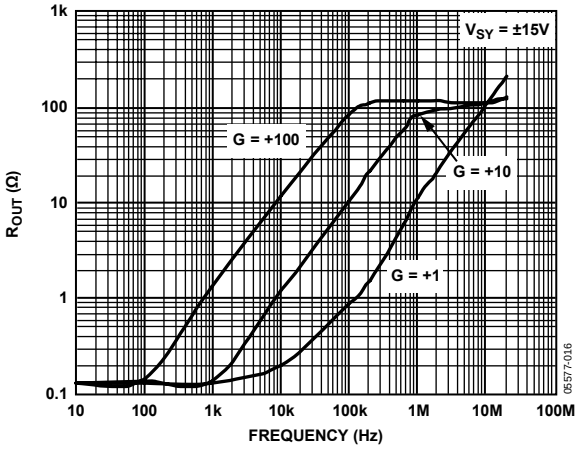



Figure 19. Output Impedance vs. Frequency

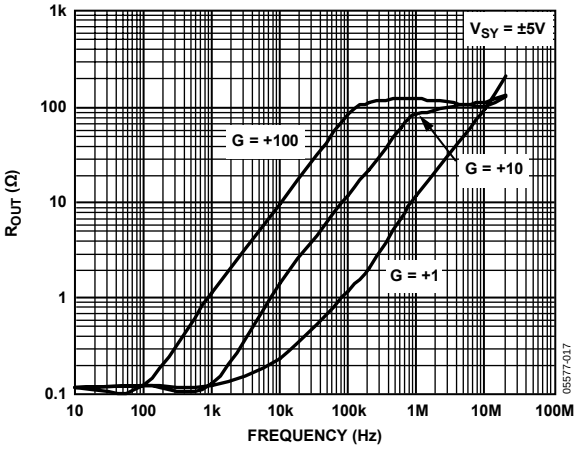



Figure 17. Output Impedance vs. Frequency

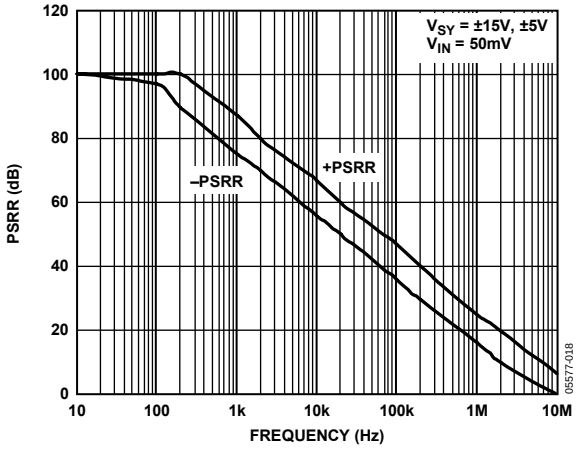



Figure 20. PSRR vs. Frequency

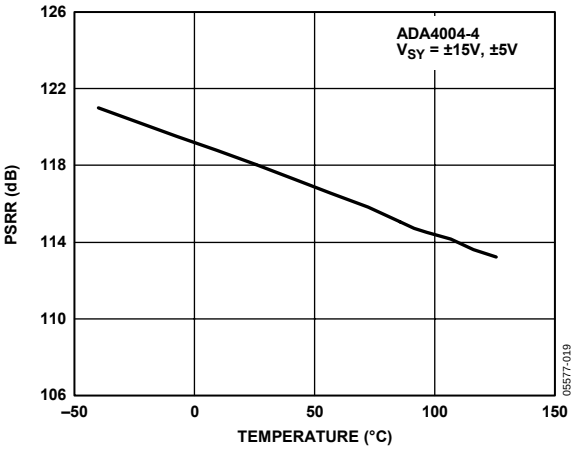



Figure 21. PSRR. vs. Temperature

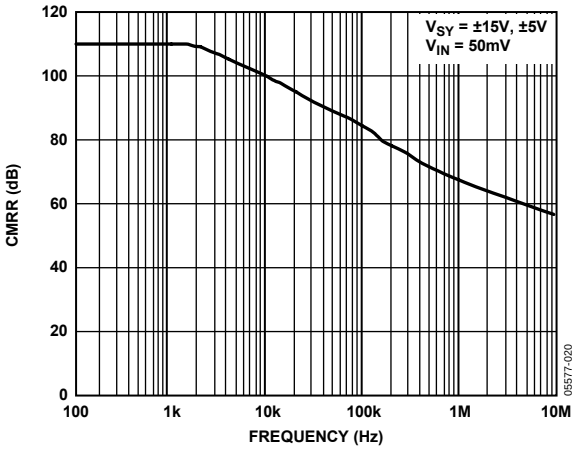



Figure 24. CMRR vs. Frequency

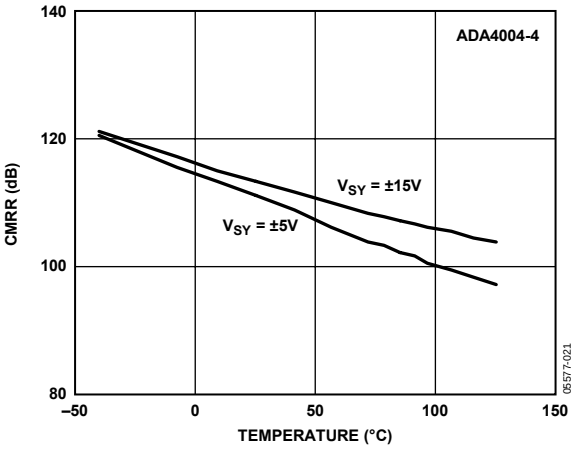



Figure 22. CMRR vs. Temperature

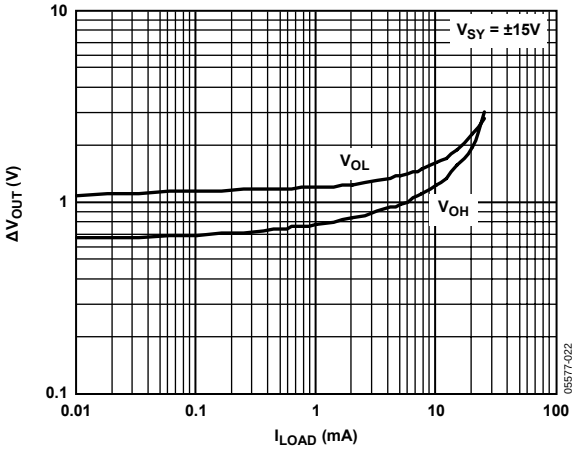



Figure 25. Output Voltage vs. Current Load

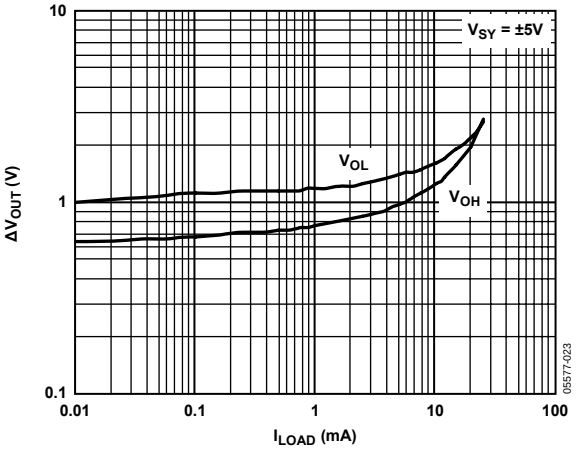



Figure 23. Output Voltage vs. Current Load

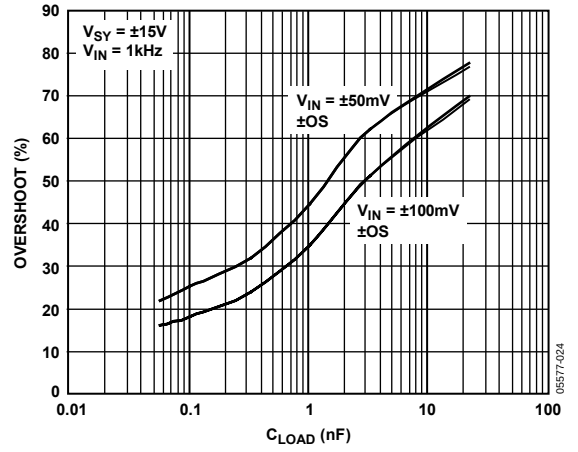



Figure 26. Small-Signal Overshoot vs. Capacitive Load

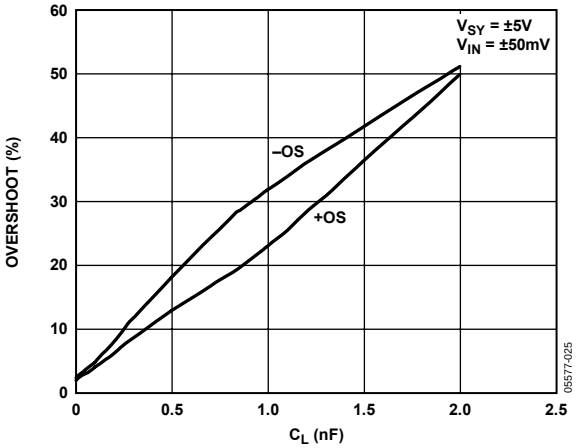



Figure 27. Small-Signal Overshoot vs. Capacitive Load

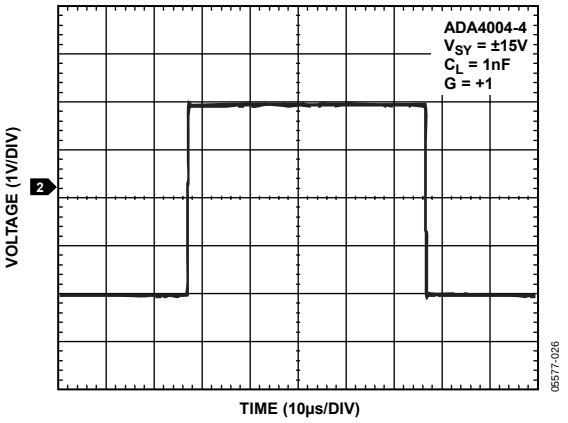



Figure 30. Large-Signal Transient Response

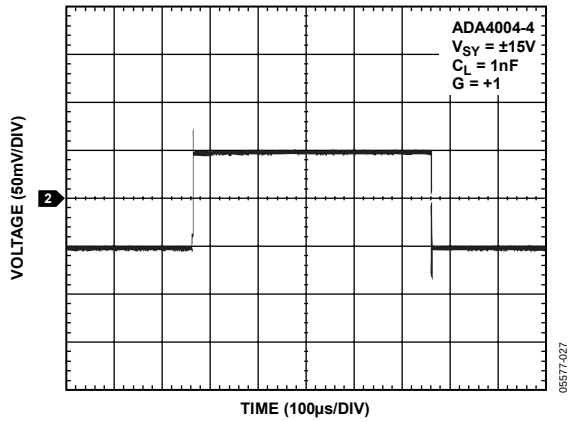



Figure 28. Small-Signal Transient Response

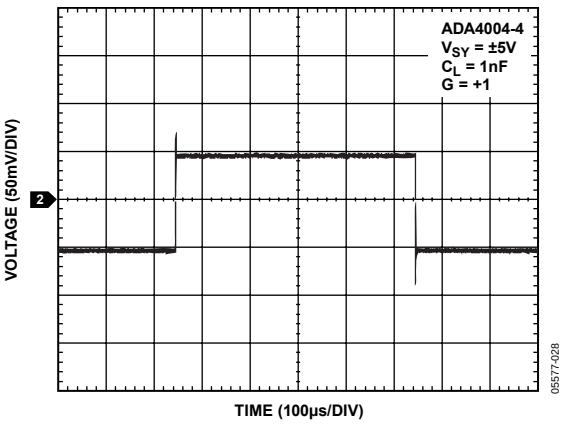



Figure 31. Small-Signal Transient Response

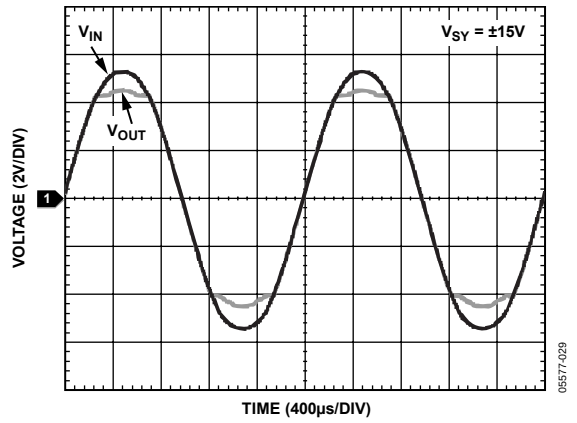



Figure 29. No Phase Reversal

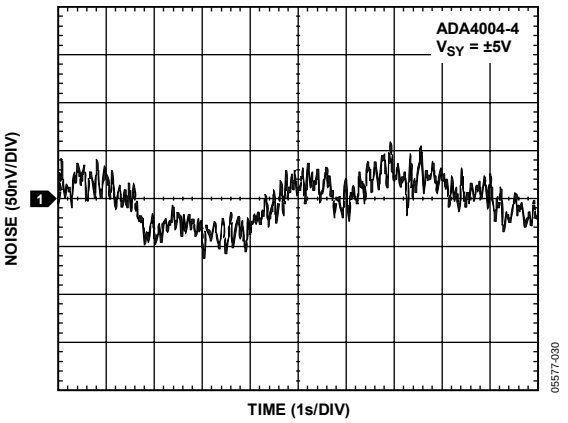



Figure 32. Voltage Noise (0.1 Hz to 10 Hz)

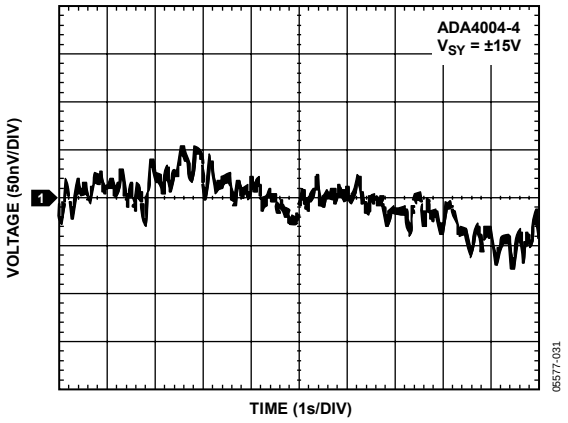



Figure 33. Voltage Noise (0.1 Hz to 10 Hz)

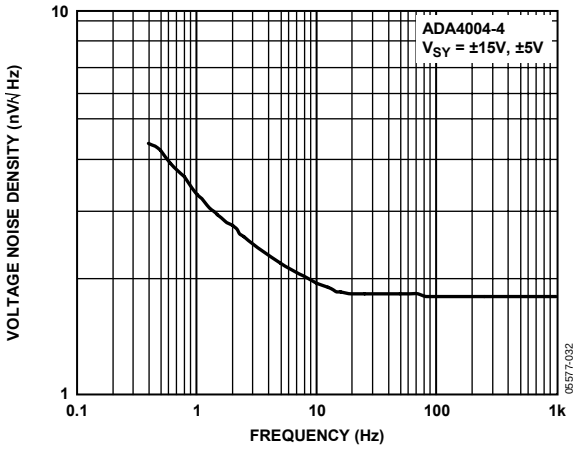



Figure 34. Voltage Noise Density vs. Frequency

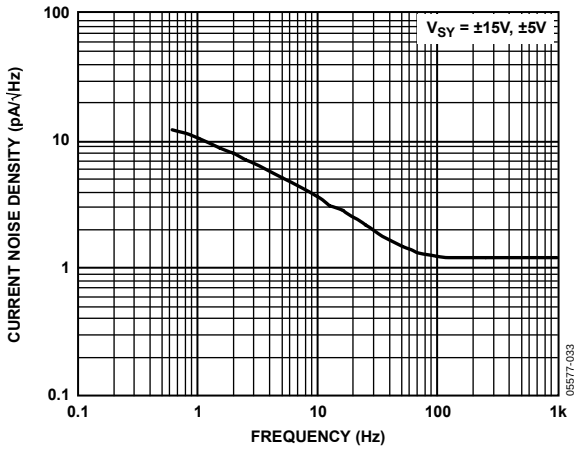



Figure 35. Current Noise Density vs. Frequency

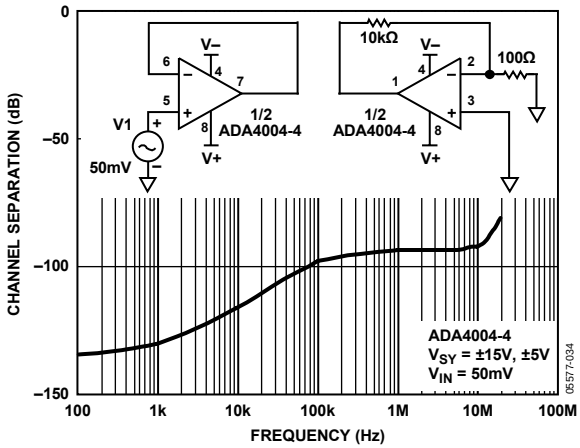
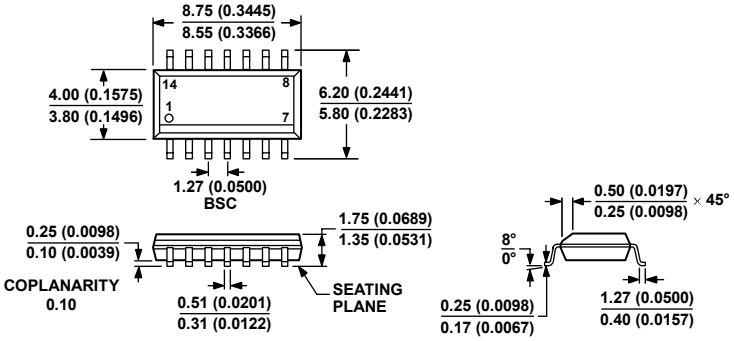



Figure 36. Channel Separation vs. Frequency

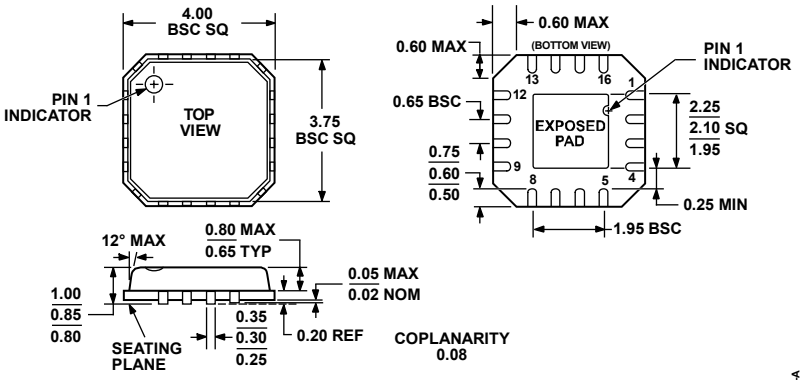
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

*Figure 37. 14-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-14)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

021207-A

*Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*4 mm × 4 mm Body, Very Thin Quad*
*(CP-16-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADA4004-4ACPZ-R2[1] | −40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-16-4 |
| ADA4004-4ACPZ-R7[1] | −40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-16-4 |
| ADA4004-4ACPZ-RL[1] | −40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-16-4 |
| ADA4004-4ARZ[1] | −40°C to +125°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 |
| ADA4004-4ARZ-R7[1] | −40°C to +125°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 |
| ADA4004-4ARZ-RL[1] | −40°C to +125°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 |

[1] Z = RoHS Compliant Part.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