

AOT460

N-Channel Enhancement Mode Field Effect Transistor

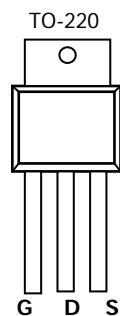
General Description

The AOT460 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in UPS, high current switching applications. *Standard Product AOT460 is Pb-free (meets ROHS & Sony 259 specifications).*

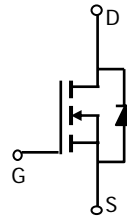
Features

$V_{DS} (V) = 60V$
 $I_D = 85 A \quad (V_{GS} = 10V)$
 $R_{DS(ON)} < 7.5m\Omega \quad (V_{GS} = 10V)$

UIS TESTED!



Top View
 Drain
 Connected to
 Tab



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ C$	A
		$T_C=100^\circ C$	
Pulsed Drain Current ^C	I_{DM}	250	
Avalanche Current ^C	I_{AR}	80	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	320	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	W
		$T_C=100^\circ C$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	45	60	$^\circ C/W$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	0.45	0.56	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250uA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V T _J =55°C			10 50	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	2.95	4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	250			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =30A T _J =125°C		6.3 10.5	7.5 13	mΩ
g _{FS}	Transconductance	V _{DS} =5V, I _D =30A		90		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				85	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		3800	4560	pF
C _{oss}	Output Capacitance			430		pF
C _{rss}	Reverse Transfer Capacitance			190		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.5	2.3	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =30A		68	88	nC
Q _{g(4.5V)}	Total Gate Charge			33		nC
Q _{gs}	Gate Source Charge			15		nC
Q _{gd}	Gate Drain Charge			19		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =1Ω, R _{GEN} =3Ω		18		ns
t _r	Turn-On Rise Time			35		ns
t _{D(off)}	Turn-Off DelayTime			44		ns
t _f	Turn-Off Fall Time			23		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =30A, dI/dt=100A/μs		53	64	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =30A, dI/dt=100A/μs		98		nC

A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

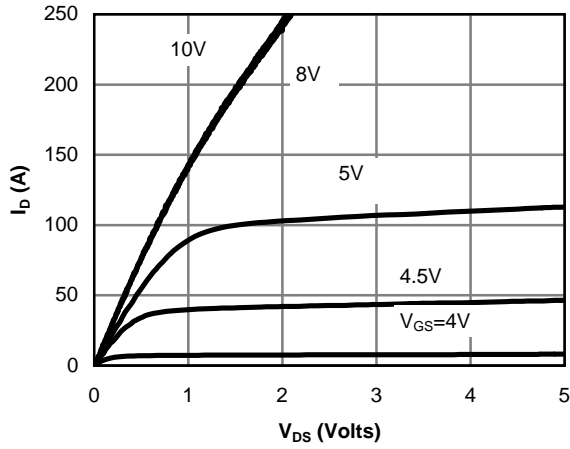


Figure 1: On-Region Characteristics

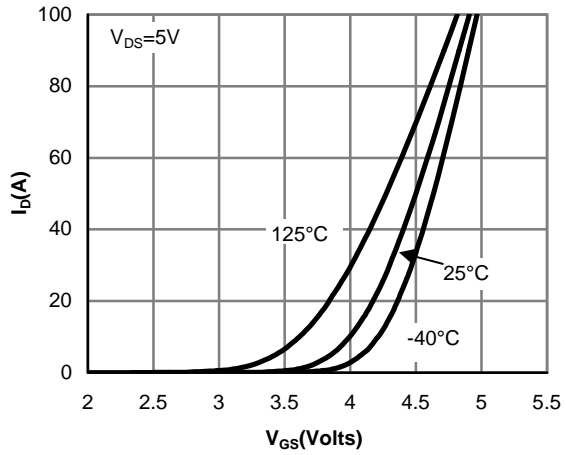


Figure 2: Transfer Characteristics

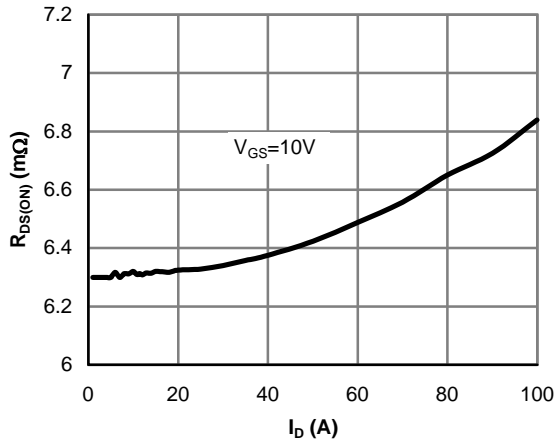


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

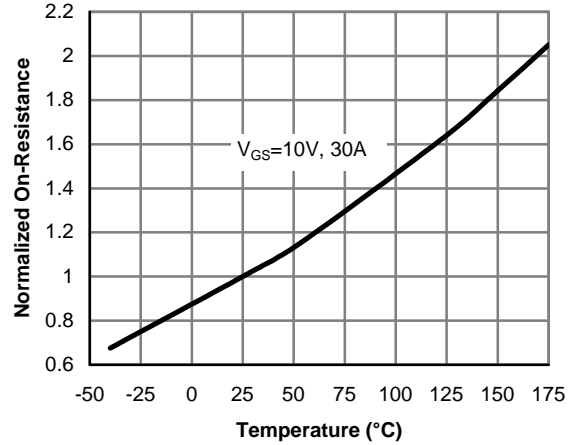


Figure 4: On-Resistance vs. Junction Temperature

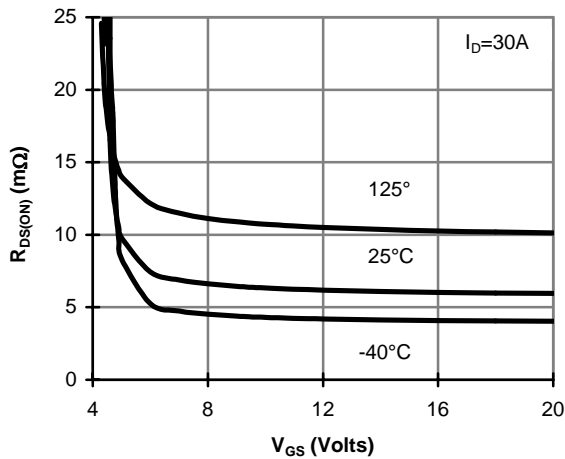


Figure 5: On-Resistance vs. Gate-Source Voltage

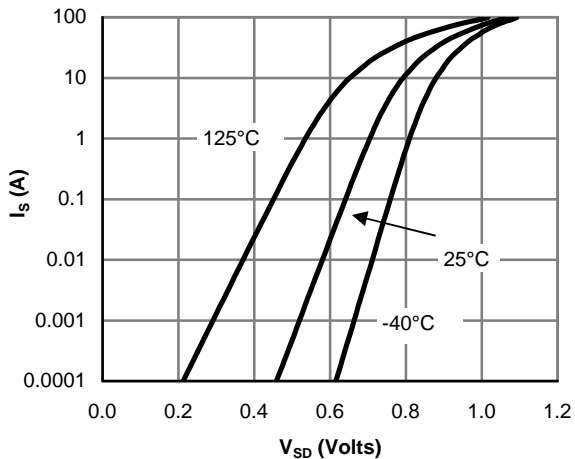


Figure 6: Body-Diode Characteristics

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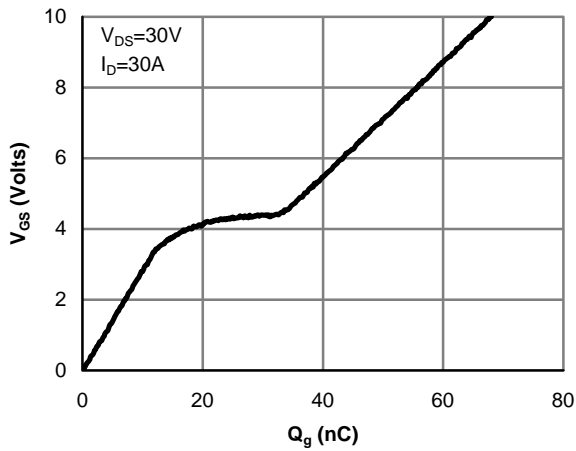


Figure 7: Gate-Charge Characteristics

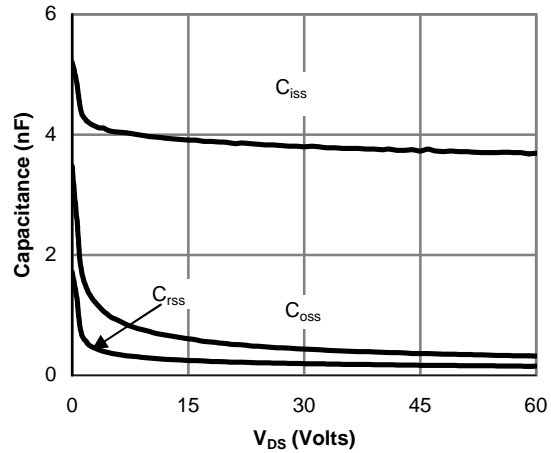


Figure 8: Capacitance Characteristics

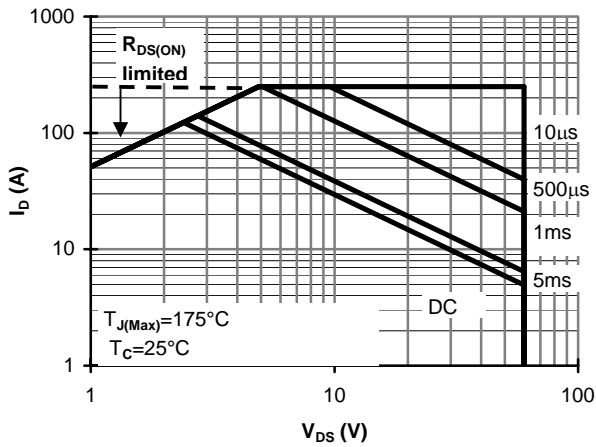


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

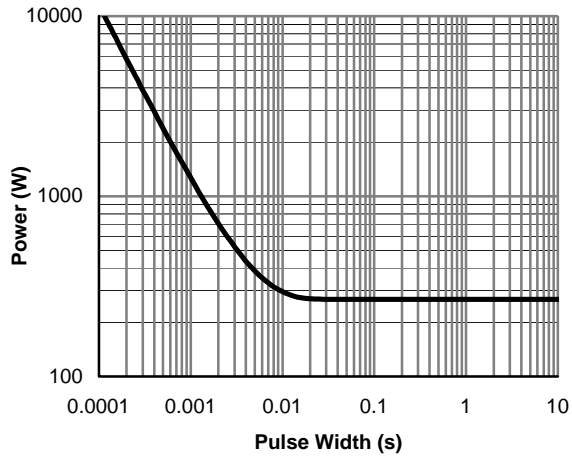


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

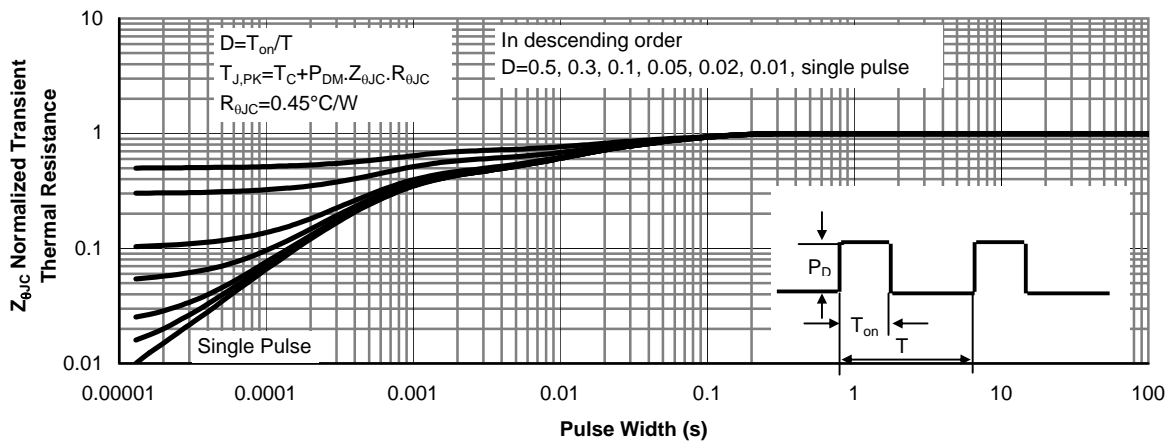


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

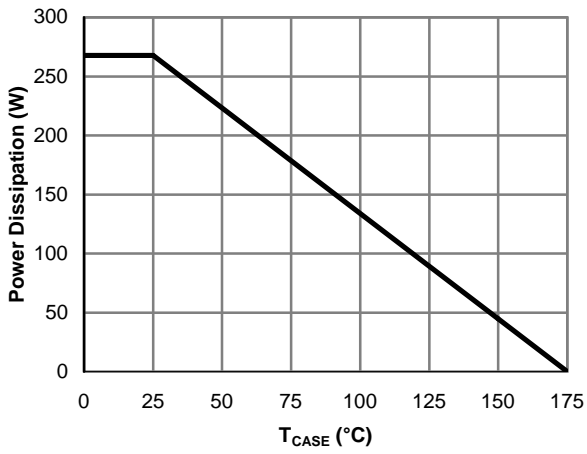


Figure 13: Power De-rating (Note B)

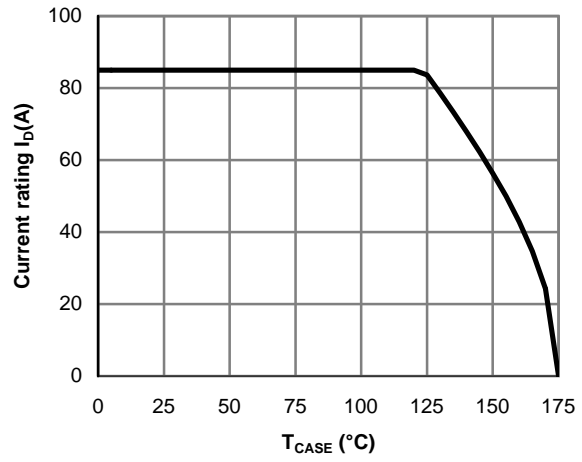


Figure 12: Current De-rating (Note B)

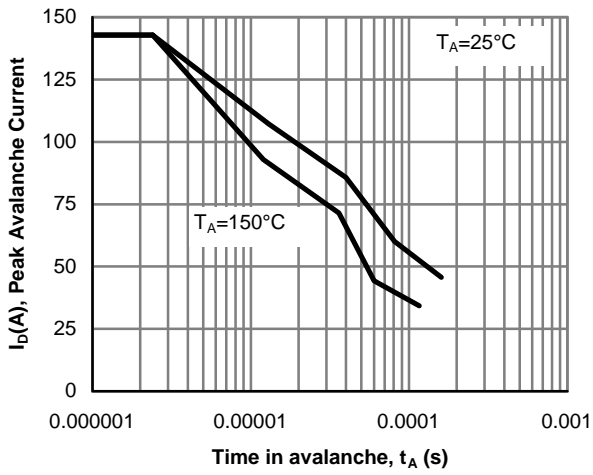


Figure 10: Single Pulse Avalanche capability