PI2EQX3431

3.2Gbps, 1-port, SATA2/SAS Re-Driver

Features

- Two 3.2Gbps differential signal pairs
- Adjustable Receiver Equalization
- 100-Ohm Differential CML I/O's
- Independent Output Level Control
- Input signal level detect and squelch for each channel
- OOB Support
- Low Power (100mW per Channel)
- Stand-by Mode – Power Down State
- V_{CC} Operating Range: 1.8V ±0.1V
- Packaging: — 20-TQFN (3.5x 4.5mm)

Description

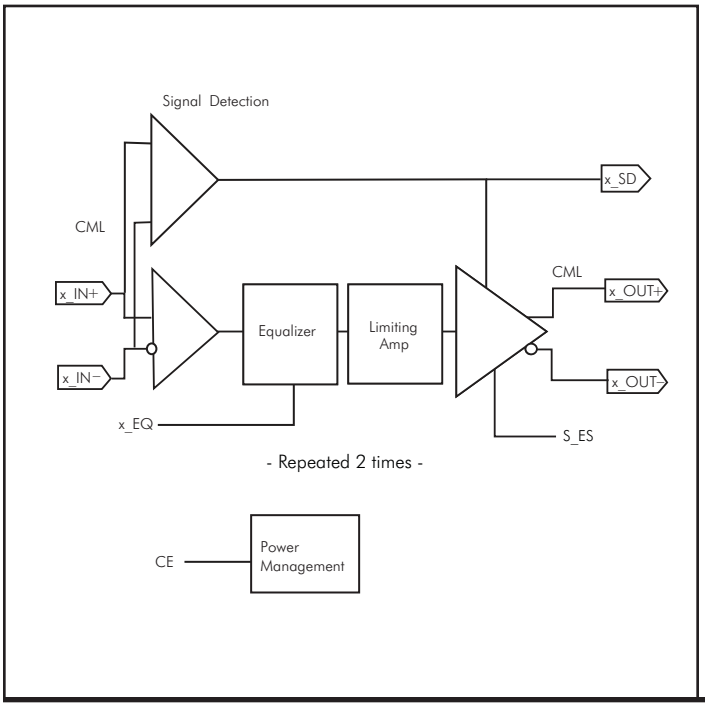
Pericom Semiconductor's PI2EQX3431 is a low power, signal Re-Driver. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX3431 supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the re-driver.

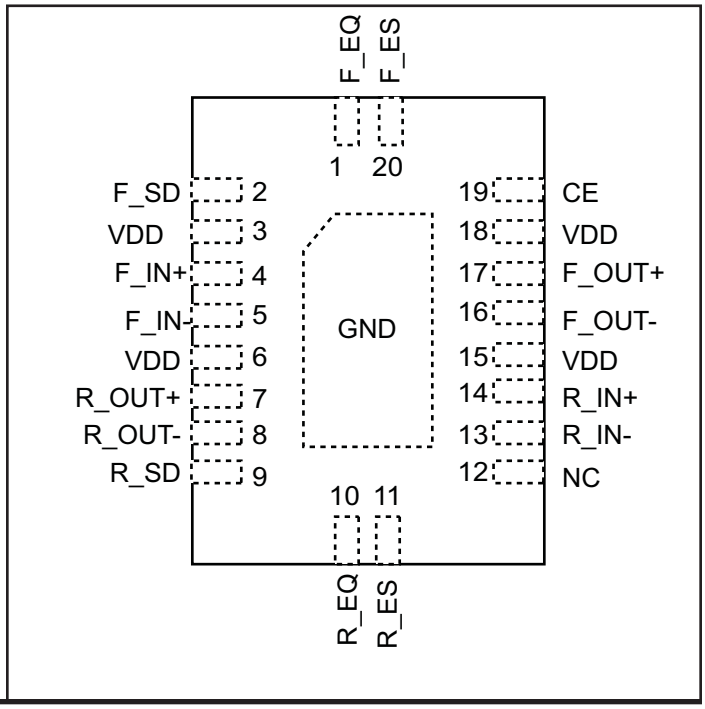
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independantly. When the channels are enabled (CE=1) and operating, that channels input signal level (on xIN+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to signal conditioning, when CE = 0, the device enters a low power standby mode.

Block Diagram



Pin Description (Top Side View)



Pin Description

Pin #	Pin Name	Type	Description
19	CE	Input	Chip Enable "high" provides normal operation. "Low" for power down mode. With internal 50K-Ohm pull-up resistor.
1	F_EQ	Input	Selection pin for equalizer of Fin. "Low" means 2.5dB, "high" means 6.5dB. With internal 50K-Ohm pull-up resistor.
20	F_ES	Input	F-Channel external SATA. When logic 1, operates to the SATA *i/m* standard. When low, operates to SATAx/SAS. With internal 50K-ohm pull-up resistor.
2	F_SD	Output	Channel Fin Signal detector output. Provides "high" when a signal is detected.
17 16	F_OUT+ F_OUT-	Output	CML output channel F with internal 50-Ohm pull up.
4 5	F_IN+ F_IN-	Input	CML input channel F with internal 50-Ohm pull down.
Center Pad	GND	GND	Supply ground.
12	NC	-	Do not connect
10	R_EQ	Input	Selection pin for equalizer of R_IN. "Low" means 2.5dB, "high" means 6.5dB. With internal 50K-Ohm pull-up resistor.
14 13	R_IN+ R_IN-	Input	CML input channel R with internal 50-Ohm pull down.
9	R_SD	Output	Signal detector for Channel R_IN. Provides "high" when signal is detected.
7 8	R_OUT+ R_OUT-	Output	Positive CML output channel R with internal 50-Ohm pull up.
11	R_ES	Input	R-channel External SATA "High" operates to the SATA *i/m* standard. "Low" means SATAx/SAS standard. With internal 50K-Ohm pull-up resistor.
3,6,15,18	VDD	Power	1.8V supply Voltage.

Equalizer Selection

x_EQ	Compliance Channel
0	[0:2.5dB] @ 1.6 GHz
1	[4.5:6.5dB] @ 1.6 GHz

Output CML Buffer

CE	x_ES	Common mode voltage	Output Operation
0	X	VDD	VDD
1	0	VDD-0.6V	1200mV Swing
1	1	VDD-0.3V	600mV Swing

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{CC} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.8 ±0.1V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$P_{STANDBY}$	Supply Power	CE = LVCMOS Low			0.1	W
P_{ACTIVE}	Supply Power	CE = LVCMOS High			0.3	
t_{PD}	Latency	From input to output		1.0		ns
CML Receiver Input						
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
Z_{RX-DC}	DC Input Impedance		40	50	60	Ohm
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
J_{RM}	Random Jitter(1,2)			1.5		psrms
Signal Detector Performance						
V_{TH}	Threshold	CE = 1	75(3)		200 (3)	mVppd
T_{EN}	Enable/disable time				16	ns

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.
3. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)							
V_{DIFFP}	Output Voltage Swing	Differential Swing | V_{TX-D+} - V_{TX-D-} |	x_ES = 1(1)	200		375	mVp-p
			x_ES = 0(1)	550		650	mVp-p
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P}$ = 2 * | V_{TX-D+} - V_{TX-D-} |	x_ES = 1(1)	400		750	mV
			x_ES = 0(1)	1100		1300	mV
V_{TX-C}	Common-Mode Voltage	| V_{TX-D+} + V_{TX-D-}|/2	x_ES = 0(1)		V_{DD} - 0.6		V
			x_ES = 1(1)		V_{DD} - 0.3		
t_F, t_R	Transition Time					150	ps
$\frac{t_F - t_R}{t_{F(t_R)}}$	Transition Mismatch Time	20% to 80%				20	%
Z_{OUT}	Output resistance	Single ended			50		Ohm
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance			80	100	120	Ohm
C_{TX}	AC Coupling Capacitor			0.3	4.7	12	nF
LVCMOS Control Pins							
V_{IH}	Input High Voltage			0.65 × V_{DD}			V
V_{IL}	Input Low Voltage					0.35 × V_{DD}	
I_{IH}	Input High Current					250	µA
I_{IL}	Input Low Current					500	
V_{OH}	DC Output Logic High	I_{OH} = 4mA		V_{DD} - 0.4			V
V_{OL}	DC Output Logic Low	I_{OL} = -4mA				0.4	

Note:
1. When S_ES=0 select SATAx standard, When S_ES=1 select SATAi/m standard

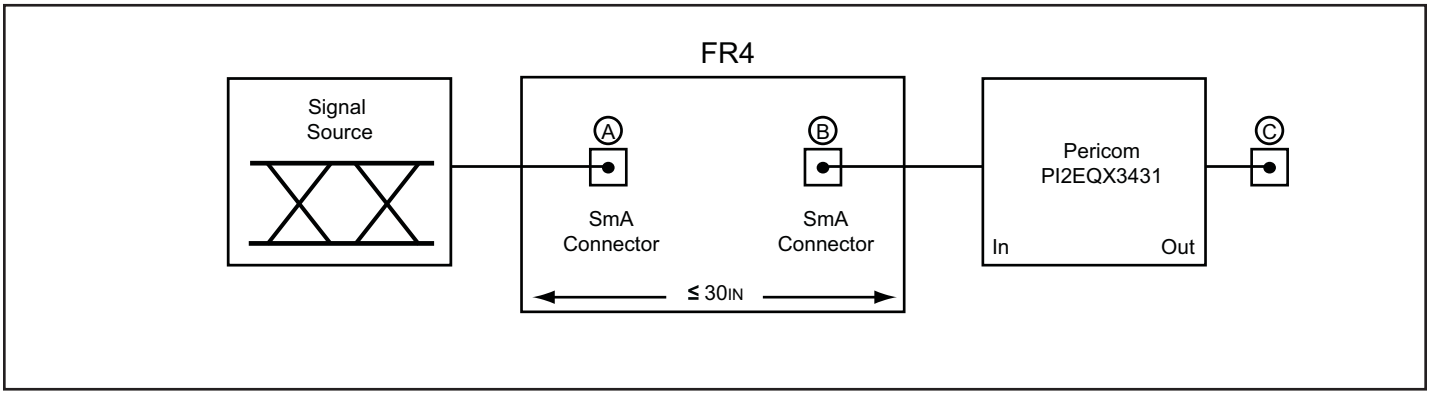
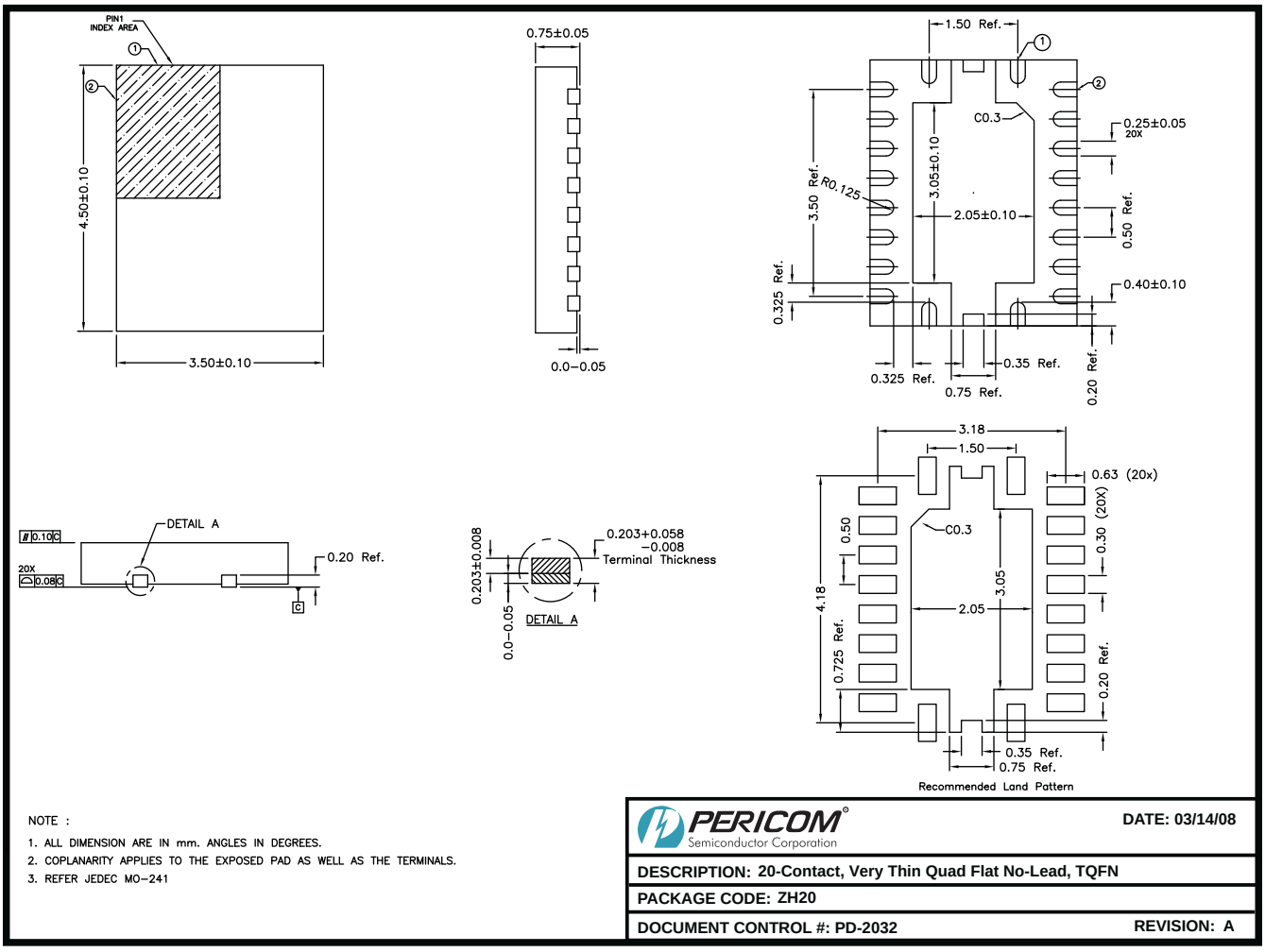


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

Packaging Mechanical: 20-contact TQFN (ZH)



Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3431ZHE	ZH	Pb-Free and Green 20-contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel