Silicon N Channel MOS FET Series Power Switching

HITACHI

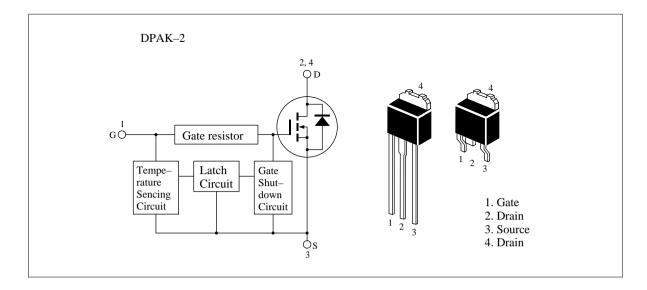
Target specification ADE-208-706 (Z) 1st. Edition Dec. 1998

This FET has the over temperature shut—down capability sensing to the junction temperature. This FET has the built—in over temperature shut—down circuit in the gate area. And this circuit operation to shut—down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

Features

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut—down operation (Need 0 voltage recovery)

Outline





Absolute Maximum Ratings $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{ exttt{DSS}}$	60	V
Gate to source voltage	V _{GSS}	(16)	V
Gate to source voltage	V_{GSS}	(-2.5)	V
Drain current	I _D	5	A
Drain peak current	Note1 D(pulse)	10	A
Body-drain diode reverse drain current	I _{DR}	5	A
Channel dissipation	Pch Note2	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW \leq 10 μ s, duty cycle \leq 1 %

2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	_	_	V	_
	V _{IL}	_	_	1.2	V	
Input current	I _{IH1}	_	_	100	μΑ	$Vi = 8V$, $V_{DS} = 0$
(Gate non shut down)	I _{IH2}	_	_	50	μΑ	$Vi = 3.5V, V_{DS} = 0$
	I _{IL}	_	_	1	μΑ	$Vi = 1.2V, V_{DS} = 0$
Input current	I _{IH(sd)1}	_	8.0	_	mA	$Vi = 8V$, $V_{DS} = 0$
(Gate non shut down)	I _{IH(sd)2}	_	0.35	_	mA	$Vi = 3.5V, V_{DS} = 0$
Shut down temperature	T _{sd}	_	175	_	°C	Channel temperature
Gate operation voltage	V _{op}	3.5	_	12	V	

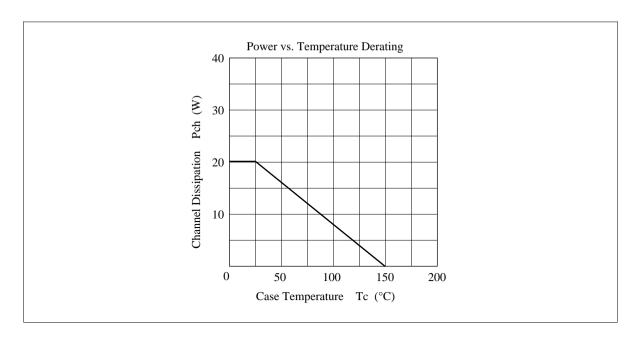
Electrical Characteristics ($Ta = 25^{\circ}C$)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain current	I _{D1}	(5)	_	_	Α	$V_{GS} = 3.5V, V_{DS} = 2V$
Drain current	I _{D2}	_	_	10	mA	$V_{GS} = 1.2V, V_{DS} = 2V$
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	_	_	V	$I_{D} = 10 \text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	(16)	_	_	V	$I_{G} = (300 \mu A), V_{DS} = 0$
Gate to source breakdown voltage	V _{(BR)GSS}	(-2.5)	_	_	V	$I_{G} = (-100 \mu A), V_{DS} = 0$
Gate to source leak current	I _{GSS1}	_	_	100	μΑ	$V_{GS} = 8V, V_{DS} = 0$
	I _{GSS2}	_	_	50	μΑ	$V_{GS} = 3.5V, V_{DS} = 0$
	I _{GSS3}	_	_	1	μΑ	$V_{GS} = 1.2V, V_{DS} = 0$
	I _{GSS4}	_	_	-100	μΑ	$V_{GS} = -2.4V, V_{DS} = 0$
Input current (shut down)	I _{GS(op)1}	_	8.0	_	mA	$V_{GS} = 8V$, $V_{DS} = 0$
	I _{GS(op)2}		0.35	_	mA	$V_{GS} = 3.5V, V_{DS} = 0$
Zero gate voltege drain current	I _{DSS}	_	_	10	μΑ	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	_	2.25	V	$I_D = 1$ mA, $V_{DS} = 10$ V
Static drain to source on state resistance	R _{DS(on)}	_	100	160	mΩ	$I_D = 2.5A, V_{GS} = 4V^{Note3}$
Static drain to source on state resistance	R _{DS(on)}	_	70	100	mΩ	$I_D = 2.5A, V_{GS} = 10V^{Note3}$
Forward transfer admittance	y _{fs}	(5)	(18)	_	S	$I_D = 2.5A, V_{DS} = 10V^{Note3}$
Output capacitance	Coss	_	(260)	_	pF	$V_{DS} = 10V , V_{GS} = 0$ f = 1 MHz
Turn-on delay time	t _{d(on)}	_	()	_	μs	$I_D = 2.5A, V_{GS} = 5V$
Rise time	t _r	_	()	_	μs	$R_L = 12\Omega$
Turn-off delay time	t _{d(off)}	_	()	_	μs	
Fall time	t _f	_	()	_	μs	
Body-drain diode forward voltage	V_{DF}	_	(1.0)	_	V	$I_F = 2.5A, V_{GS} = 0$
Body-drain diode reverse recovery time	t _{rr}	_	()	_	ns	$I_F = 5A, V_{GS} = 0$ diF/ dt =50A/ μ s
Over load shut down	t _{os1}	_	()	_	ms	$V_{GS} = 5V$, $V_{DD} = 12V$
operation time Note4	t _{os2}	_	()	_	ms	$V_{GS} = 5V$, $V_{DD} = 24V$

Note: 3. Pulse test

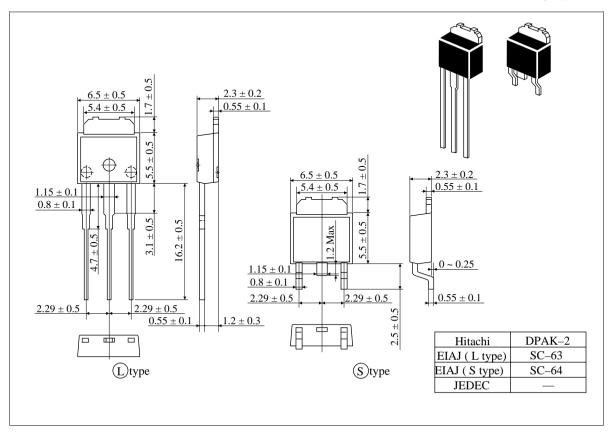
4. Include the time shift based on increasing of chennel temperature when operete under over load condition.

Main Characteristics



Package Dimensions

Unit: mm



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