

2SK2788

Silicon N Channel MOS FET
High Speed Power Switching

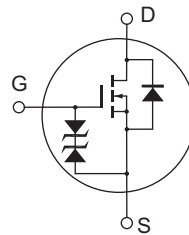
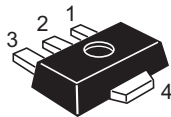
REJ03G1033-0200
(Previous: ADE-208-538)
Rev.2.00
Sep.07,2005

Features

- Low on-resistance
 $R_{DS(on)} = 0.12 \Omega$ typ ($V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$)
- Low drive current
- High speed switching
- 4 V gate drive devices.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK[®])



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "VY"

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	2	A
Drain peak current	I _{D(pulse)} *1	4	A
Body to drain diode reverse drain current	I _{DR}	2	A
Channel dissipation	P _{ch} *2	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1 %

2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

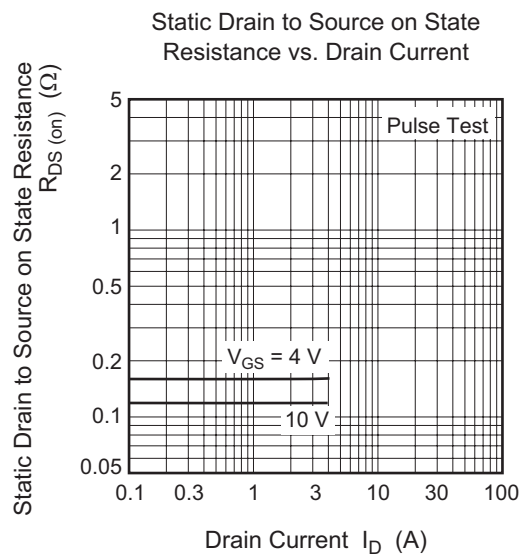
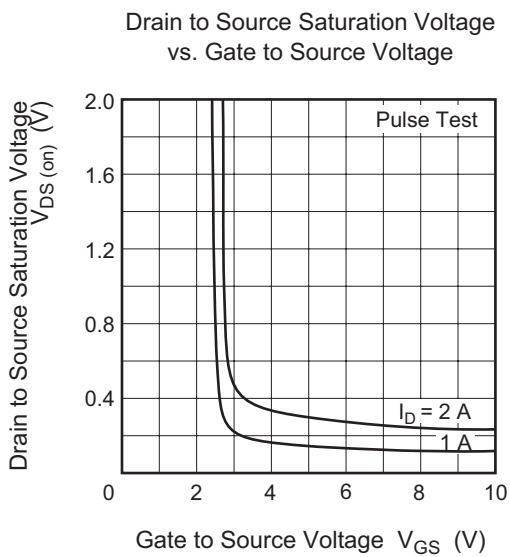
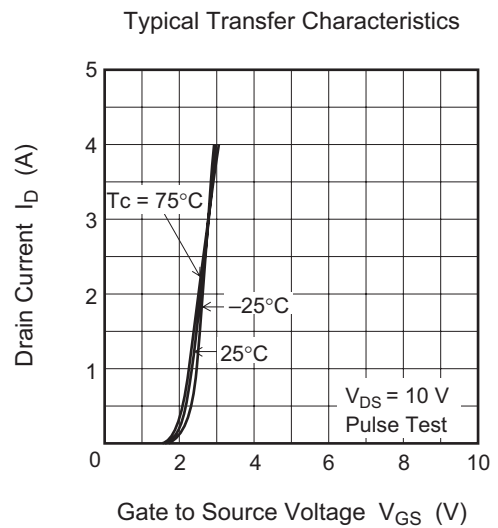
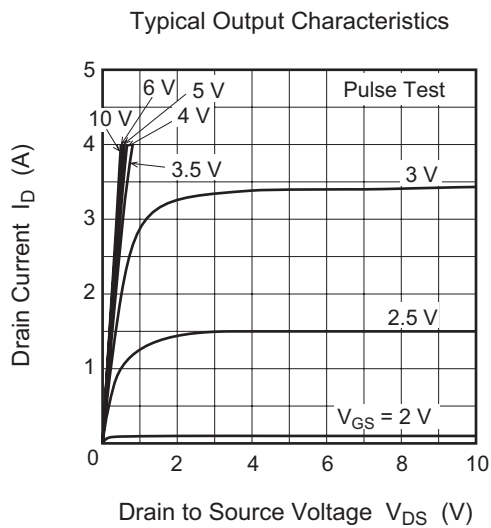
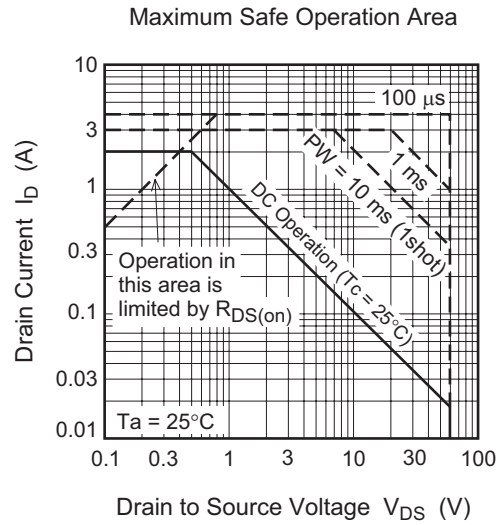
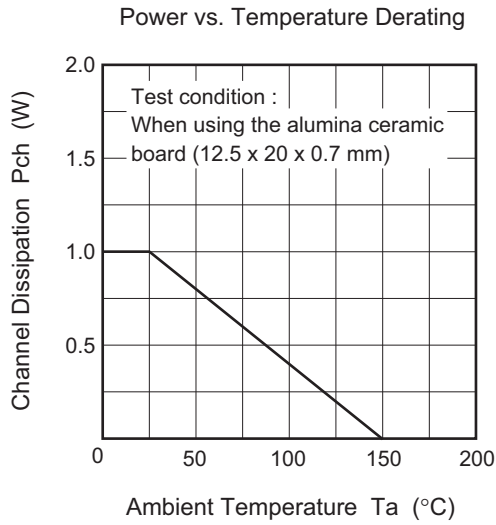
Electrical Characteristics

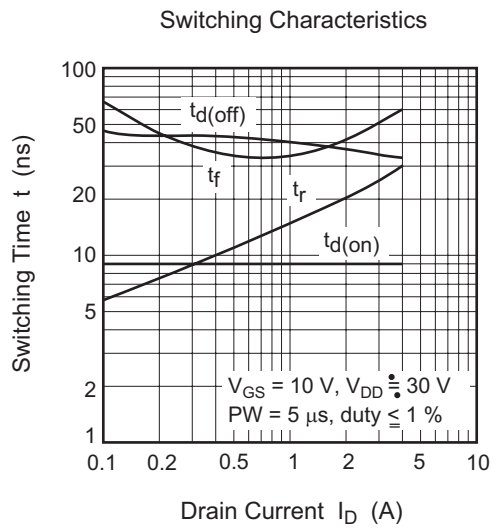
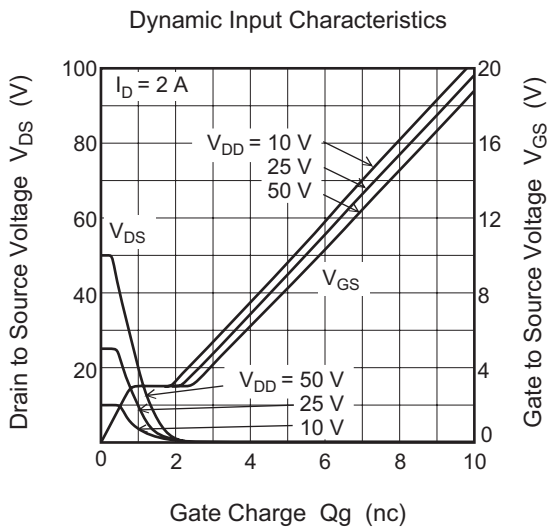
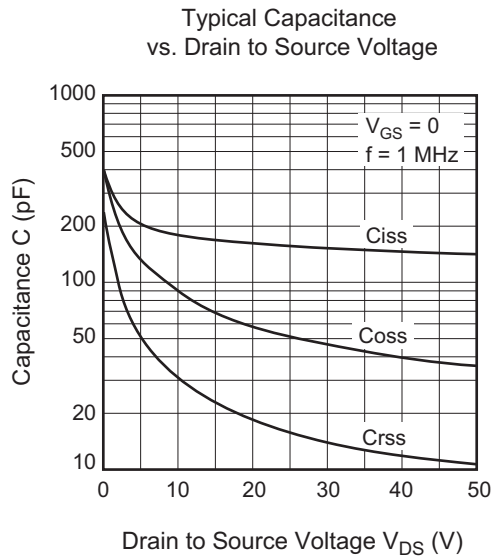
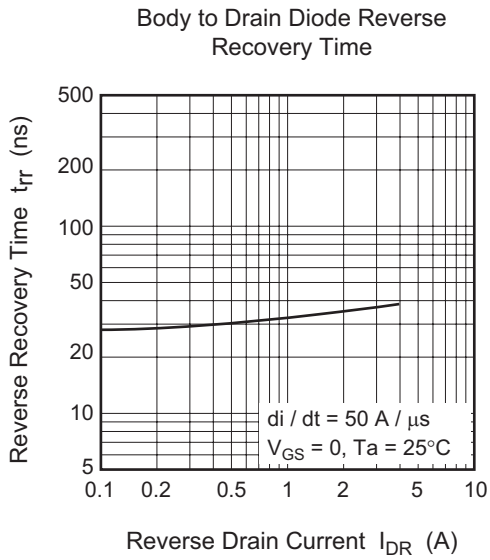
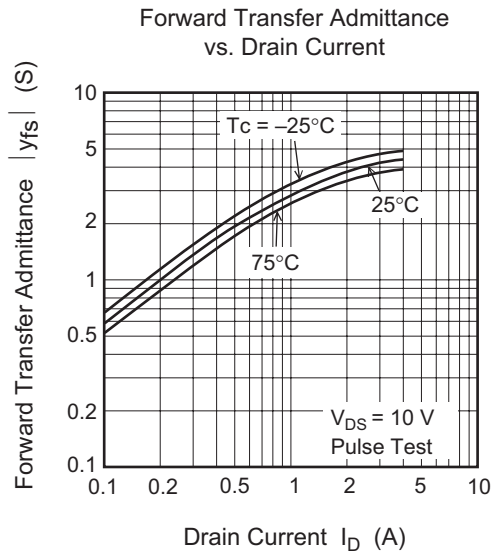
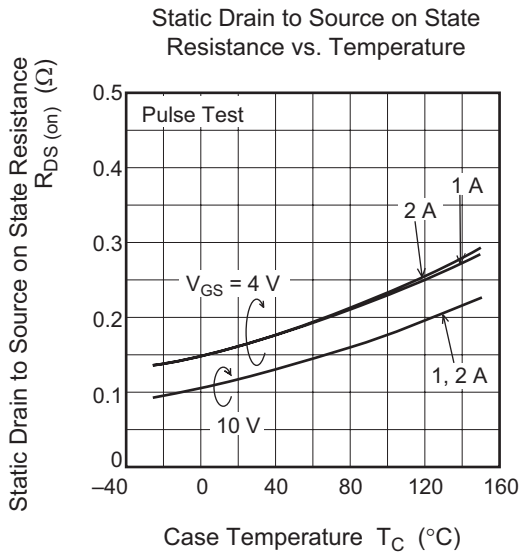
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	60	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.0	—	2.0	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS(on)}	—	0.12	0.16	Ω	I _D = 1 A, V _{GS} = 10 V*3
	R _{DS(on)}	—	0.16	0.25	Ω	I _D = 1 A, V _{GS} = 4 V*3
Forward transfer admittance	y _{fs}	1.6	2.8	—	S	I _D = 1 A, V _{DS} = 10 V*3
Input capacitance	C _{iss}	—	180	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	90	—	pF	
Reverse transfer capacitance	C _{rss}	—	30	—	pF	
Turn-on delay time	t _{d(on)}	—	9	—	ns	V _{GS} = 10 V, I _D = 1 A, R _L = 30 Ω
Rise time	t _r	—	15	—	ns	
Turn-off delay time	t _{d(off)}	—	40	—	ns	
Fall time	t _f	—	35	—	ns	
Body to drain diode forward voltage	V _{DF}	—	0.9	—	V	I _D = 2 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	35	—	ns	I _F = 2 A, V _{GS} = 0 di _F /dt = 50A/μs

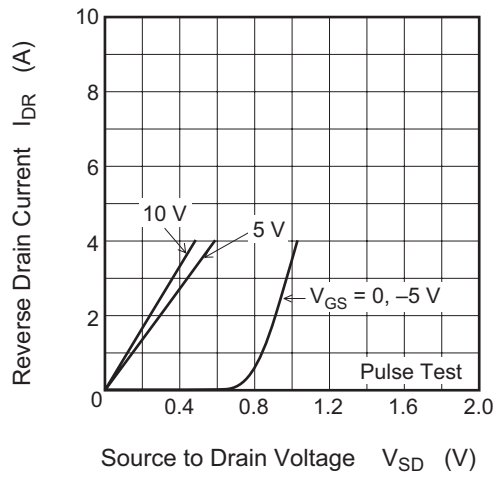
Notes: 3. Pulse test

Main Characteristics

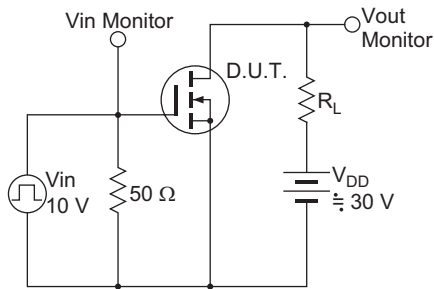




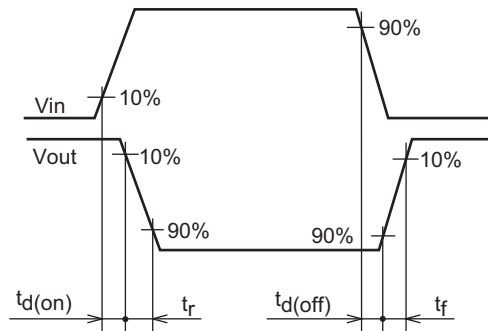
Reverse Drain Current vs. Source to Drain Voltage



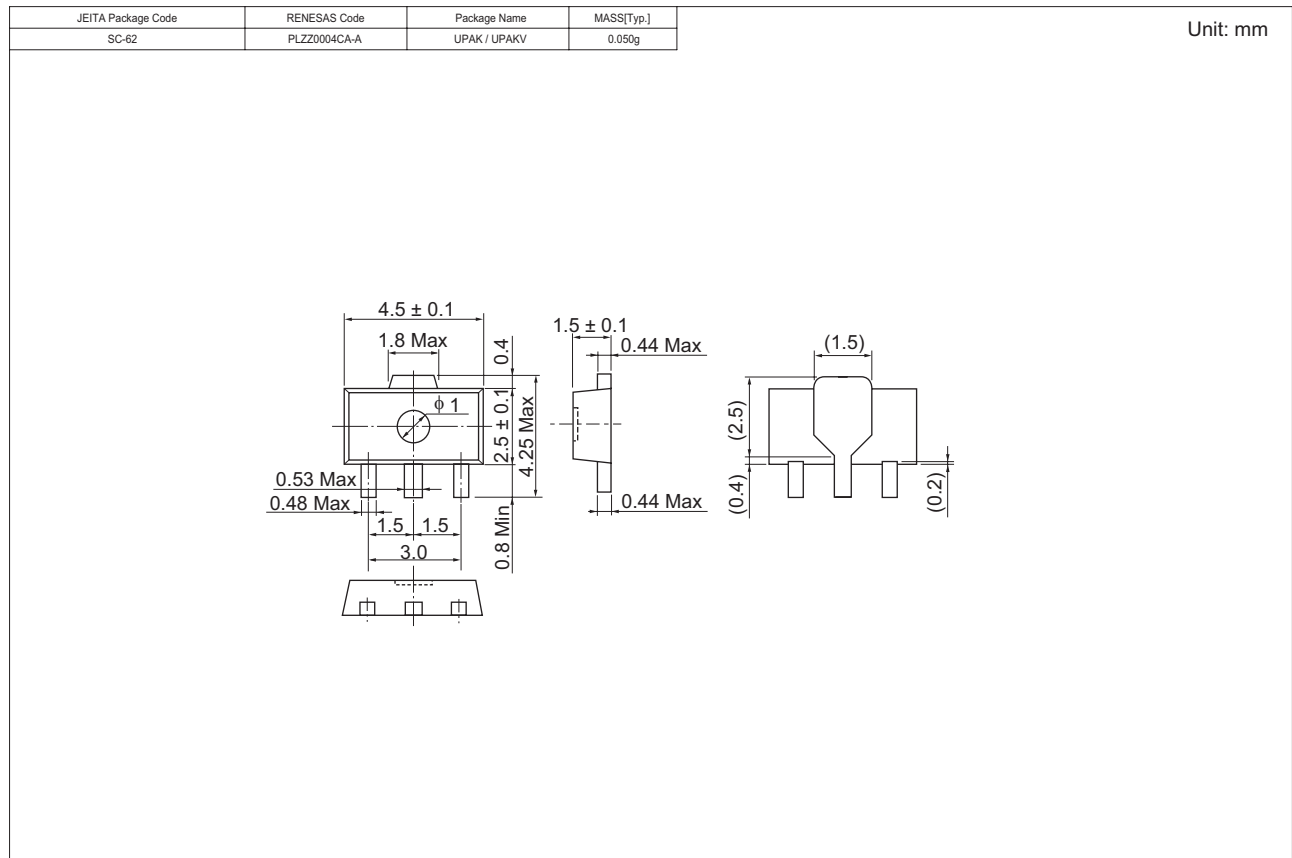
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SK2788VYTL-E	1000 pcs	Taping
2SK2788VYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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