

HAT3008R, HAT3008RJ

Silicon N / P Channel Power MOS FET
High Speed Power Switching

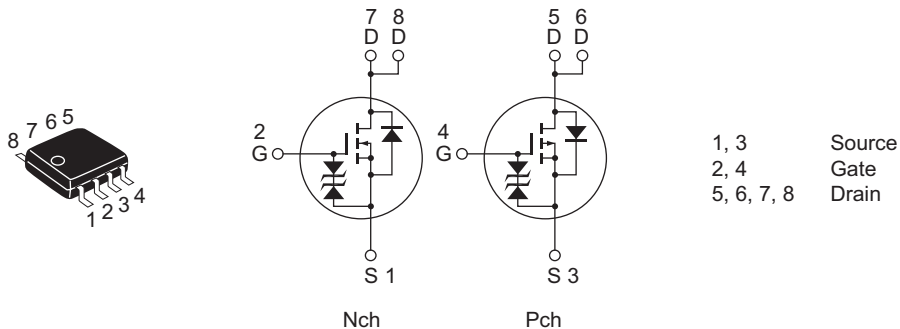
REJ03G1198-0400
(Previous: ADE-208-536B)
Rev.4.00
Sep 07, 2005

Features

- For Automotive Application (at Type Code "J")
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	-60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	5	-3.5	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	40	-28	A
Body-drain diode reverse drain current	I_{DR}	5	-3.5	A
Avalanche current	HAT3008R	—	—	—
	HAT3008RJ	5	-3.5	A
Avalanche energy	HAT3008R	—	—	—
	HAT3008RJ	2.14	1.05	mJ
Channel dissipation	P_{ch} ^{Note 2}	2	2	W
Channel dissipation	P_{ch} ^{Note 3}	3	3	W
Channel temperature	T_{ch}	150	150	°C
Storage temperature	T_{stg}	-55 to +150	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), $PW \leq 10 s$

3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), $PW \leq 10 s$

4. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

N Channel

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$	
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$	
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
	HAT3008RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	—	μA	$V_{DS} = 48 \text{ V}$, $V_{GS} = 0$ $T_a = 125^\circ C$
	HAT3008RJ	I_{DSS}	—	—	10	μA	
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.2	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$	
Static drain to source on state resistance	$R_{DS(on)}$	—	0.043	0.058	Ω	$I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 5}	
	$R_{DS(on)}$	—	0.056	0.084	Ω	$I_D = 3 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note 5}	
Forward transfer admittance	$ y_{fs} $	6	9	—	S	$I_D = 3 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 5}	
Input capacitance	C_{iss}	—	520	—	pF	$V_{DS} = 10 \text{ V}$	
Output capacitance	C_{oss}	—	270	—	pF	$V_{GS} = 0$	
Reverse transfer capacitance	C_{rss}	—	100	—	pF	$f = 1 \text{ MHz}$	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 3 \text{ A}$ $V_{DD} \cong 30 \text{ V}$	
Rise time	t_r	—	40	—	ns		
Turn-off delay time	$t_{d(off)}$	—	110	—	ns		
Fall time	t_f	—	80	—	ns		
Body-drain diode forward voltage	V_{DF}	—	0.84	1.1	V	$I_F = 5 \text{ A}$, $V_{GS} = 0$ ^{Note 5}	
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 5 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$	

Note: 5. Pulse test

P Channel

(Ta = 25°C)

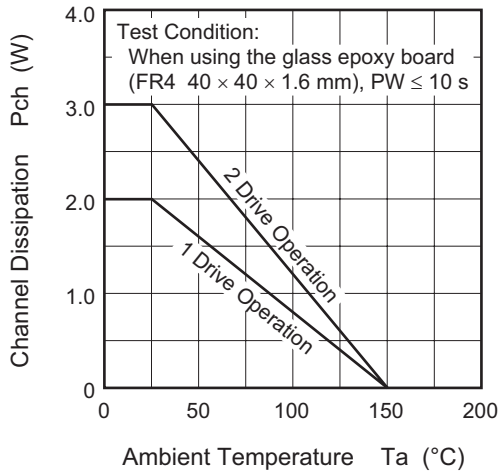
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}, V_{GS} = 0$	
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$	
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	-1	μA	$V_{DS} = -60 \text{ V}, V_{GS} = 0$
	HAT3008RJ	I_{DSS}	—	—	-0.1	μA	
Zero gate voltage drain current	HAT3008R	I_{DSS}	—	—	—	μA	$V_{DS} = -48 \text{ V}, V_{GS} = 0$ $T_a = 125^\circ\text{C}$
	HAT3008RJ	I_{DSS}	—	—	-10	μA	
Gate to source cutoff voltage	$V_{GS(off)}$	-1.2	—	-2.2	V	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$	
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	$I_D = -2 \text{ A}, V_{GS} = -10 \text{ V}$ ^{Note 6}	
	$R_{DS(on)}$	—	0.16	0.23	Ω	$I_D = -2 \text{ A}, V_{GS} = -4 \text{ V}$ ^{Note 6}	
Forward transfer admittance	$ y_{fs} $	3	4.5	—	S	$I_D = -2 \text{ A}, V_{DS} = -10 \text{ V}$ ^{Note 6}	
Input capacitance	C_{iss}	—	600	—	pF	$V_{DS} = -10 \text{ V}$	
Output capacitance	C_{oss}	—	290	—	pF	$V_{GS} = 0$	
Reverse transfer capacitance	C_{rss}	—	75	—	pF	$f = 1 \text{ MHz}$	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = -10 \text{ V}, I_D = -2 \text{ A}$ $V_{DD} \cong -30 \text{ V}$	
Rise time	t_r	—	30	—	ns		
Turn-off delay time	$t_{d(off)}$	—	100	—	ns		
Fall time	t_f	—	55	—	ns		
Body-drain diode forward voltage	V_{DF}	—	-0.98	-1.28	V	$I_F = -3.5 \text{ A}, V_{GS} = 0$ ^{Note 6}	
Body-drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -3.5 \text{ A}, V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$	

Note: 6. Pulse test

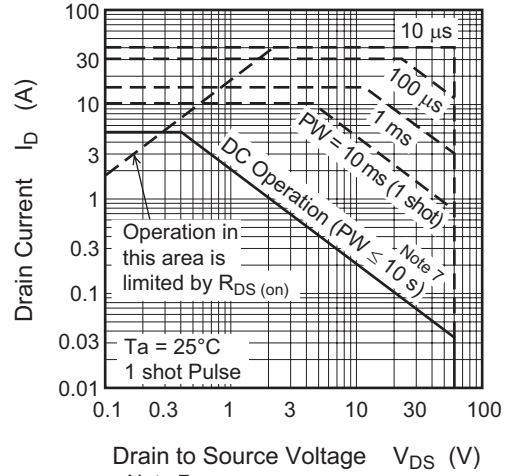
Main Characteristics

N Channel

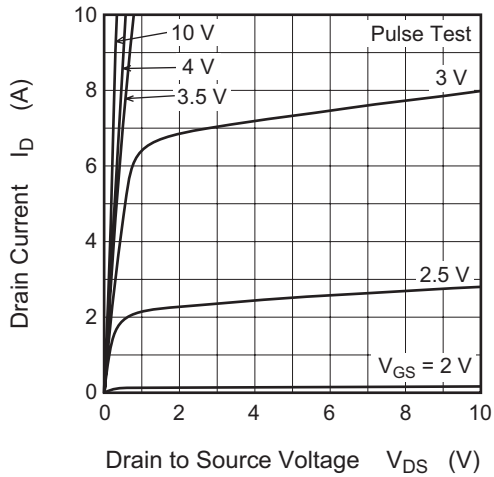
Power vs. Temperature Derating



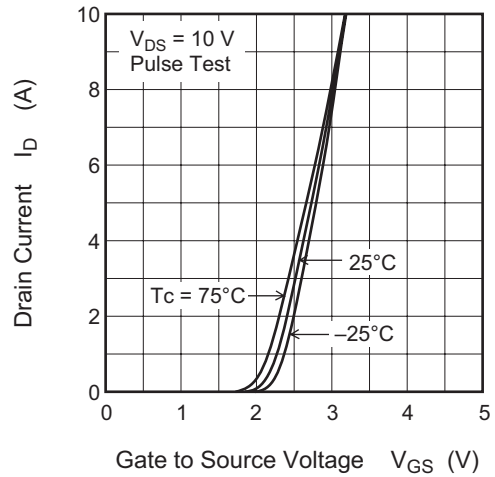
Maximum Safe Operation Area



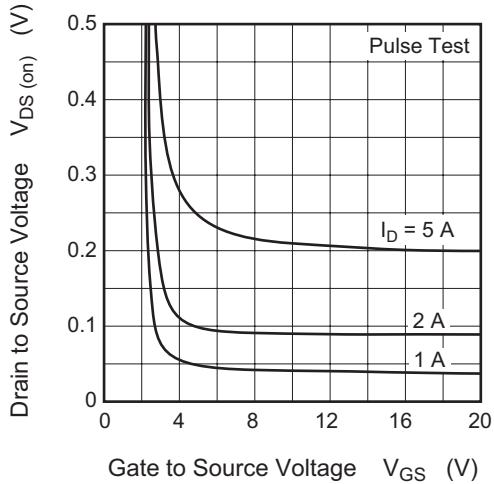
Typical Output Characteristics



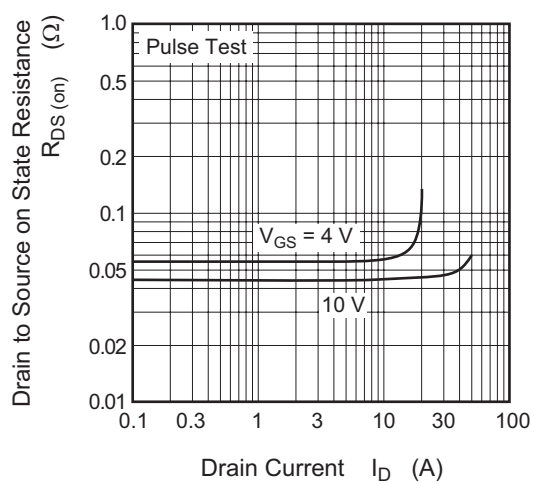
Typical Transfer Characteristics

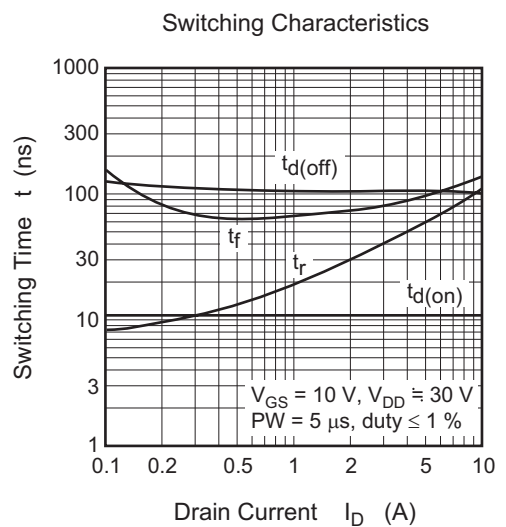
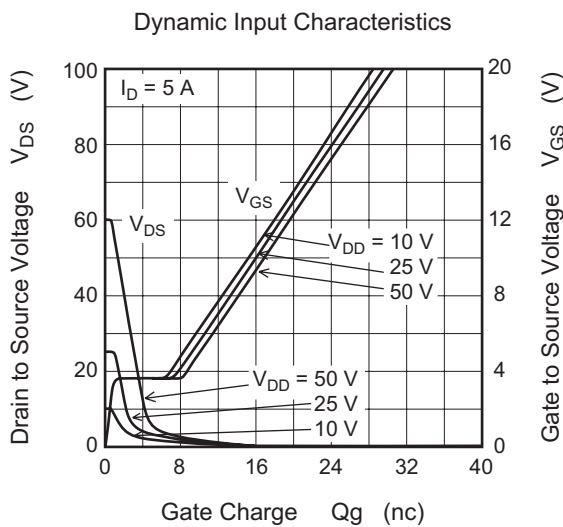
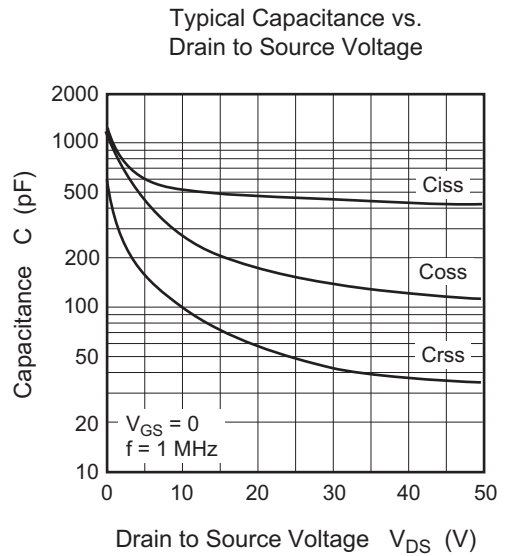
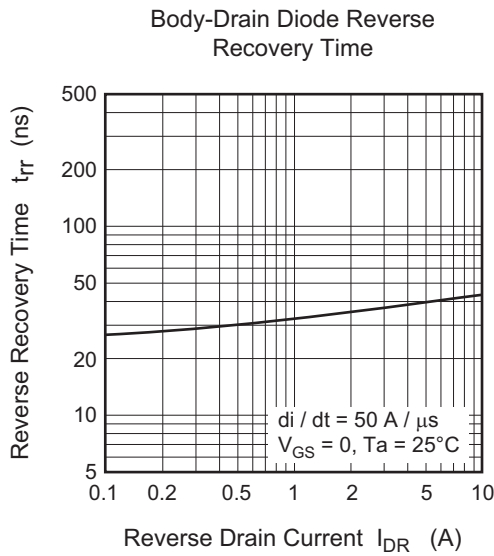
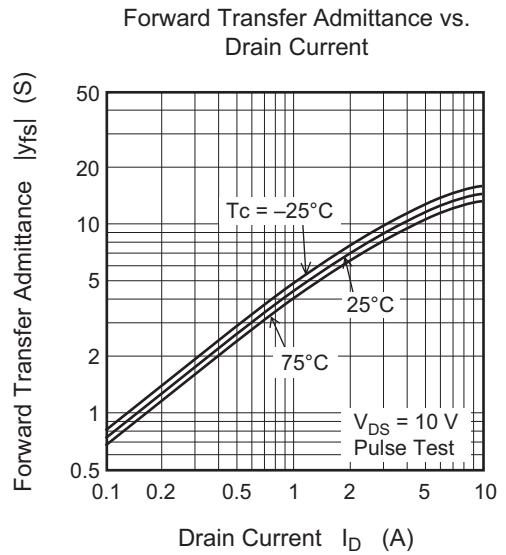
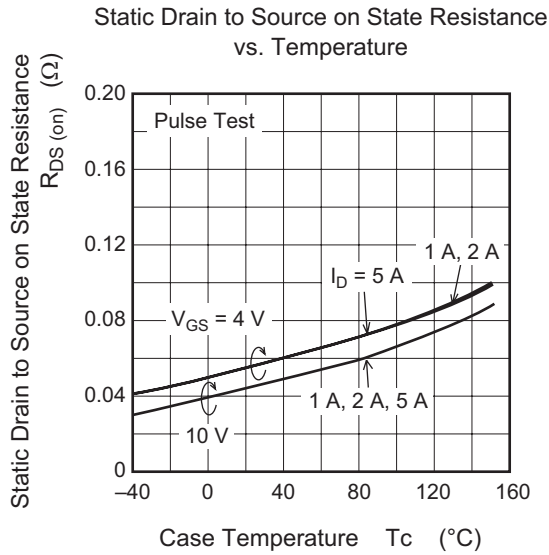


Drain to Source Saturation Voltage vs. Gate to Source Voltage

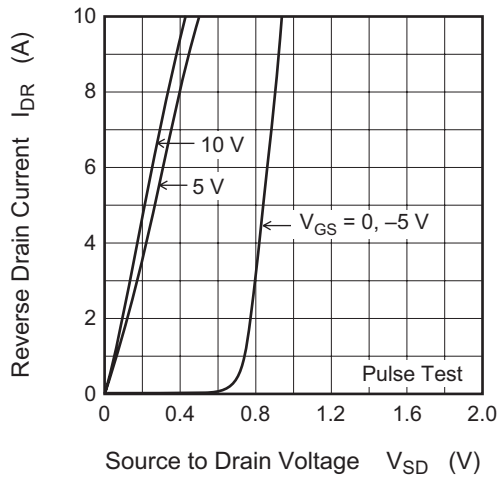


Static Drain to Source on State Resistance vs. Drain Current

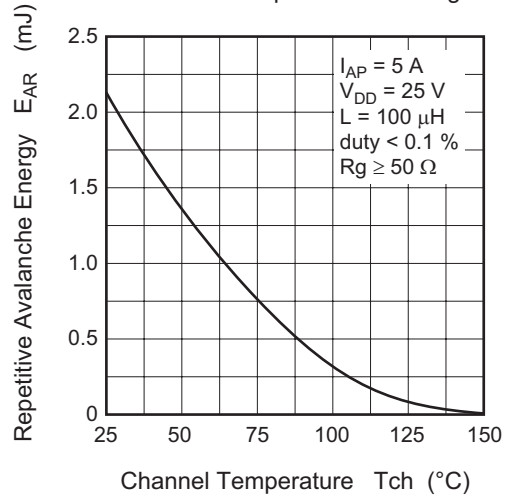




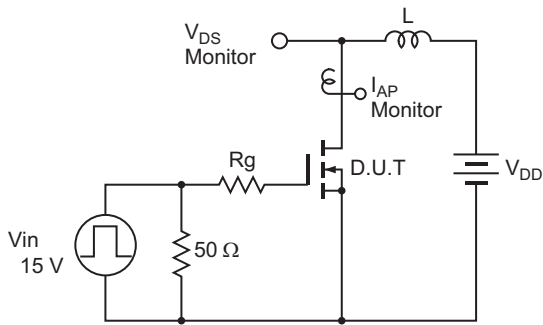
Reverse Drain Current vs. Source to Drain Voltage



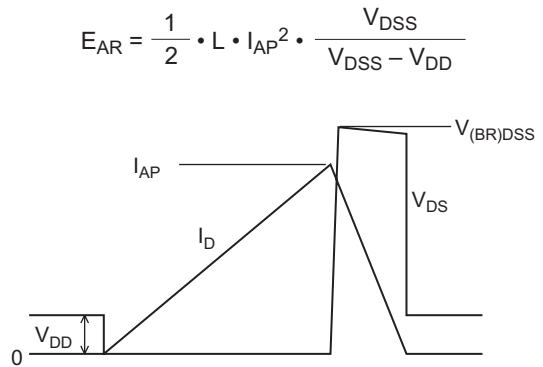
Maximum Avalanche Energy vs. Channel Temperature Derating



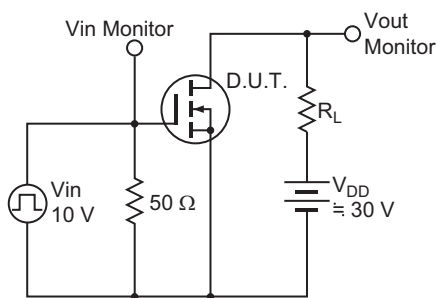
Avalanche Test Circuit



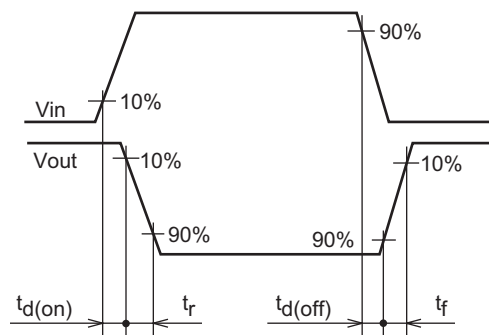
Avalanche Waveform



Switching Time Test Circuit

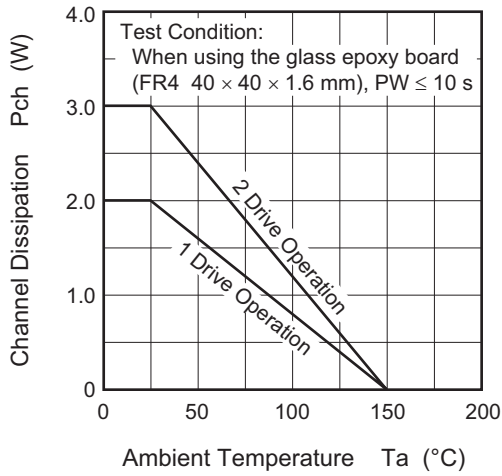


Switching Time Waveform

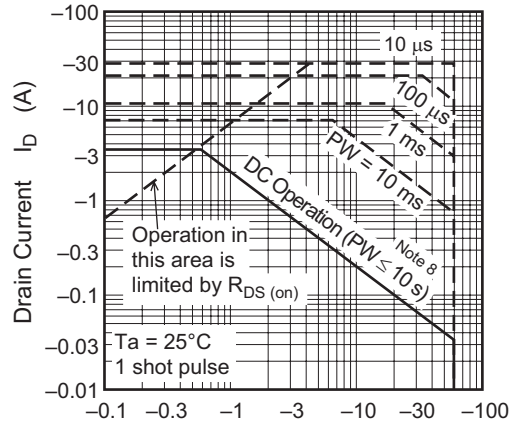


P Channel

Power vs. Temperature Derating



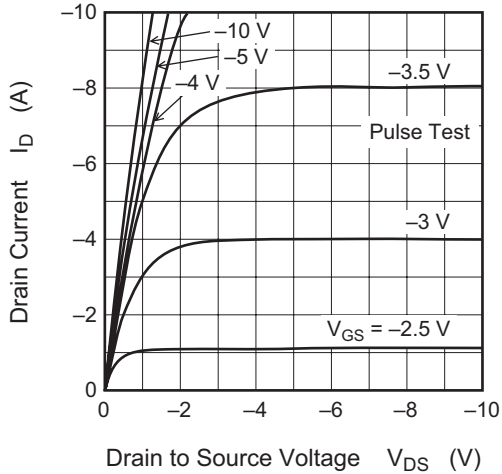
Maximum Safe Operation Area



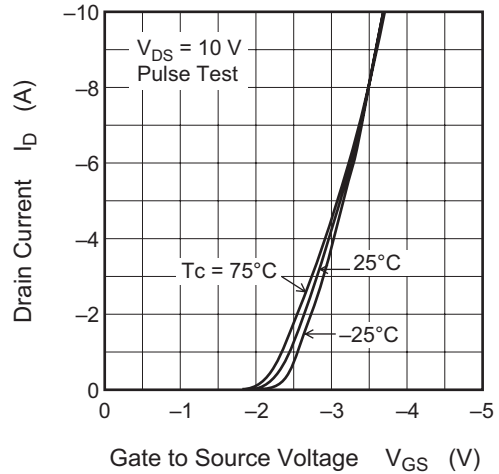
Drain to Source Voltage VDS (V)

Note 8:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

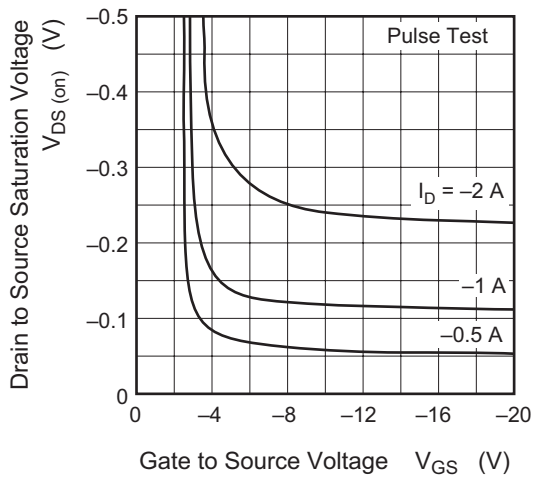
Typical Output Characteristics



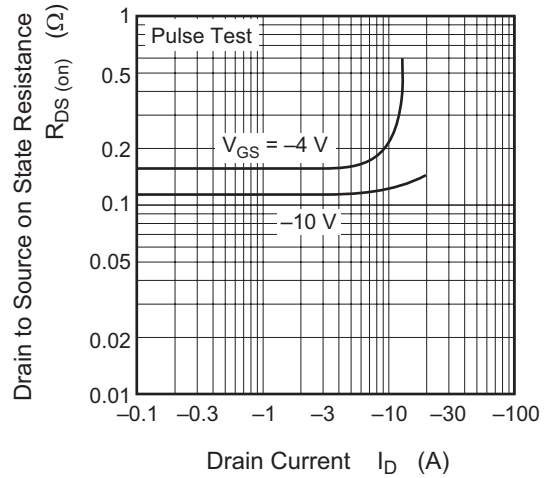
Typical Transfer Characteristics

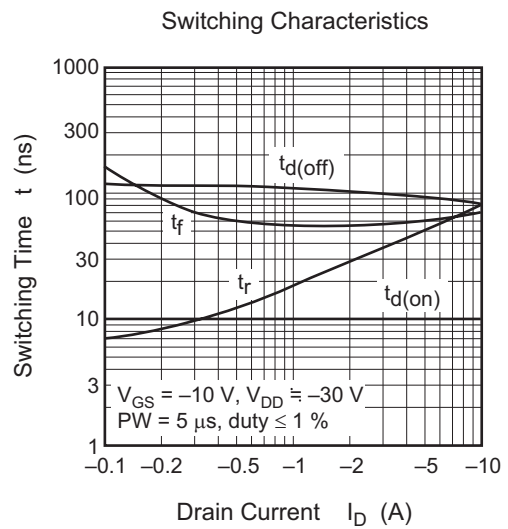
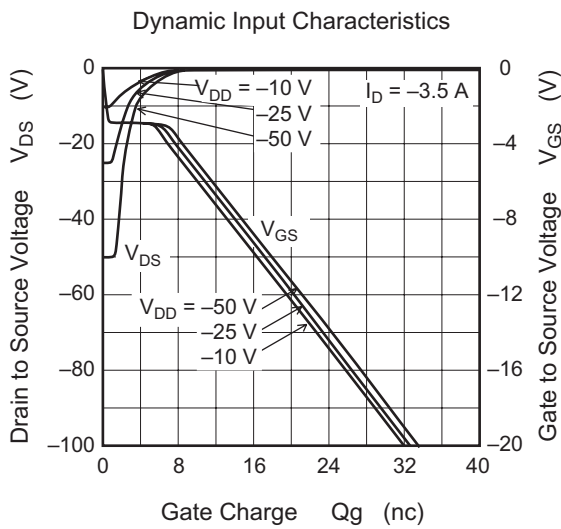
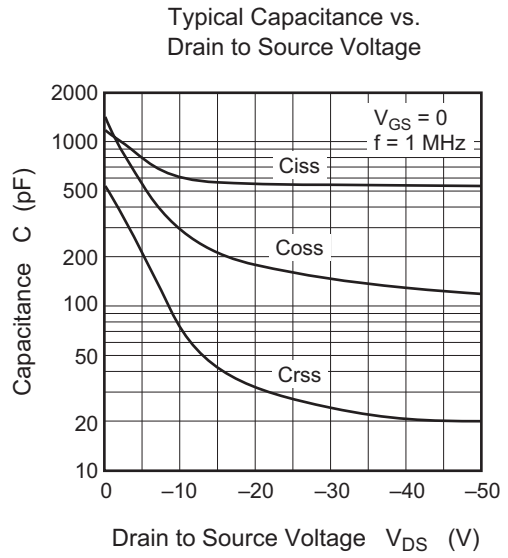
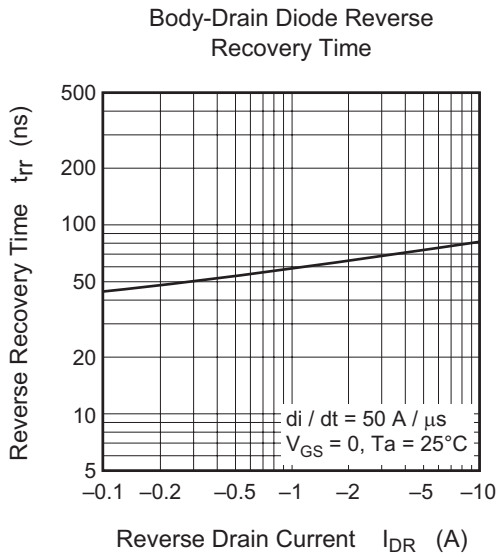
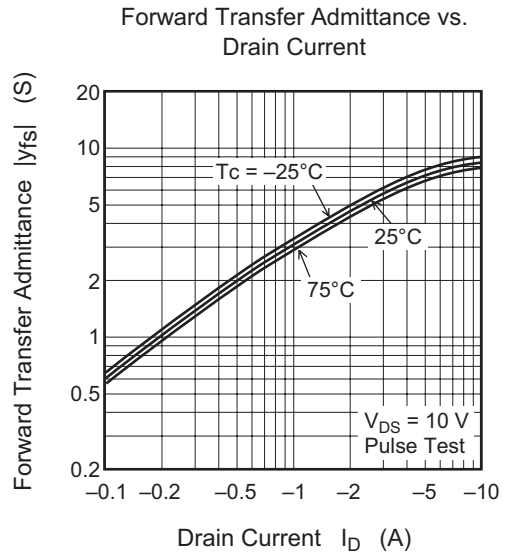
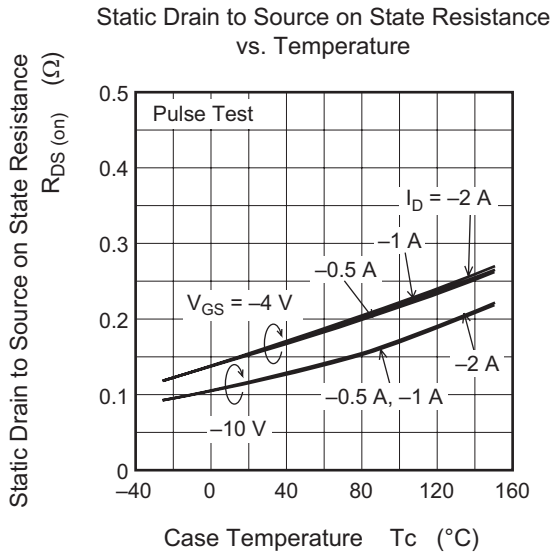


Drain to Source Saturation Voltage vs. Gate to Source Voltage

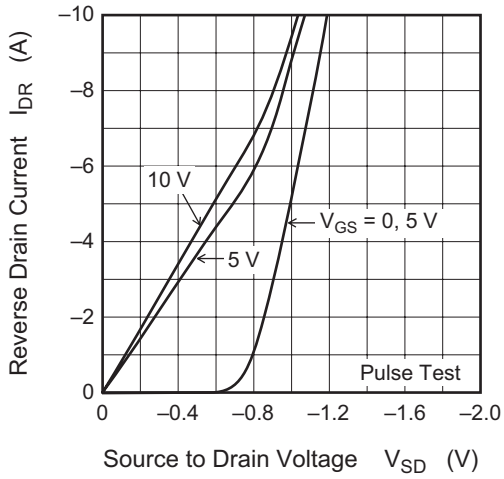


Static Drain to Source on State Resistance vs. Drain Current

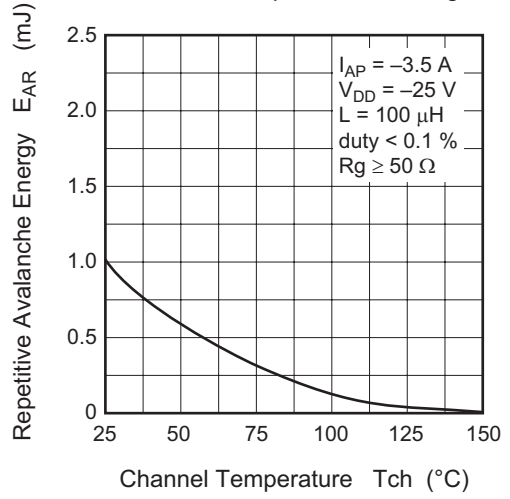




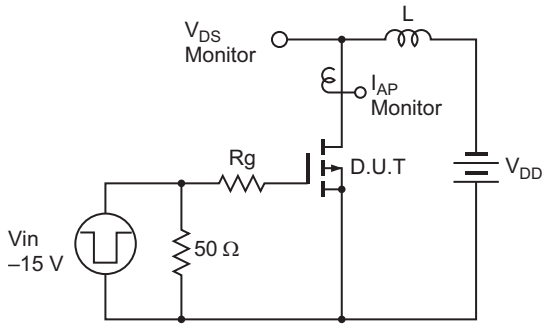
Reverse Drain Current vs. Source to Drain Voltage



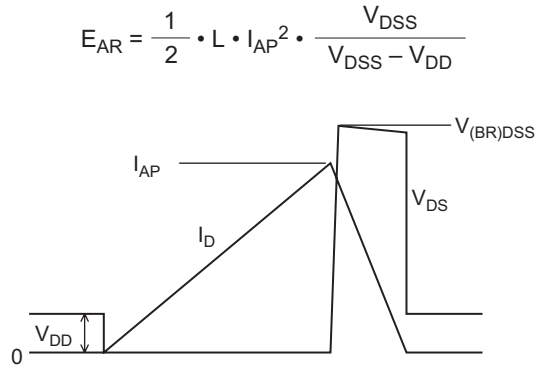
Maximum Avalanche Energy vs. Channel Temperature Derating



Avalanche Test Circuit

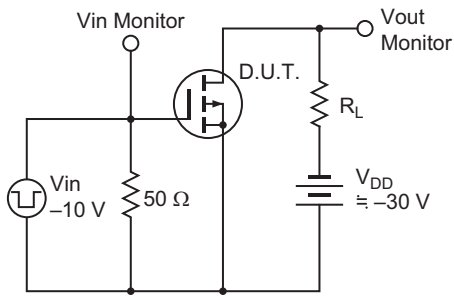


Avalanche Waveform

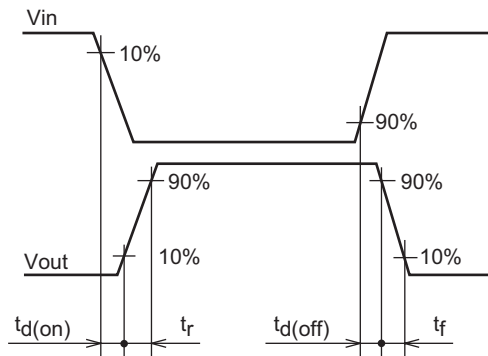


$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

Switching Time Test Circuit

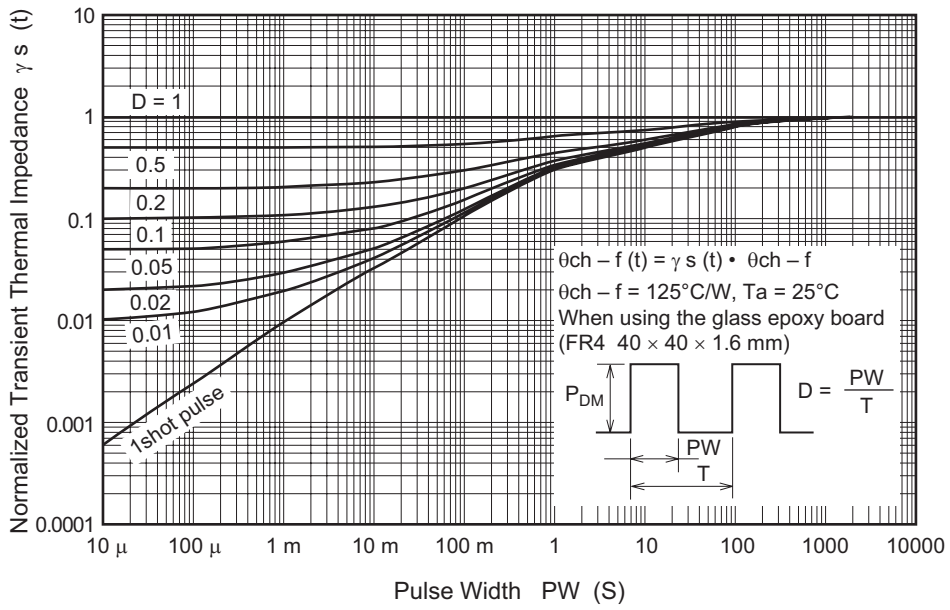


Switching Time Waveform

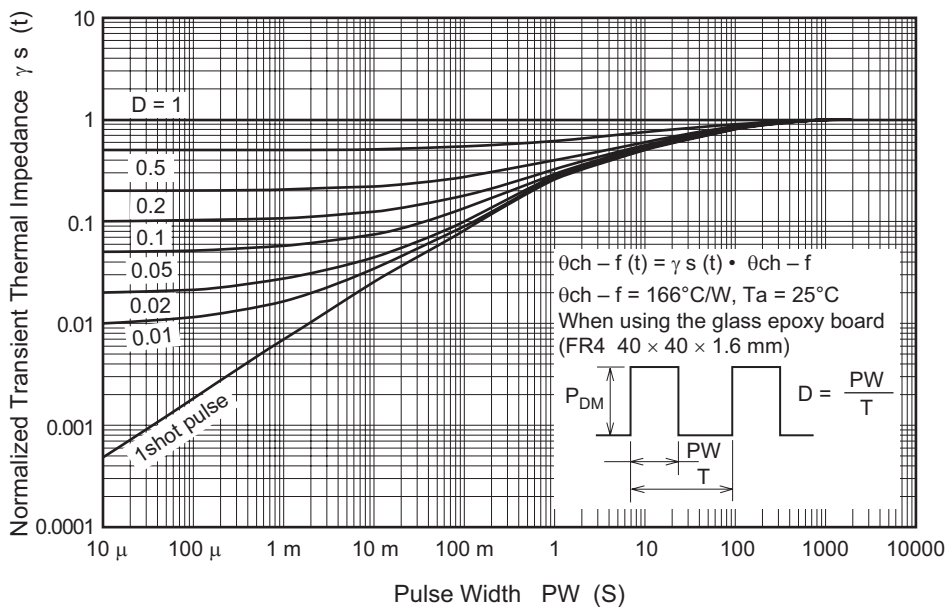


Common

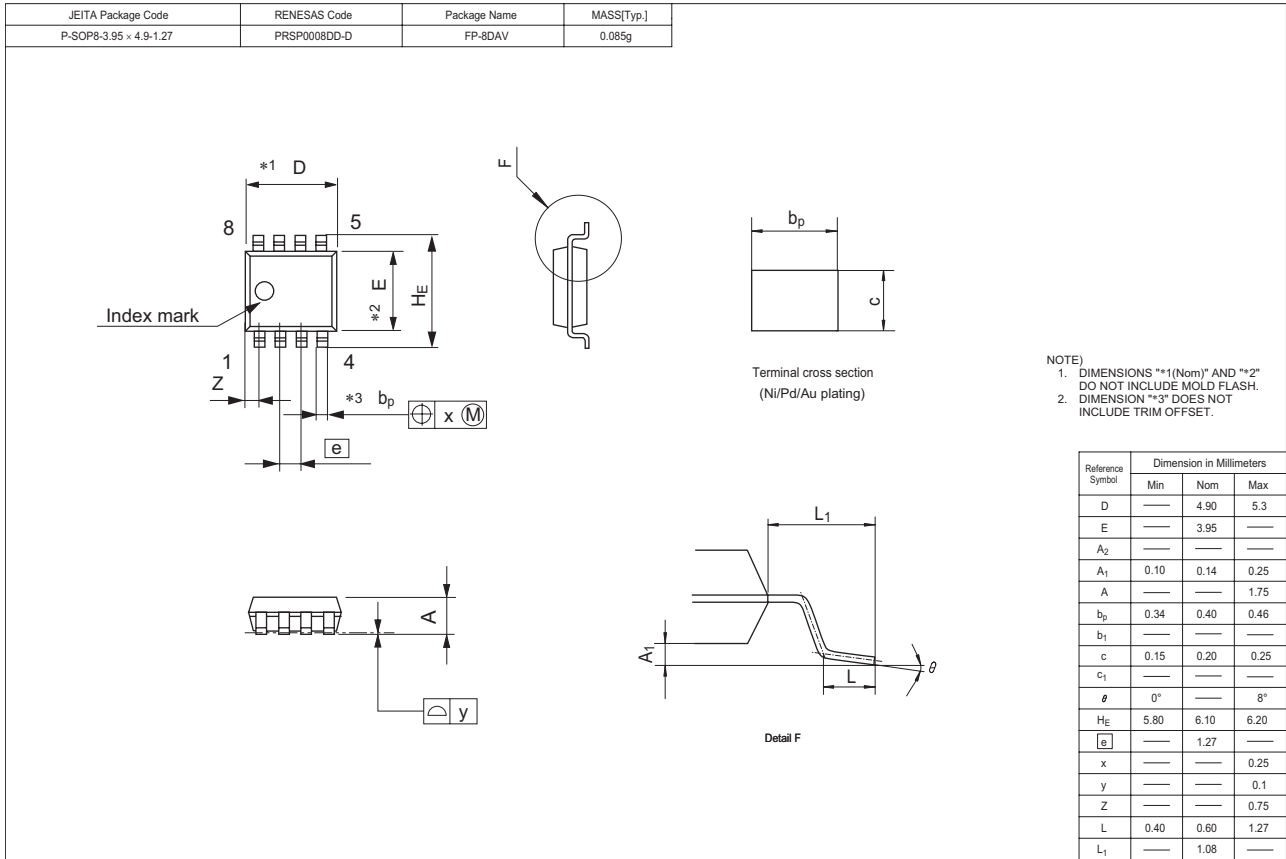
Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)



Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT3008R-EL-E	2500 pcs	Taping
HAT3008RJ-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510