Freescale Semiconductor
Technical Data

Document Number: MRF6V4300N
Rev. 0, 7/2008

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF6V4300NR1
MRF6V4300NBR1

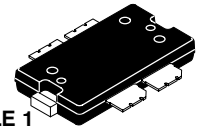
10-600 MHz, 300 W, 50 V
LATERAL N-CHANNEL
SINGLE-ENDED
BROADBAND
RF POWER MOSFETs

Designed primarily for CW large-signal output and driver applications with frequencies up to 600 MHz. Devices are unmatched and are suitable for use in industrial, medical and scientific applications.

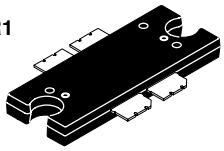
- Typical CW Performance: V_{DD} = 50 Volts, I_{DQ} = 900 mA, P_{out} = 300 Watts, f = 450 MHz
  Power Gain — 22 dB
  Drain Efficiency — 60%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 450 MHz, 300 Watts CW Output Power

Features

- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Excellent Thermal Stability
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

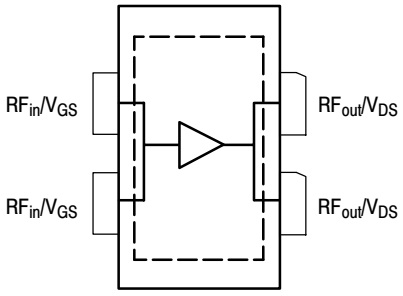


CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF6V4300NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF6V4300NBR1

PARTS ARE SINGLE-ENDED



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case Case Temperature 83°C, 300 W CW	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

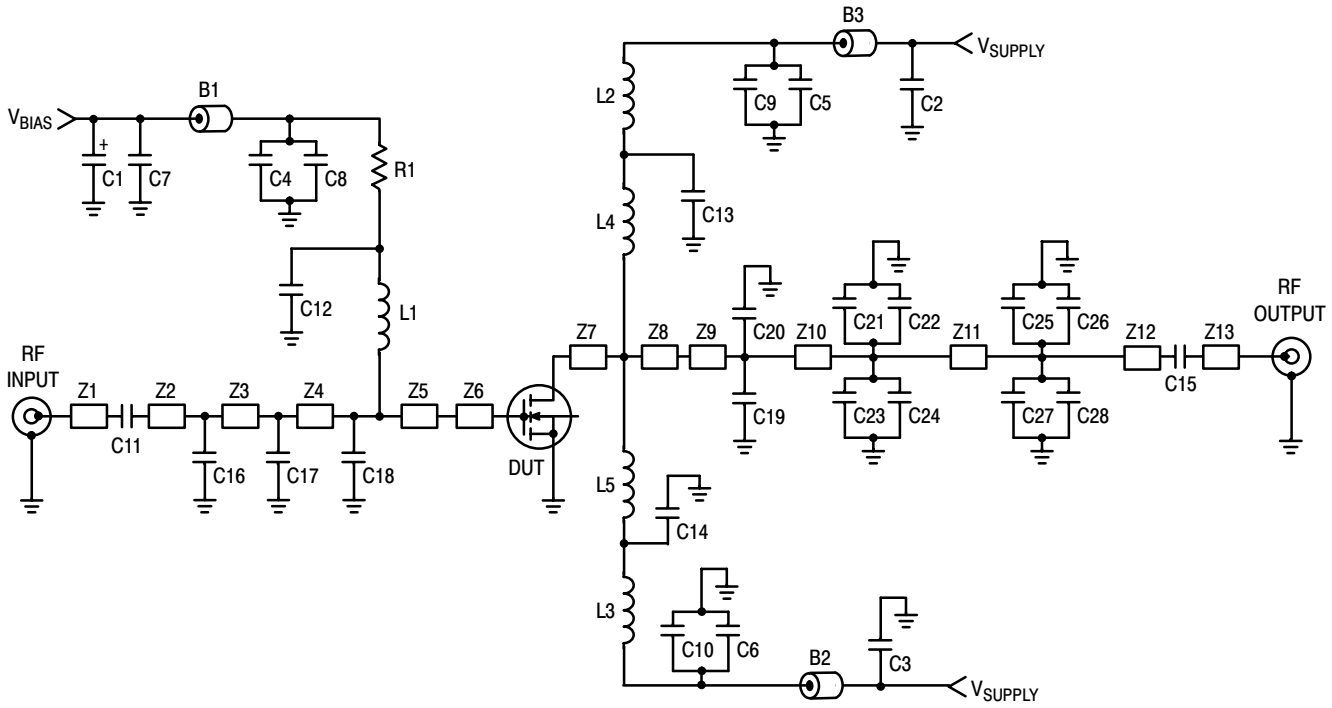
Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
Drain-Source Breakdown Voltage (I_D = 150 mA, V_{GS} = 0 Vdc)	$V_{(BR)DSS}$	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	50	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	2.5	mA
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 800 μAdc)	$V_{GS(th)}$	0.9	1.65	2.4	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 900 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.9	2.7	3.4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.25	—	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.8	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	105	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	304	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 900 mA, P_{out} = 300 W, f = 450 MHz, CW					
Power Gain	G_{ps}	20	22	24	dB
Drain Efficiency	η_D	58	60	—	%
Input Return Loss	IRL	—	-16	-9	dB

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

ATTENTION: The MRF6V4300N and MRF6V4300NB are high power devices and special considerations must be followed in board design and mounting. Incorrect mounting can lead to internal temperatures which exceed the maximum allowable operating junction temperature. Refer to Freescale Application Note AN3263 (for bolt down mounting) or AN1907 (for solder reflow mounting) **PRIOR TO STARTING SYSTEM DESIGN** to ensure proper mounting of these devices.



Z1	0.900″ x 0.082″ Microstrip	Z8	0.380″ x 0.220″ Microstrip
Z2	0.115″ x 0.170″ Microstrip	Z9	0.040″ x 0.170″ Microstrip
Z3	0.260″ x 0.170″ Microstrip	Z10	0.315″ x 0.170″ Microstrip
Z4	0.380″ x 0.170″ Microstrip	Z11	0.230″ x 0.170″ Microstrip
Z5	0.220″ x 0.220″ Microstrip	Z12	0.390″ x 0.170″ Microstrip
Z6	0.290″ x 0.630″ Microstrip	Z13	0.680″ x 0.082″ Microstrip
Z7	0.220″ x 0.630″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 2. MRF6V4300NR1(NBR1) Test Circuit Schematic

Table 6. MRF6V4300NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Short Ferrite Bead	2743019447	Fair-Rite
B2, B3	Long Ferrite Beads	2743021447	Fair-Rite
C1	47 μF, 25 V, Tantalum Capacitor	T491B476M025AT	Kemet
C2, C3	22 μF, 50 V, Chip Capacitors	C5750JF1H226ZT	TDK
C4, C5, C6, C7	1 μF, 100 V, Chip Capacitors	C3225JB2A105KT	TDK
C8, C9, C10	15 nF, 100 V, Chip Capacitors	C3225CH2A153JT	TDK
C11, C12, C13, C14, C15	240 pF, Chip Capacitors	ATC100B241JT500XT	ATC
C16	9.1 pF, Chip Capacitor	ATC100B9R1JT500XT	ATC
C17	15 pF, Chip Capacitor	ATC100B150JT500XT	ATC
C18	51 pF, Chip Capacitor	ATC100B510JT500XT	ATC
C19, C20	5.6 pF, Chip Capacitors	ATC100B5R6JT500XT	ATC
C21, C22, C23, C24	4.3 pF, Chip Capacitors	ATC100B4R3JT500XT	ATC
C25, C26, C27, C28	4.7 pF, Chip Capacitors	ATC100B4R7JT500XT	ATC
L1	27 nH Inductor	1812SMS-27NJLC	Coilcraft
L2, L3	47 nH Inductors	1812SMS-47NJLC	Coilcraft
L4, L5	5 Turns, #18 AWG Inductors, Hand Wound	Copper Wire	
R1	10 Ω, 1/4 W, Chip Resistor	CRCW120610R1FKEA	Vishay

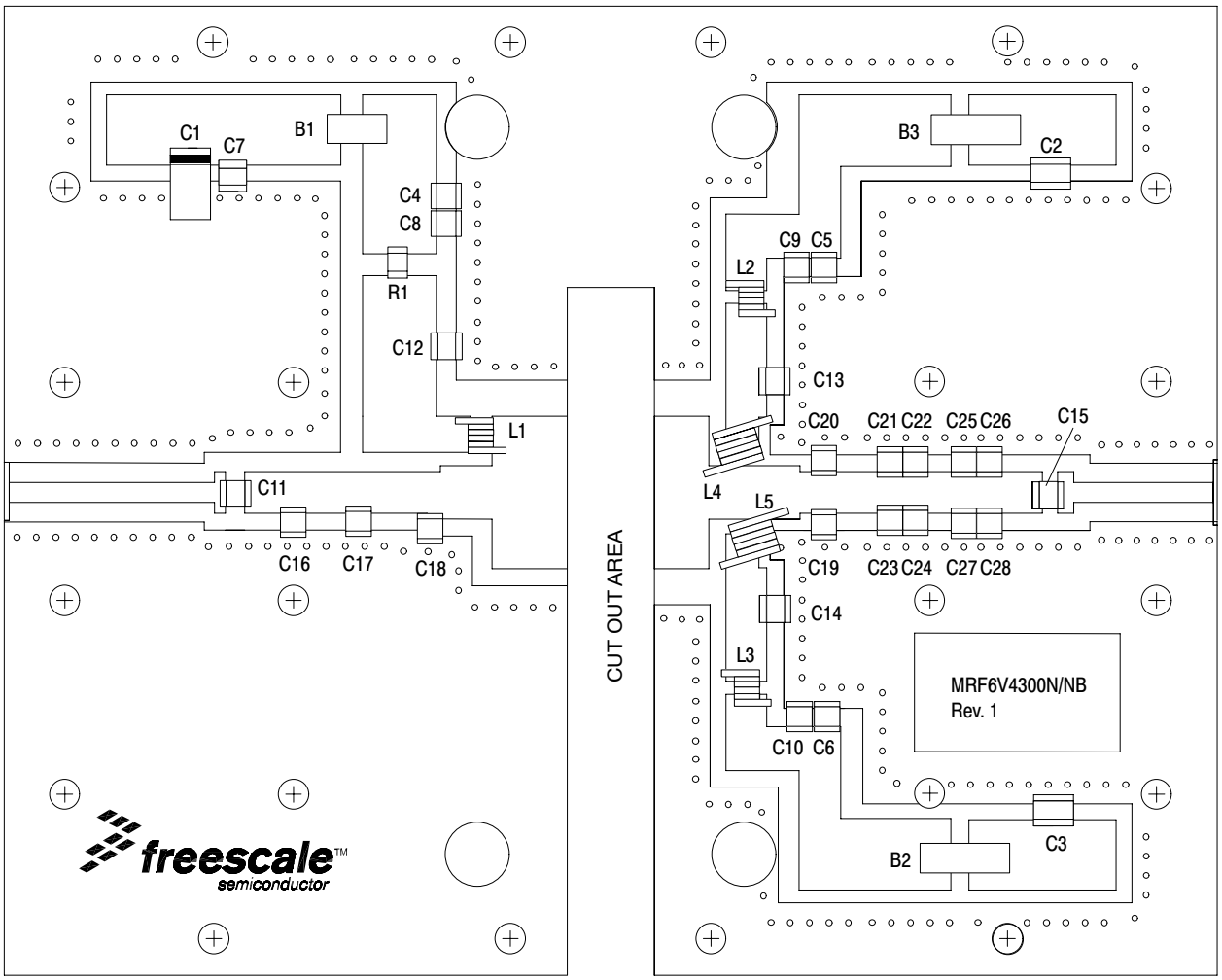


Figure 3. MRF6V4300NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

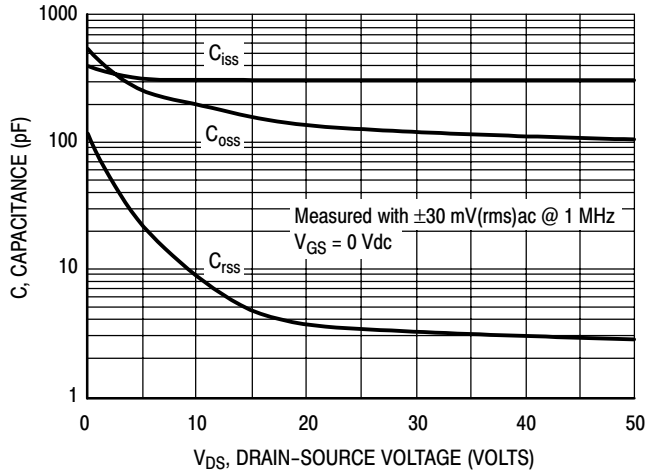


Figure 4. Capacitance versus Drain-Source Voltage

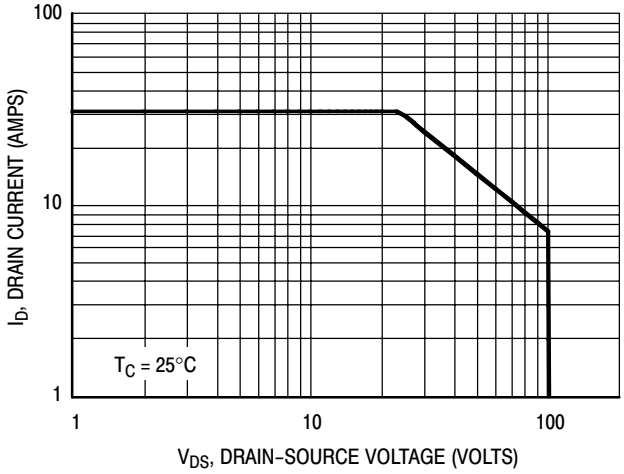


Figure 5. DC Safe Operating Area

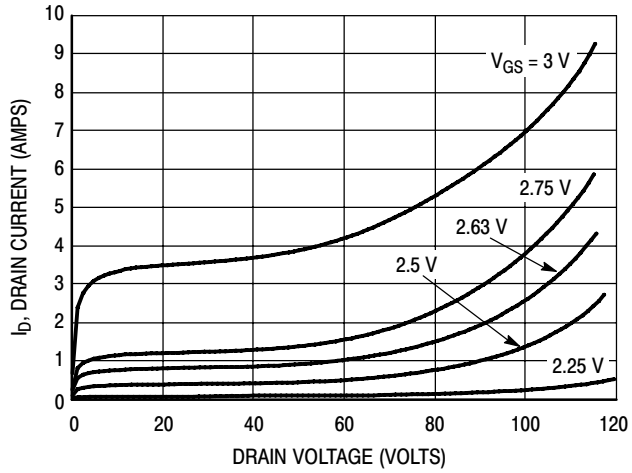


Figure 6. DC Drain Current versus Drain Voltage

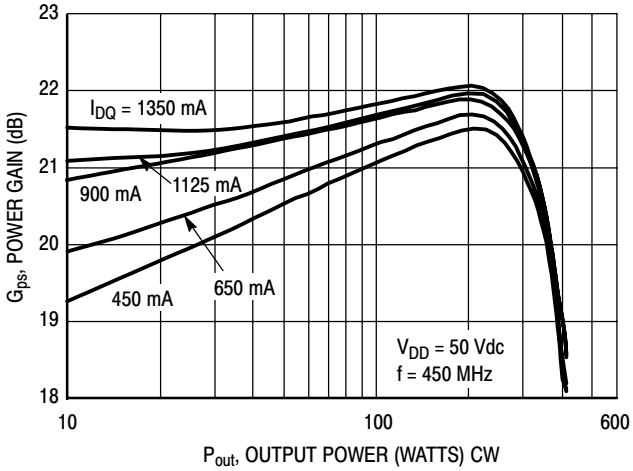


Figure 7. CW Power Gain versus Output Power

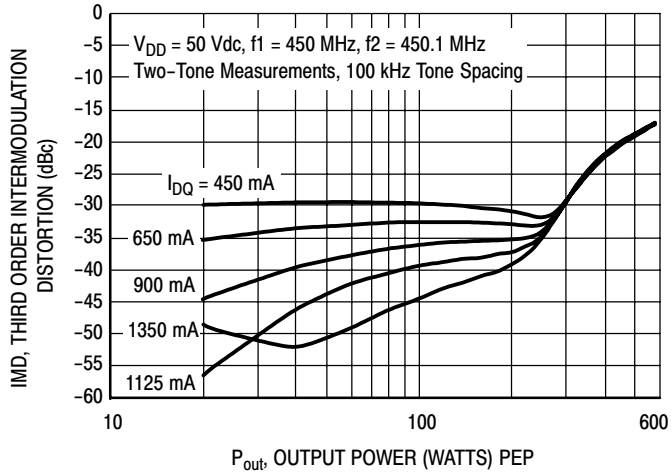


Figure 8. Third Order Intermodulation Distortion versus Output Power

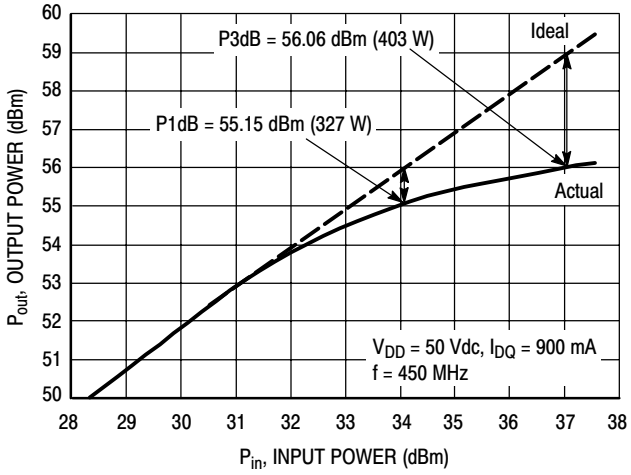


Figure 9. CW Output Power versus Input Power

TYPICAL CHARACTERISTICS

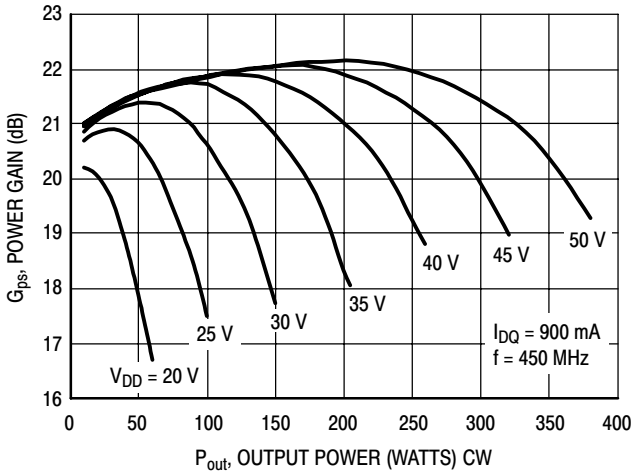


Figure 10. Power Gain versus Output Power

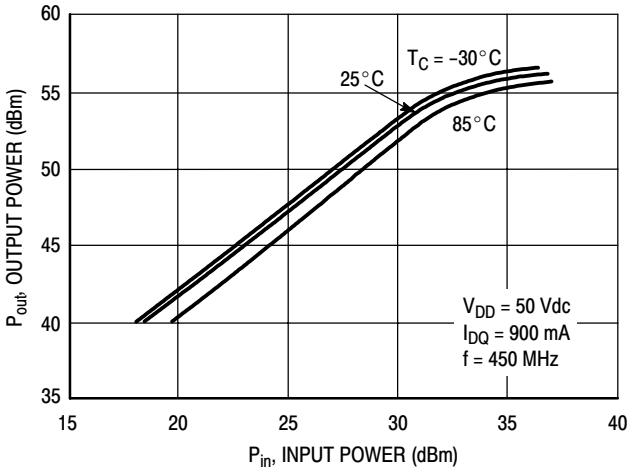


Figure 11. Power Output versus Power Input

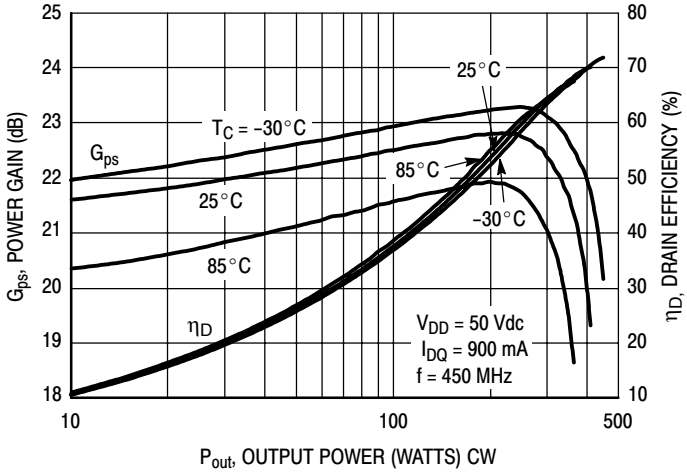
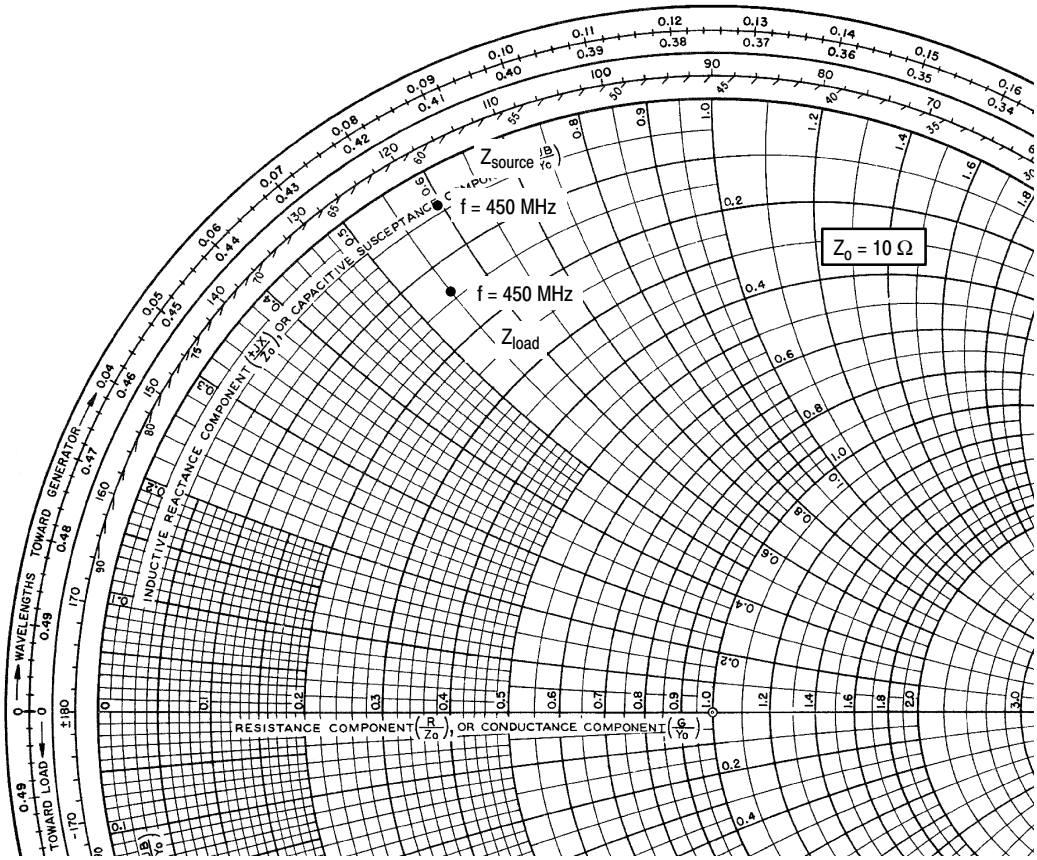


Figure 12. Power Gain and Drain Efficiency versus CW Output Power



V_{DD} = 50 Vdc, I_{DQ} = 900 mA, P_{out} = 300 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
450	0.40 + j5.93	1.42 + j5.5

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

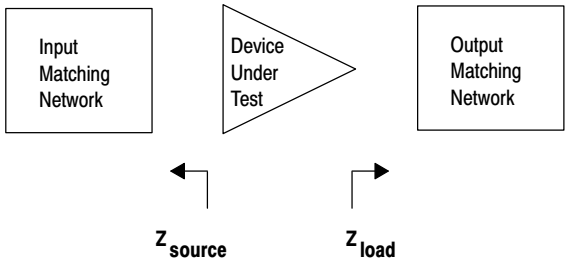
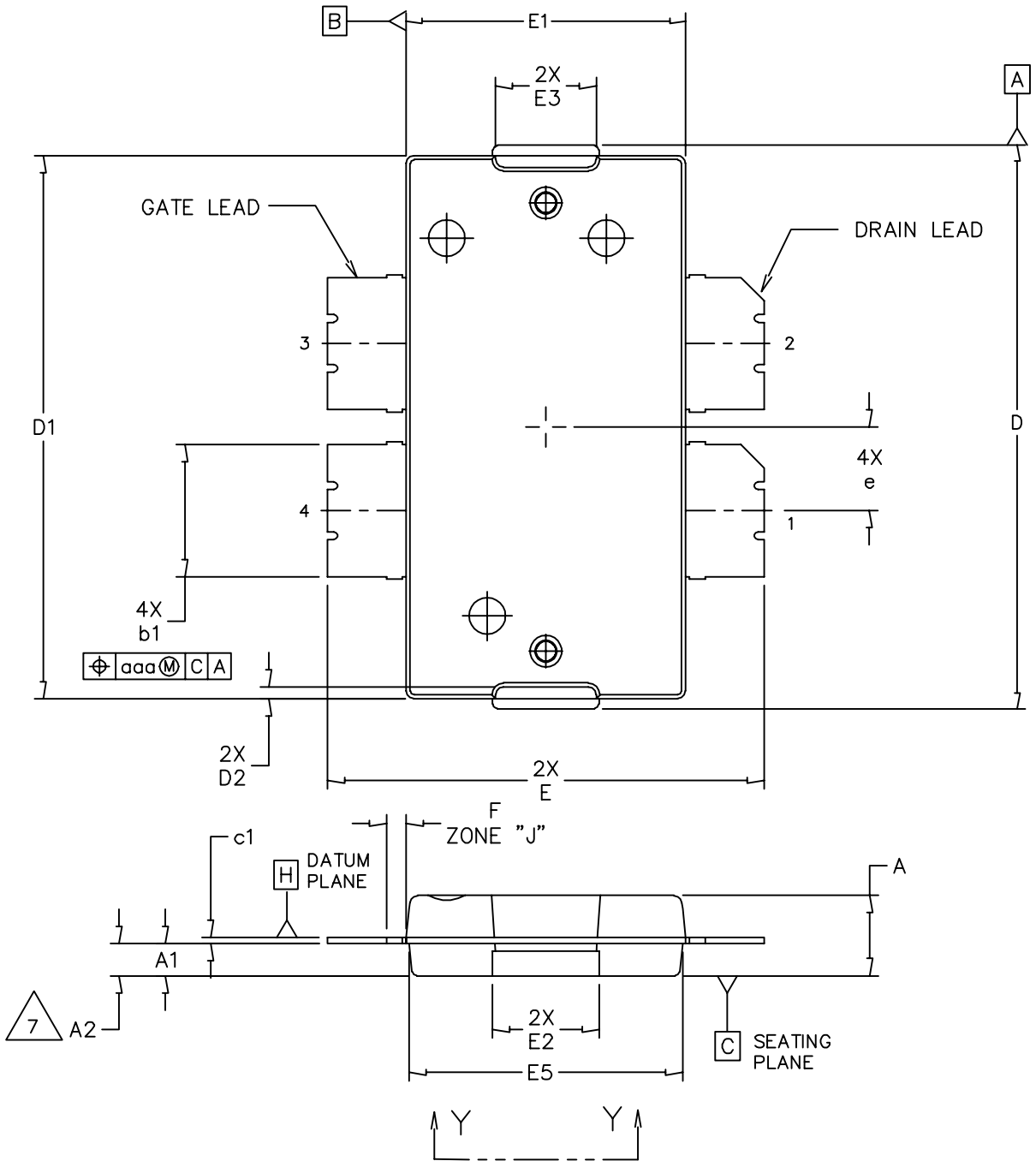


Figure 13. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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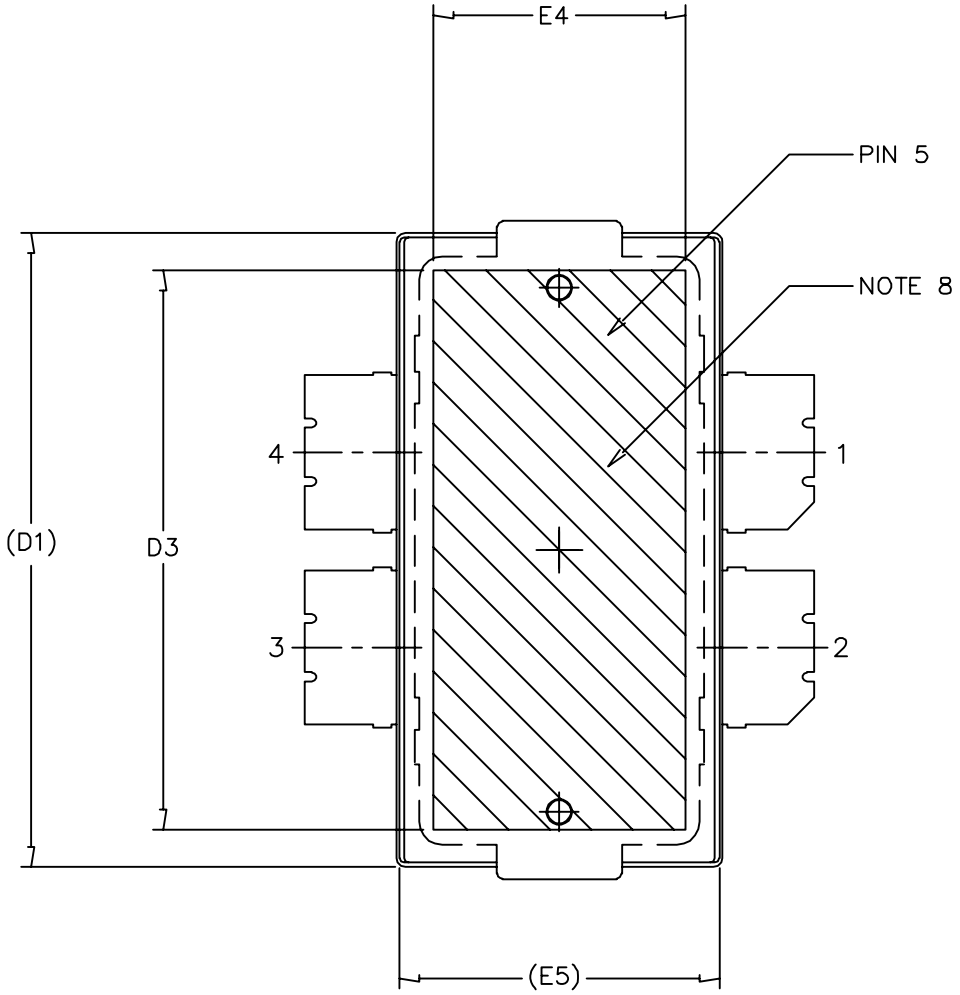

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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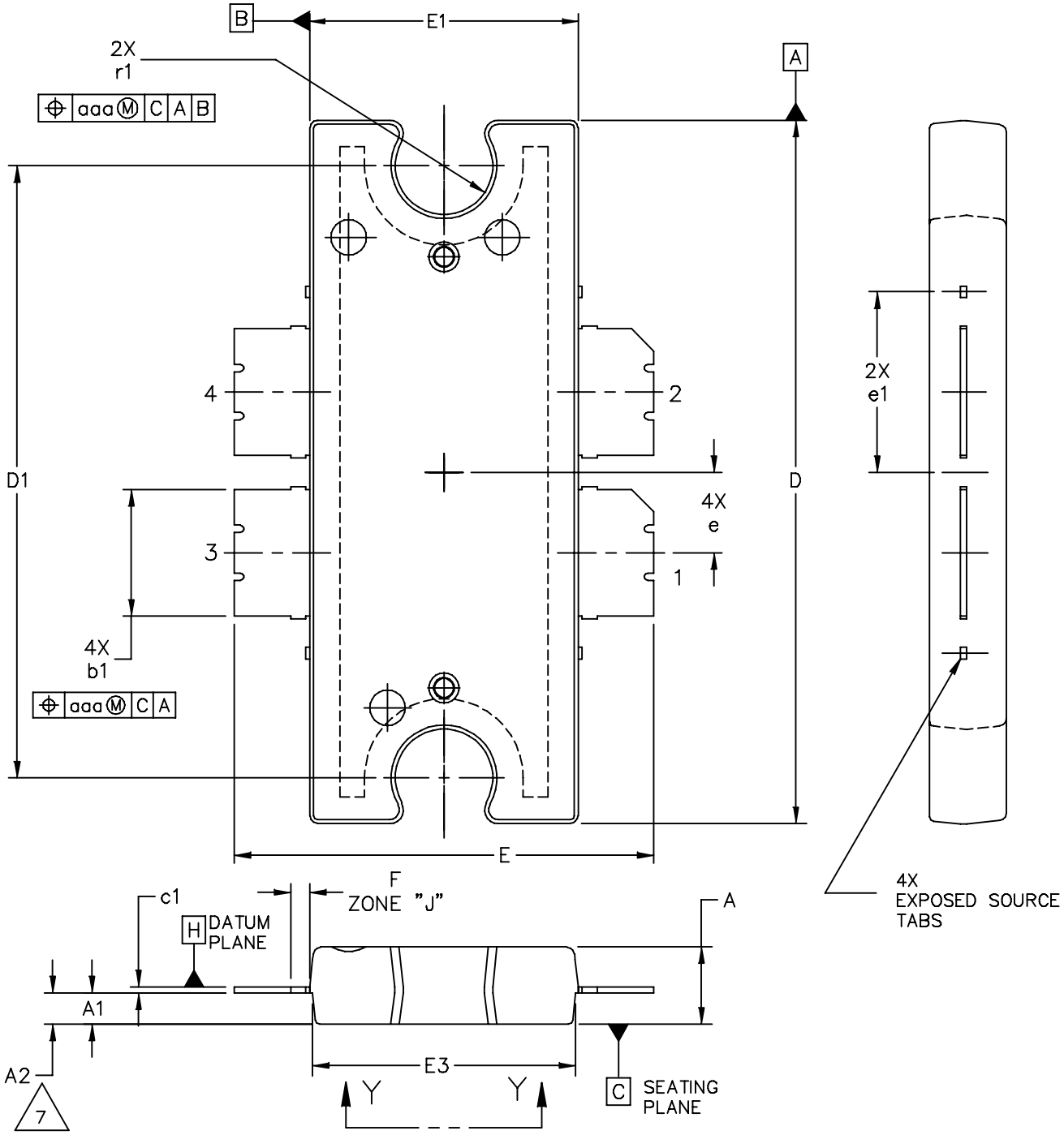

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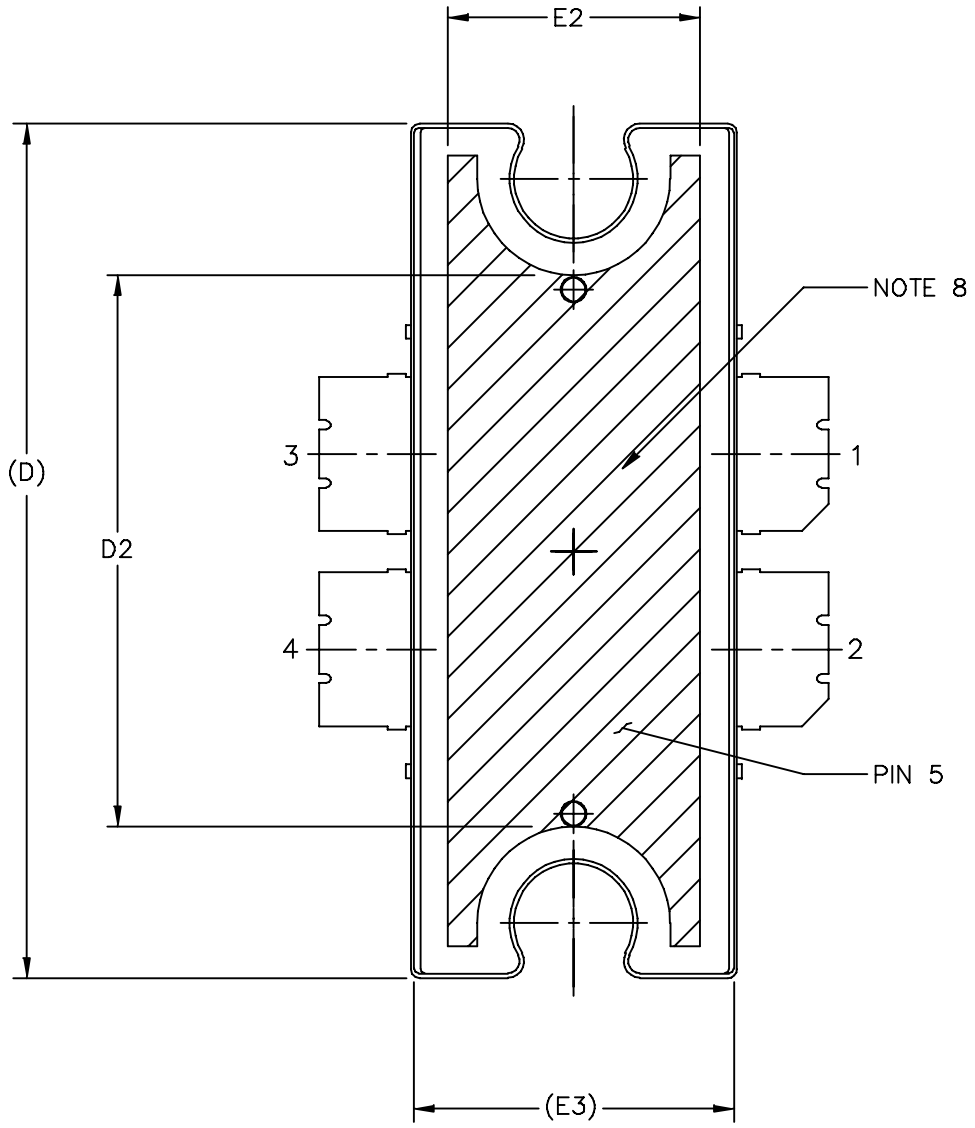

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NOTES:

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5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 − DRAIN PIN 2 − DRAIN
PIN 3 − GATE PIN 4 − GATE
PIN 5 − SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	−−−	15.24	−−−	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	−−−	6.86	−−−					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2008	• Initial Release of Data Sheet

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