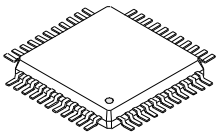
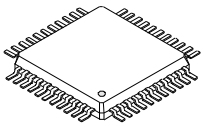
4-CHANNEL MOTOR DRIVER FOR PORTABLE CD PLAYER

DESCRIPTION

SA5901 is suitable for portable CD player with 4-ch H bridge drivers and DC/DC converter control circuit. Because of the small package QFP-44, it is most suitable for small equipment.



QFP44-10 x10-0.8



LQFP44-10 x10-0.8

FEATURES

* Four channels of H-bridge drivers are contained.
* DC/DC converter control circuit is contained.
* Reset circuit
* Reduced voltage detection circuit.
* Battery charging circuit
* General purpose operational amplifier is contained
* Low power consumption
* Thermal shutdown circuit
* QFP-44 package

<H-bridge driver>

* Load drive voltage can be processed by PWM control through an external component.
* Excellent gain can be obtained by a voltage feedback circuit.
* Mute function is disabled for ch1, ch2 and ch3/ch4 respectively.

<DC/DC converter control circuit>

* Starter and power off function
* Soft-start function and short-circuit protection function
* Self-advancing oscillation and clock synchronization are available.

<Reset circuit>

* Reset voltage is interlocked with the set voltage of DC/DC converter.
* Inversion output pin for reset output is available.

<Reduced voltage detection circuit>

* Battery charger and dry battery allow to switch “Empty” detection level.

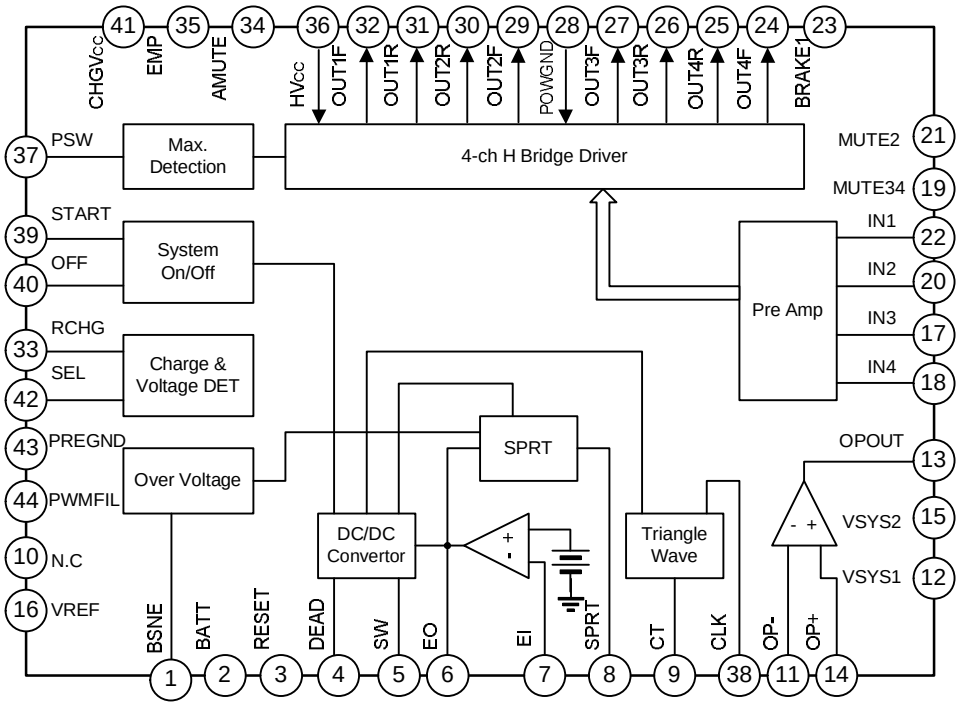
ORDERING INFORMATION

Device	Package
SA5901A	QFP44-10 X 10-0.8
SA5901L	LQFP44-10 X 10-0.8

<Battery charging circuit>

* Constant current battery charging system allows varying current value through resistance.
* It is separated from any other blocks and it can be operated independently.
* A charging power transistor is contained.
* Independent thermal shutdown circuit is contained.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C, unless otherwise specified)

Characteristic	Symbol	Ratings	Unit
Supply voltage	V_{CC}	13.5	V
Driver output current	IO	500	mA
Power dissipation	P_D	625 (note)	mW
Operating temperature range	T_{opr}	-30~85	°C
Storage temperature range	T_{stg}	-55~150	°C

Note: derating is done at 5mW/°C for operating above Tamb=25°C.

RECOMMENDED OPERATING CONDITION

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Control circuit power supply voltage	V_{SYS1}	2.7	3.2	5.5	V
Pre-driver power supply voltage	V_{SYS2}	2.7	3.2	5.5	V
H-bridge power supply voltage	HVCC	--	PWM	BATT	V
Power unit power supply voltage	BATT	1.5	2.4	8.0	V
Charging circuit power supply voltage	CHGVCC	3.0	4.5	8.0	V
Ambient temperature	T_{amb}	-10	2.5	70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified ,T_{amb}=25°C, BATT = 2.4V , V_{REF}=1.6V,V_{SYS1}=V_{SYS2}=3.2V, CHGV_{CC}=0V,f_{CLK}=88.2KHz)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
Common section								
BATT stand-by current	I_{ST}	BATT=9V, V_{SYS1}=V_{SYS2}=V_{REF}=0V	--	0	3	μA	Test circuit 1	1
BATT supply current at no-load	I_{BAT}	HV$_{CC}$=0.45V, MUTE34=3.2V	--	2.5	4.0	mA	Test circuit 1	2
VSYS1 supply current at no-load	I_{SYS1}	HV$_{CC}$=0.45V, MUTE34=3.2V, EI=0V	--	3.3	4.5	mA	Test circuit 1	3
VSYS2 supply current at no-load	I_{SYS2}	HV$_{CC}$=0.45V, MUTE34=3.2V	--	4.1	5.5	mA	Test circuit 1	4
CHGVCC supply current at no-load	ICGV$_{CC}$	CHGV$_{CC}$=4.5V, R$_{OUT}$=OPEN	--	0.65	2.0	mA	Test circuit 1	5
H-bridge driver section								
Voltage CH1,3,4 gain CH2	GVC134		12	14	16	dB	Test circuit 2	6
	GVC2		21.5	23.5	24.5	dB	Test circuit 2	6
Gain error by polarity	ΔGVC		-2	0	2	dB	Test circuit 2	7
IN pin CH1,3,4 input resistance CH2	RIN134	IN=1.7 and 1.8	9	11	13	kΩ	Test circuit 2	8
	RIN2		6	7.5	9	kΩ	Test circuit 2	8
Maximum output voltage	V_{OUT}	R_L=8Ω, HV$_{CC}$=BATT=4V, IN=0-3.2V	1.9	2.1	--	V	Test circuit 2	9
Lower transistor saturated voltage	V_{SATL}	I_O=-300mA, IN=0 and 3.2V	--	240	400	mV	Test circuit 2	10
Upper transistor saturated voltage	V_{SATU}	I_O=300mA, IN= 0 and 3.2V	--	240	400	mV	Test circuit 2	11
Input offset voltage	V_{OI}		-8	0	8	mV	Test circuit 2	12
Output CH1,3,4 offset voltage CH2	V_{OO134}	V_{REF}=IN=1.6V	-50	0	50	mV	Test circuit 2	13
	V_{OO2}		-130	0	130	mV	Test circuit 2	13
Dead zone	V_{DB}		-10	0	10	mV	Test circuit 2	14

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
BRAKE1 ON threshold voltage	V_{BRON}	IN1=1.8V	2.0	--	--	V	Test circuit 2	15
BRAKE1 OFF threshold voltage	V_{BROFF}	IN1=1.8V	--	--	0.8	V	Test circuit 2	16
MUTE2 ON threshold voltage	V_{M2ON}	IN2=1.8V	2.0	--	--	V	Test circuit 2	17
MUTE2 OFF threshold voltage	V_{M2OFF}	IN2=1.8V	--	--	0.8	V	Test circuit 2	18
MUTE34 ON threshold voltage	V_{M34ON}	IN3=IN4=1.8V	--	--	0.8	V	Test circuit 2	19
MUTE34 OFF threshold voltage	V_{M34OFF}	IN3=IN4=1.8V	2.0	--	--	V	Test circuit 2	20
VREF ON threshold voltage	V_{REFON}	IN1=IN2=IN3=IN4=1.8V	1.2	--	--	V	Test circuit 2	21
VREF OFF threshold voltage	V_{REFOFF}	IN1=IN2=IN3=IN4=1.8V	--	--	0.8	V	Test circuit 2	22
BRAKE1 break current	I_{BRAKE1}	BRAKE 1pin. The current difference between 'H' and 'L'.	4	--	10	mA	Test circuit 2	23
PWM Power supply driving section								
PSW sink current	I_{PSW}	IN1=2.1V	10	13	17	mA	Test circuit 2	24
HVCC level shift voltage	V_{SHIF}	IN1=1.8V, HVCC-OUT1F	0.35	0.45	0.55	V	Test circuit 2	25
HVCC leak current	I_{MLK}	HV_{CC}=9V, V_{SYS1}-V_{SYS2}=BATT=0V	--	0	5	μA	Test circuit 2	26
PWM amplifier transfer gain	GPWM	IN1=1.8V, HV_{CC}=1.2~1.4V	1/60	1/50	1/40	1/kΩ	Test circuit 2	27
DC/DC converter section								
Error amplifier section								
VSYS1 pin threshold	V_{SITH}		3.05	3.20	3.35	V	Test circuit 1	28
E0 pin output voltage H	V_{EOH}	EI=0.7V, I_O=-100μA	1.4	1.6	--	V	Test circuit 1	29
E0 pin output voltage L	V_{EOL}	EI=1.3V, I_O=100μA	--	--	0.3	V	Test circuit 1	30
Short-circuit protection								
SPRT pin voltage (normal)	V_{SPR}	EI=1.3V	--	0	0.1	V	Test circuit 1	31

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
SPRT pin current 1 E0=H	I_{SPR1}	EI=0.7V	6	10	16	μA	Test circuit 1	32
SPRT pin current 2 OFF=L	I_{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA	Test circuit 1	33
SPRT pin current 3 (over-voltage)	I_{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA	Test circuit 1	34
SPRT pin impedance	RSPR		175	220	265	kΩ	Test circuit 1	35
SPRT pin threshold voltage	V_{SPTH}	EI=0.7V, CT=0V	1.10	1.20	1.30	V	Test circuit 1	36
Over-voltage protection detect	V_{HVPR}	BSEN pin voltage	8.0	8.4	9.0	V	Test circuit 1	37
Transistor driving section								
SW pin output voltage 1H	VSW1H	BATT=CT=1.5V VSYS1=VSYS2=0V IO=2mA, at starter	0.78	0.98	1.13	V	Test circuit 1	38
SW pin output voltage 2H	VSW2H	CT=0V, IO=-10mA, EI=0.7V, SPRT=0V	1.0	1.50	--	V	Test circuit 1	39
SW pin output voltage 2L	VSW2L	CT=2V, IO=10mA	--	0.3	0.45	V	Test circuit 1	40
SW pin oscillating frequency 1	f_{SW1}	CT=470pF, VSYS1=VSYS2=0V, at starter	65	80	95	KHz	Test circuit 3	41
SW pin oscillating frequency 2	f_{SW2}	CT=470pF, CLK=0V	60	70	82	KHz	Test circuit 3	42
SW pin oscillating frequency 3	f_{SW3}	CT=470pF	--	88.2	--	KHz	Test circuit 3	43
SW pin minimum pulse width	TSWMIN	CT=470pF, E0=0.5→0.7V sweep	0.01	--	0.6	Usec	Test circuit 3	44
Pulse duty at start	DSW1	CT=470pF, V_{SYS1}=V_{SYS2}=0V	40	50	60	%	Test circuit 3	45
Max. pulse duty at seld-runing	DSW2	EI=0.7V, CT=470pF, CLK=0V	70	80	90	%	Test circuit 3	46
Max. pulse duty at CLK synchronization	DSW3	EI=0.7V, CT=470pF	65	75	85	%	Test circuit 3	47
Dead time section								
DEAD pin impedance	RDEAD		52	65	78	KΩ	Test circuit 1	48
DEAD pin output voltage	V_{DEAD}		0.78	0.88	0.98	V	Test circuit 1	49

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
Interface section								
OFF pin threshold voltage	V_{OFTH}	EI=1.3V	--	--	V_{SYS} 1-2.0	V	Test circuit 1	50
OFF pin bias current	I_{OFF}	OFF=0V	75	95	115	μA	Test circuit 1	51
START pin ON threshold voltage	V_{STATH1}	V_{SYS1}=V_{SYS2}=0V, CT=2V	--	--	BATT -1.0	V	Test circuit 1	52
START pin OFF threshold voltage	V_{STATH2}	V_{SYS1}=V_{SYS2}=0V, CT=2V	BAT T-0.3	--	--	V	Test circuit 1	53
START pin bias current	I_{START}	START=0V	13	16	19	μA	Test circuit 1	54
CLK pin threshold voltage H	V_{CLKTHH}		2.0	--	--	V	Test circuit 3	55
CLK pin threshold voltage L	V_{CLKTHL}		--	--	0.8	V	Test circuit 3	56
CLK pin bias current	I_{CLK}	CLK=3.2V	--	--	10	μA	Test circuit 1	57
Starter circuit section								
Starter switching voltage	V_{STNM}	V_{SYS1}=V_{SYS2}=0V→3.2V, START=0V	2.3	2.5	2.7	V	Test circuit 1	58
Starter switching hysteresis width	V_{SNHS}	START=0V	130	200	300	mV	Test circuit 1	59
Discharge release voltage	V_{DIS}		1.63	1.83	2.03	V	Test circuit 1	60
Empty detection section								
Empty detection voltage 1	V_{EMPT1}	V_{SEL}=0V	2.1	2.2	2.3	V	Test circuit 3	61
Empty detection voltage 2	V_{EMPT2}	I_{SEL}=-2μA	1.7	1.8	1.9	V	Test circuit 3	62
Empty detection hysteresis width 1	V_{EMHS1}	V_{SEL}=0V	25	50	100	mV	Test circuit 3	63
Empty detection hysteresis width 2	V_{EMHS2}	I_{SEL}=-2μA	25	50	100	mV	Test circuit 3	64
EMP pin output voltage	V_{EMP}	I_O=1mA, BSEN=1V	--	--	0.5	V	Test circuit 3	65
EMP pin output leak current	I_{EMPL}	BSEN=2.4V	--	--	1.0	μA	Test circuit 3	66
BSEN pin input resistance	RBSEN	V_{SEL}=0V	17	2.3	27	kΩ	Test circuit 3	67

(To be continued)

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Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
BSEN pin input leak current	I_{BSENL}	V_{SYS1}=V_{SYS2}=0V, BSEN=4.5V	--	--	1.0	μA	Test circuit 3	68
SEL pin detection voltage	V_{SELTH}	V_{SELTH}=BATT-SEL, BSEN=2V	1.5	--	--	V	Test circuit 3	69
SEL pin detection current	I_{SELT}		-2	--	--	μA	Test circuit 3	70
Reset circuit section								
VSYS1 reset threshold voltage ratio	HSRT	Ratio of VSYS1 voltage and error-amp threshold voltage	85	90	95	%	Test circuit 3	71
Reset detection hysteresis width	V_{RSTHS}		25	50	100	mV	Test circuit 3	72
RESET pin output voltage	V_{RST}	I_O=1mA, V_{SYS1}=V_{SYS2}=2.8V	--	--	0.5	V	Test circuit 3	73
RESET pin pull up resistance	RRST		72	90	108	kΩ	Test circuit 3	74
AMUTE pin output voltage 1	V_{AMT1}	IO=-1mA, VSYS1=VSYS2=2.8V	BATT-0.4	--	BATT	V	Test circuit 3	75
AMUTE pin output voltage 2	V_{AMT2}	IO=-1mA, V_{SYS1}=V_{SYS2}=0V, START=0V	BATT-0.4	--	BATT	V	Test circuit 3	76
AMUTE pin pull down resistance	RAMT		77	95	113	kΩ	Test circuit 3	77
Operational amplifier section								
Input bias current	I_{BIAS}		--	--	300	nA	Test circuit 1	78
Input offset voltage	V_{OIOP}		-5.5	0	5.5	mV	Test circuit 1	79
High level output voltage	V_{OHOP}	R_L=OPEN	3.0	--	--	V	Test circuit 1	80
Low level output voltage	V_{OLOP}	R_L=OPEN	--	--	0.2	V	Test circuit 1	81
Output drive current (source)	V_{SOU}	Output short to GND by 50Ω	--	-3	-1	mA	Test circuit 1	82
Output drive current (sink)	I_{SIN}	Output short to VSYS by 50Ω	0.4	0.7	--	mA	Test circuit 1	83
Open loop voltage gain	GVO	IN=-75dBV, f=1kHz	--	70	--	dB	Test circuit 1	84
Slew rate	SR		--	0.5	--	V/μsec	Test circuit 1	85

(To be continued)

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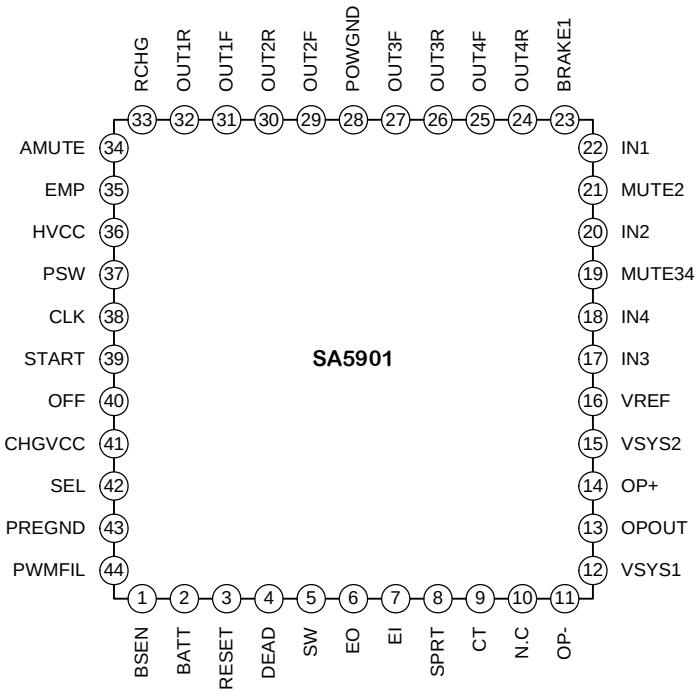
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit	Test circuit No	
Charging circuit section								
RCHG pin bias voltage	V_{RCHG}	CHGV_{CC}=4.5V, RCHG=1.8kΩ	0.71	0.81	0.91	V	Test circuit 1	86
RCHG pin output resistance	RRCHG	CHGV_{CC}=4.5V, RCHG=0.5 and 0.6V	0.75	0.95	1.20	kΩ	Test circuit 1	87
SEL pin leak current 1	I_{SELLK}	CHGV_{CC}=4.5V, RCHG=OPEN	--	--	1.0	μA	Test circuit 1	88
SEL pin leak current 2	I_{SELLK}	CHGV_{CC}=0.6V, RCHG=1.8 kΩ	--	--	1.0	μA	Test circuit 1	89
SEL pin saturated voltage	V_{SELCG}	CHGV_{CC}=4.5V, I_O=300mA, RCHG=0Ω	--	0.45	1.0	V	Test circuit 1	90

This product is not designed for protection against radioactive rays.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN No.	Symbol	Description
1	BSEN	Battery voltage monitor pin
2	BATT	Battery power supply input pin
3	RESET	Cassette detection output pin
4	DEAD	Dead-time setting pin

(To be continued)

(Continued)

PIN No.	Symbol	Description
5	SW	Booster transistor drive pin
6	EO	Error amplifier output pin
7	EI	Error amplifier input pin
8	SPRT	Short-circuit protection setting pin
9	CT	Triangular wave output pin
10	NC	Not connected
11	OP-	Operational amplifier negative input pin
12	VSYS1	Control circuit power supply input pin
13	OPOUT	Operational amplifier output pin
14	OP+	Operational amplifier positive input pin
15	VSYS2	Pre-driver power supply input pin
16	VREF	Reference power supply input pin
17	IN3	CH3 control signal input pin
18	IN4	CH4 control signal input pin
19	MUTE34	CH3/CH4 mute pin
20	IN2	CH2 control signal input pin
21	MUTE2	CH2 mute pin
22	IN1	CH1 control signal input pin
23	BRAKE1	CH1 brake pin
24	OUT4R	CH4 negative output
25	OUT4F	CH4 positive output
26	OUT3R	CH3 negative output
27	OUT3F	CH3 positive output
28	POWGND	Power unit power supply ground
29	OUT2F	CH2 positive output
30	OUT2R	CH2 negative output
31	OUT1F	CH1 positive output
32	OUT1R	CH1 negative output
33	RCHG	Charging current setting pin
34	AMUTE	Reset inversion output pin
35	EMP	‘Empty’ detection output pin
36	HVCC	h-bridge power supply input pin
37	PSW	PWM transistor drive pin
38	CLK	External clock synchronization input pin
39	START	Boost DC/DC converter starting pin
40	OFF	Boost DC/DC converter OFF pin
41	CHGVCC	Charging circuit power supply input pin
42	SEL	‘Empty’ detection level switching pin
43	PREGND	Pre-unit power supply ground pin
44	PWMFLL	PWM phase compensation pin

FUNCTION DESCRIPTION

H-bridge driver

(Gain setting)

Driver input resistance is 11kΩ (typ.) for CH1, CH3 and CH4 and 7.5 kΩ for CH2.

Calculate driver gain with the under-mentioned expression and set it.

Ch1, Ch3, Ch4	$GV=20\log\left\|\frac{55K}{11K+R}\right\|$ (dB)
Ch2	$GV=20\log\left\|\frac{110K}{7.5K+R}\right\|$ (dB)

The power supply of drive output stage is HVCC pin (36-pin) and that of pre-drive circuit is VSYS2 pin (15-pin). Attach by-pass capacitor (approximately 0.1μF) to the legs of this IC between the power supplies.

(Mute function)

Brake function and mute function are assigned to CH1 and other channels of the four channels respectively.

When BRAKE1 pin (23-pin) has been set to “H”, the output of CH1 becomes “L” for both pin 31 and pin 32, and enters a brake mode.

When MUTE2 pin (21-pin) has been set to “H”, the output of CH2 is muted.

When MUTE34 pin (19-pin) has been set to “L”, the output of CH3 and that of CH4 are muted simultaneously.

(VREF drop mute)

When the voltage impressed to VREF pin (16-pin) is 1.0V (typ.) orless, impedance of driver output becomes ‘high”.

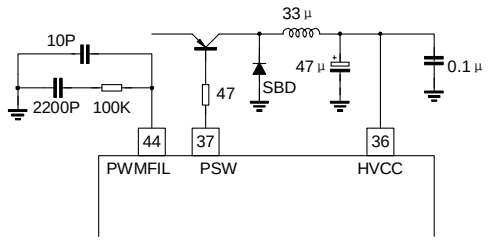
(Thermal shutdown)

When the chip temperature has been 150°C(typ.), the output current is cut.

When the chip temperature has dropped to 120°C(typ.), the output current begins to flow.

PWM power supply drive unit

This unit detects a maximum output level of drivers of four channels and performs the PWM supply of load drive power supply (36-pin). This unit uses PNP transistor, coil, schottky diode and capacitor as external component.

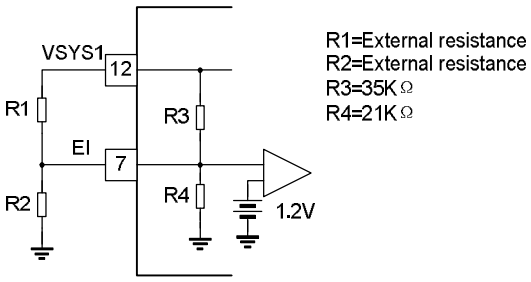


DC/DC converter

(Output voltage)

Booster circuit of 3.2V(typ.) can be configured with external components. This voltage varies depending on addition of external components. How to set the voltage is as follows:

$$VSYS1 = 1.20 \times \frac{\frac{R1 \cdot R3}{R1+R3} + \frac{R2 \cdot R4}{R2+R4}}{\frac{R2 \cdot R4}{R2+R4}} (V)$$



(Short-circuit protection function)

When the output (6-pin) of error amplifier is "H", if the voltage of SPRT pin (8-pin) has reached 1.2V (typ.) upon charging the pin, switching of SW pin (5-pin) is disabled. Time to disable switching depends on a capacitor of the SPRT pin (8-pin) and it can be calculated by the under-mentioned expression:

$$t = CSPRT \times \frac{VTH}{ISPRT} (sec) \quad (VTH = 1.20V, ISPRT = 10\mu A)$$

(Soft-start function)

The soft-start is functioned by putting a capacitor between DEAD pin (4-pin) and GND. MAX duty can be changed by attaching resistance to 4-pin.

$$t=CDEAD \times R \quad (sec) \quad (R=65k\Omega)$$

(Power-off operation)

SPRT pin (8-pin) is charged by setting OFF pin (40-pin) to "L". Then, switching of SW pin (5-pin) is terminated when the voltage of the SPRT pin (8-pin) has reached 1.2V (typ.). time to disable switching depends on a capacitor of the SPRT pin (8-pin) and it can be calculated by the under-mentioned expression:

$$t=CSPRT \times \frac{VTH}{IOFF} (sec) \quad (VTH = 1.20V, IOFF = 20uA)$$

(Over-voltage protection operation)

When the voltage impressed to BSEN pin (1-pin) has been 8.4V (typ.), SPRT pin (8-pin) is charged. Then, switching of SW pin (5-pin) is terminated when the voltage of the SPRT pin (8-pin) has reached 1.2V (typ.). time to disable switching depends on a capacitor of the SPRT pin (8-pin) and it can be calculated by the under-mentioned expression:

$$t=CSPRT \times \frac{VTH}{IHV} (sec) \quad (VTH = 1.20V, IHV = 20uA)$$

"Empty" detector unit

When the voltage impressed to BSEN pin (1-pin) has been the detecting voltage or less, EMP pin (35-pin) varies from "H" to "L" (open collector output). Hysteresis of 50mV (typ.) set to the detecting voltage to prevent the output chattering. The detecting voltage varies depending on SEL pin (42-pin) as follows:

SEL pin	Detect voltage	Return voltage
L	2.2V (Typ.)	2.25V (Typ.)
High-2	1.8V (Typ.)	1.85V (Typ.)

Reset circuit

Upon 90% (typ.) of DC/DC converter output voltage, RESET pin (3-pin) varies from "L" to "H" and AMUTE pin (34-pin) changes from "H" to "L". Hysteresis of 50mV(typ.) set to the reset voltage to prevent the output chattering.

Charging circuit

The power supply of the charging unit is CHGVCC pin (41-pin) and it is independent of any other circuit. Charging current is set by the resistance between RCHG pin (33-pin) and GND. The charging current takes constant current through SEL pin (42-pin).

This circuit has a private thermal shutdown circuit. When the chip temperature has been 150°C (typ.), the charging current is cut. When the chip temperature has dropped to 120°C(typ.), the charging current begins to flow.

TEST CIRCUIT (1)

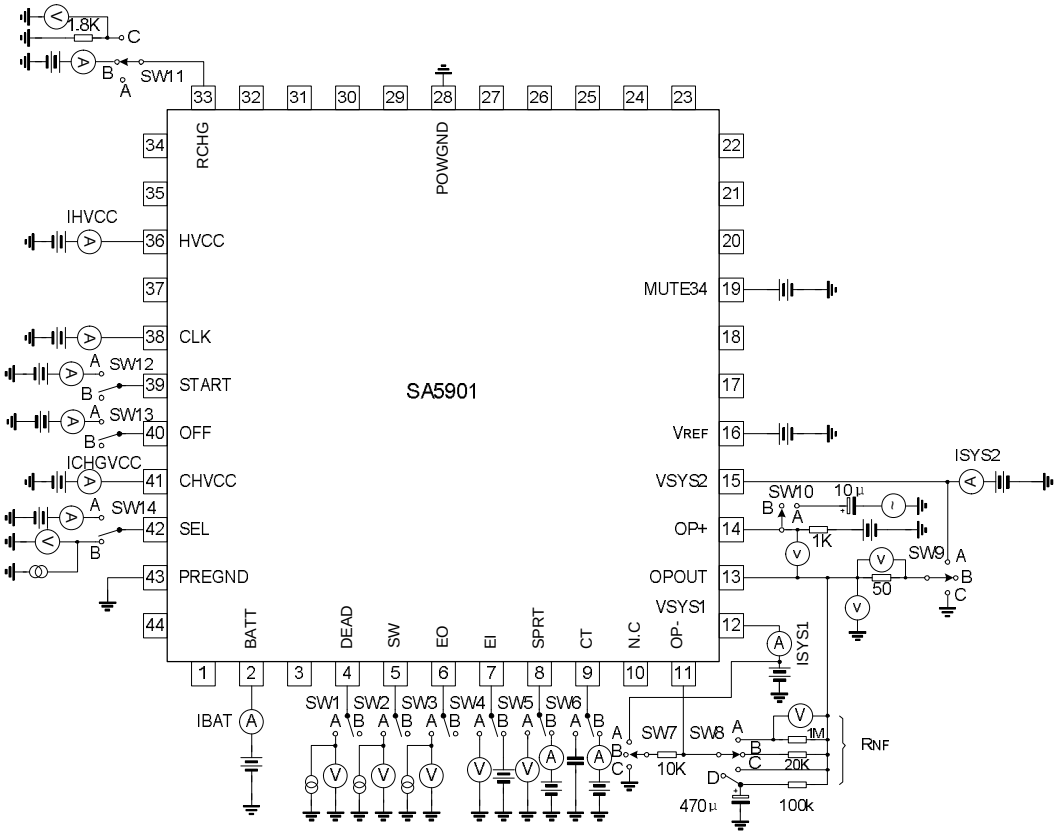


Table of test circuit 1 switches position

Measuring no.	SW no													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	--	--	--	--	--	--	--	--	--	--	--	--	--	--
2	--	--	--	--	--	--	--	--	--	--	--	--	--	--
3	--	--	--	B	--	--	--	B	--	--	--	--	--	--
4	--	--	--	B	--	--	--	B	--	--	--	--	--	--
5	--	--	--	--	--	--	--	--	--	--	A	--	--	--
28	--	--	A	--	--	--	--	--	--	--	--	--	--	--
29	--	--	A	B	--	--	--	--	--	--	--		--	--
30	--	--	A	B	--	--	--	--	--	--	--	--	--	--

(To be continued)

(Continued)

Measuring	SW no													
no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
31	--	--	--	B	--	--	--	--	--	--	--	--	--	--
32	--	--	--	B	--	--	--	--	--	--	--	--	--	--
33	--	--	--	B	--	--	--	--	--	--	--	--	A	--
34	--	--	--	B	--	--	--	--	--	--	--	--	--	--
35	--	--	--	--	B	--	--	--	--	--	--	--	--	--
36	--	--	--	B	B	--	--	--	--	--	--	--	--	--
37	--	--	--	--	--	--	--	--	--	--	--	--	--	--
38	--	A	--	--	--	B	--	--	--	--	--	A	--	--
39	--	A	--	B	B	B	--	--	--	--	--	--	--	--
40	--	A	--	--	--	B	--	--	--	--	--	--	--	--
48	A	--	--	--	--	--	--	--	--	--	--	--	--	--
49	A	--	--	--	--	--	--	--	--	--	--	--	--	--
50	--	--	--	--	A	--	--	--	--	--	--	--	A	--
51	--	--	--	--	--	--	--	--	--	--	--	--	A	--
52	--	A	--	--	--	--	--	--	--	--	--	A	--	--
53	--	A	--	--	--	--	--	--	--	--	--	A	--	--
54	--	--	--	--	--	--	--	--	--	--	--	A	--	--
57	--	--	--	--	--	--	--	--	--	--	--	--	--	--
58	--	A	--	--	--	--	--	--	--	--	--	A	--	--
59	--	A	--	--	--	--	--	--	--	--	--	A	--	--
60	A	--	--	--	--	--	--	--	--	--	--	--	--	--
78	--	--	--	--	--	--	B	A	B	--	--	--	--	--
79	--	--	--	--	--	--	B	C	B	--	--	--	--	--
80	--	--	--	--	--	--	C	B	B	--	--	--	--	--
81	--	--	--	--	--	--	A	B	B	--	--	--	--	--
82	--	--	--	--	--	--	B	C	C	--	--	--	--	--
83	--	--	--	--	--	--	B	C	A	--	--	--	--	--
84	--	--	--	--	--	--	B	D	B	A	--	--	--	--
85	--	--	--	--	--	--	B	C	B	A	--	--	--	--
86	--	--	--	--	--	--	--	--	--	--	C	--	--	--
87	--	--	--	--	--	--	--	--	--	--	B	--	--	--
88	--	--	--	--	--	--	--	--	--	--	A	--	--	A
89	--	--	--	--	--	--	--	--	--	--	C	--	--	A
90	--	--	--	--	--	--	--	--	--	--	B	--	--	B

--: Switch open.

Supplementary explanation of test circuit 1.

No. 1 Measure IBAT.

No. 2 Measure IBAT

No.3 Measure ISYS1

No.4 Measure ISYS2

No.5 Measure ICHGVCC.

No. 28 VSYS1 voltage when E0 pin varies from “H” to “L” upon increasing VSYS1.

No. 29 E0 pin voltage when 100μA has been taken from the E0 pin.

No. 30 E0 pin voltage when 100μA has flowed into the E0 pin

No. 31, 32, 33 &34 measure SPRT pin voltage

No. 35 Current flowing when 0.5V has been impressed to SPRT terminal shall be I1, and current flowing when 0.6V has been impressed shall be I2.

$$RSPR=\frac{0.1V}{I2-I1}(\Omega)$$

No. 36 SPRT pin voltage when SW pin varies from “H” to “L” upon increasing the SPRT voltage.

No. 37 BSEN pin voltage when SPRT pin varies form “L” to “H” upon increasing BSEN voltage and BATT voltage.

No. 38 SW pin voltage when 2mA has been taken from the SW pin. (START=0V)

No. 39 SW pin voltage when 10mA has been taken from the SW pin. (CT=SPRT=0V, EI=0.7V)

No. 40 SW pin voltage when 10mA has flowed into the SW pin. (CT=2V)

No. 48 DEAD pin voltage when 2μA has been taken from the DEAD pin shall be DEAD1, and DEAD pin voltage when 4μA has been taken shall be DEAD2.

$$RDEAD=\frac{DEAD1-DEAD1}{2\mu A}\ (\Omega)$$

No. 49 DEAD pin voltage upon IDEAD=0μA.

No. 50 OFF pin voltage when SPRT pin varies from “L” to “H” upon decreasing the OFF pin.

No. 51 OFF pin outgoing current upon OFF=0V.

No. 52 START pin voltage when SW pin varies from “L” to “H” upon decreasing the START pin.

No. 53 SW pin shall be “L” when voltage of BATT-0.5V has been impressed to START pin.

No. 54 START pin outgoing current upon START=0V

No. 57 CLK pin incoming current upon CLK=3.2V

No. 58 & 59 VSYS1 voltage when SW pin varies from “L” to “H” upon increasing VSYS1 voltage. The voltage width until SW pin varies “H” to “L” upon decreasing VSYS1 from that voltage shall be hysteresis width.

No. 60 VSYS1 voltage when dead pin varies from “L” to “H” upon increasing VSYS1 voltage.

No. 78 Calculated from voltage at both ends of RNF=1MΩ.

No. 79 Voltage between OP- and OP+ of RNF=0Ω.

No. 80 &81 DC voltage at OPOUT pin in inversion amplifier configuration of RNF=20kΩ.

No. 82 Calculated voltage at both ends of 50Ω when short-circuiting OPOUT pin to GND, grounding , with 50Ω at RNF=0Ω.

No. 83 Calculated voltage at both ends of 50Ω when short-circuiting OPOUT pin to VSYS2, high voltage, with 50Ω at RNF=0Ω.

No. 85

No. 86 Measure RCHG pin voltage when 1.8kΩ has been impressed to RCHG pin and GND.

No. 87 Current flowing from this pin when 0.5V has been impressed to RCHG pin shall be IRC1, and current when 0.6V has been impressed shall be IRC2.

$$RRCHG=\frac{0.1V}{IRC2-IRC1}(\Omega)$$

No. 88 & 89 Measure leak current of SEL pin.

No. 90 Measure SEL pin voltage when 300mA has been flowed into the SEL pin.

TEST CIRCUIT (2)

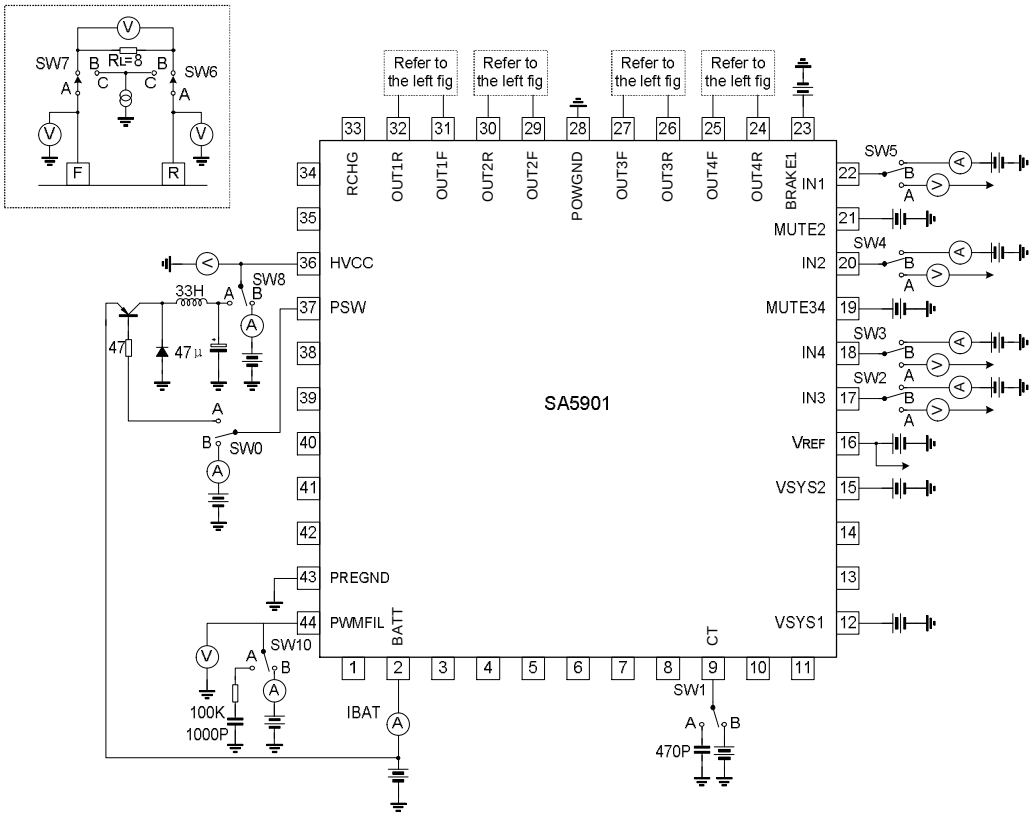


Table 1/2 of test circuit 2 switches position

Measuring no.		SW no									
		1	2	3	4	5	6	7	8	9	10
6	CH1F,R	--	--	--	--	B	B	B	B	--	--
	CH2F,R	--	--	--	B	--	B	B	B	--	--
	CH3F,R	--	B	--	--	--	B	B	B	--	--
	CH4F,R	--	--	B	--	--	B	B	B	--	--
7	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
	Ch3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
8	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
9	CH1F,R	--	--	--	--	B	B	B	B	--	--
	CH2F,R	--	--	--	B	--	B	B	B	--	--
	CH3F,R	--	B	--	--	--	B	B	B	--	--
	CH4F,R	--	--	B	--	--	B	B	B	--	--

(To be continued)

(Continued)

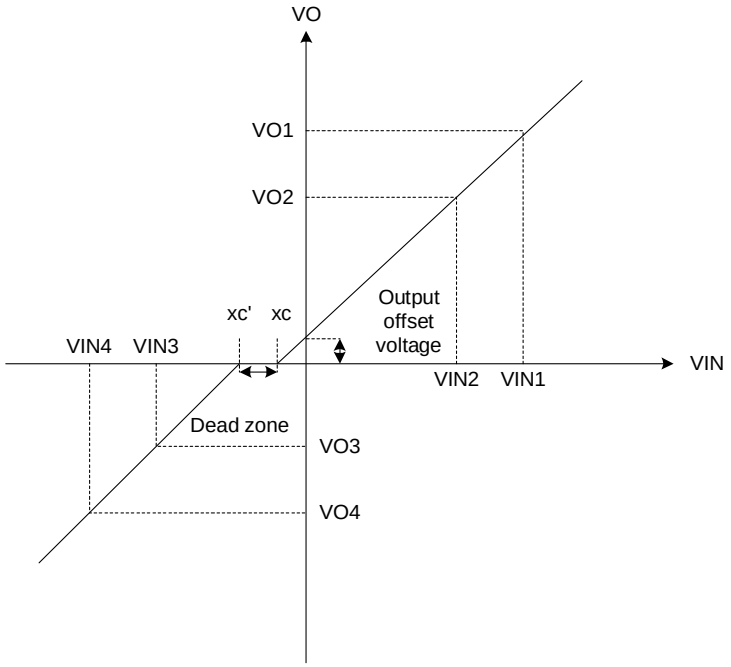
Measuring no.		SW no									
		1	2	3	4	5	6	7	8	9	10
10	CH1F	--	--	--	--	B	C	A	B	--	--
	CH1R	--	--	--	--	B	A	C	B	--	--
	CH2F	--	--	--	B	--	C	A	B	--	--
	CH2R	--	--	--	B	--	A	C	B	--	--
	CH3F	--	B	--	--	--	C	A	B	--	--
	CH3R	--	B	--	--	--	A	C	B	--	--
	CH4F	--	--	B	--	--	C	A	B	--	--
	CH4R	--	--	B	--	--	A	C	B	--	--
11	CH1F	--	--	--	--	B	C	A	B	--	--
	CH1R	--	--	--	--	B	A	C	B	--	--
	CH2F	--	--	--	B	--	C	A	B	--	--
	CH2R	--	--	--	B	--	A	C	B	--	--
	CH3F	--	B	--	--	--	C	A	B	--	--
	CH3R	--	B	--	--	--	A	C	B	--	--
	CH4F	--	--	B	--	--	C	A	B	--	--
	CH4R	--	--	B	--	--	A	C	B	--	--
12	CH1	--	--	--	--	A	--	--	--	--	--
	CH2	--	--	--	A	--	--	--	--	--	--
	CH3	--	A	--	--	--	--	--	--	--	--
	CH4	--	--	A	--	--	--	--	--	--	--
13	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
14	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
14	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
15	CH1	--	--	--	--	B	B	B	B	--	--
16	CH1	--	--	--	--	B	B	B	B	--	--
17	Ch2	--	--	--	B	--	B	B	B	--	--
18	CH2	--	--	--	B	--	B	B	B	--	--
19	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
20	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--

(To be continued)

(Continued)

Measuring no.		SW no									
		1	2	3	4	5	6	7	8	9	10
21	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
22	CH1	--	--	--	--	B	B	B	B	--	--
	CH2	--	--	--	B	--	B	B	B	--	--
	CH3	--	B	--	--	--	B	B	B	--	--
	CH4	--	--	B	--	--	B	B	B	--	--
23	CH1	--	--	--	--	B	B	B	B	--	--
24		--	--	--	--	B	--	--	B	B	--
25		--	--	--	--	B	B	B	A	A	A
26		--	--	--	--	--	B	B	B	--	--
27		A	--	--	--	B	B	B	B	--	B

--: Switch open



Voltage gain

$$GVC(+)=20\log\left|\frac{V01-V02}{VIN1-VIN2}\right|$$

$$GVC(-)=20\log\left|\frac{V03-V04}{VIN3-VIN4}\right|$$

Gain error by polarity

GVC(+)-GVC(-)

Dead zone

$$xc\text{-}xc'=\frac{VIN2\cdot V01-VIN1\cdot V02}{V01-V02}-\frac{VIN3\cdot V04-VIN4\cdot V03}{V03-V04}$$

Supplementary explanation of test circuit 2

No.6 Input conditions

CH1, 3&4 (VIN1=VREF+0.15V) CH2 only (VIN1=VREF+0.10V)

(VIN2=VREF+0.15V) (VIN2=VREF+0.05V)

(VIN3=VREF-0.15V) (VIN3=VREF-0.10V)

(VIN4=VREF-0.15V) (VIN4=VREF-0.05V)

No. 7 GVC(+)-GVC(-)

No. 8 Current flowing when 1.7V has been impressed each driver shall be IRIN1, and current flowing when 1.8V has been impressed shall be IRIN2.

No.9 Measure voltage between output F and output R of each driver upon RL=8Ω. (HVCC=BATT=4V)

No. 10 Voltage between each output F and GND when 300mA has been flowed into a lower power transistor. (HVCC=BATT=2V)

No. 11 Voltage between each output and HVCC when 300mA has been taken from an upper power transistor. (HVCC=BATT=2V)

No. 12 Measure voltage between each driver input pin and VREF pin.

No. 13 Measure voltage between output F and output R of driver upon short-circuiting between each driver input pin and VREF pin. (RL=8Ω).

No. 14 Measure at input conditions of (VIN1=VREF+50mV)

(VIN2=VREF+30mV)

(VIN3=VREF-50mV)

(VIN4=VREF-30mV)

No. 15 Output of CH1 shall be 0 when 2.0V has been impressed to BRAKE1 pin.

No. 16 Output of CH1 shall be observed completely when 0.8V has been impressed to BRAKE1 pin.

No. 17 Output of CH2 shall be 0 when 2.0V has been impressed to MUTE2 pin.

No. 18 Output of CH2 shall be observed completely when 0.8V has been impressed to MUTE2

No. 19 Output of CH3 &CH4 shall be 0 when 0.8V has been impressed to MUTE34 pin.

No. 20. Output of CH3 &CH4 shall be observed completely when 2.0V has been impressed to MUTE34 pin.

No. 21 Each output of driver shall be observed completely when 1.2V has been impressed to VREF pin.

No. 22 Each output of driver shall be 0 when 0.8V has been impressed to VREF pin.

No. 23 Measure the difference between IBAT upon BRAKE=0V and IBAT upon BRAKE1=3.2V.

No. 24 Measure current flowing into PSW pin.

No. 25 Difference between OUT1F pin voltage and HVCC pin voltage generated by a switching regulator.

No. 26 Measure leak current of HVCC pin.

No. 27 When approximately 1V is observed in driver output (OUT1F pin) (VIN1=VREF+0.2V), PWMFIL pin current upon HVCC=1.2V shall be IPWM1 and the current upon HVCC=1.4V shall be IPWM2. (Measure PWMFIL pin at 0.7V.)

$$GPWM = \frac{IPWM1 - IPWM2}{0.2V}(1/K\Omega)$$

TEST CIRCUIT (3)

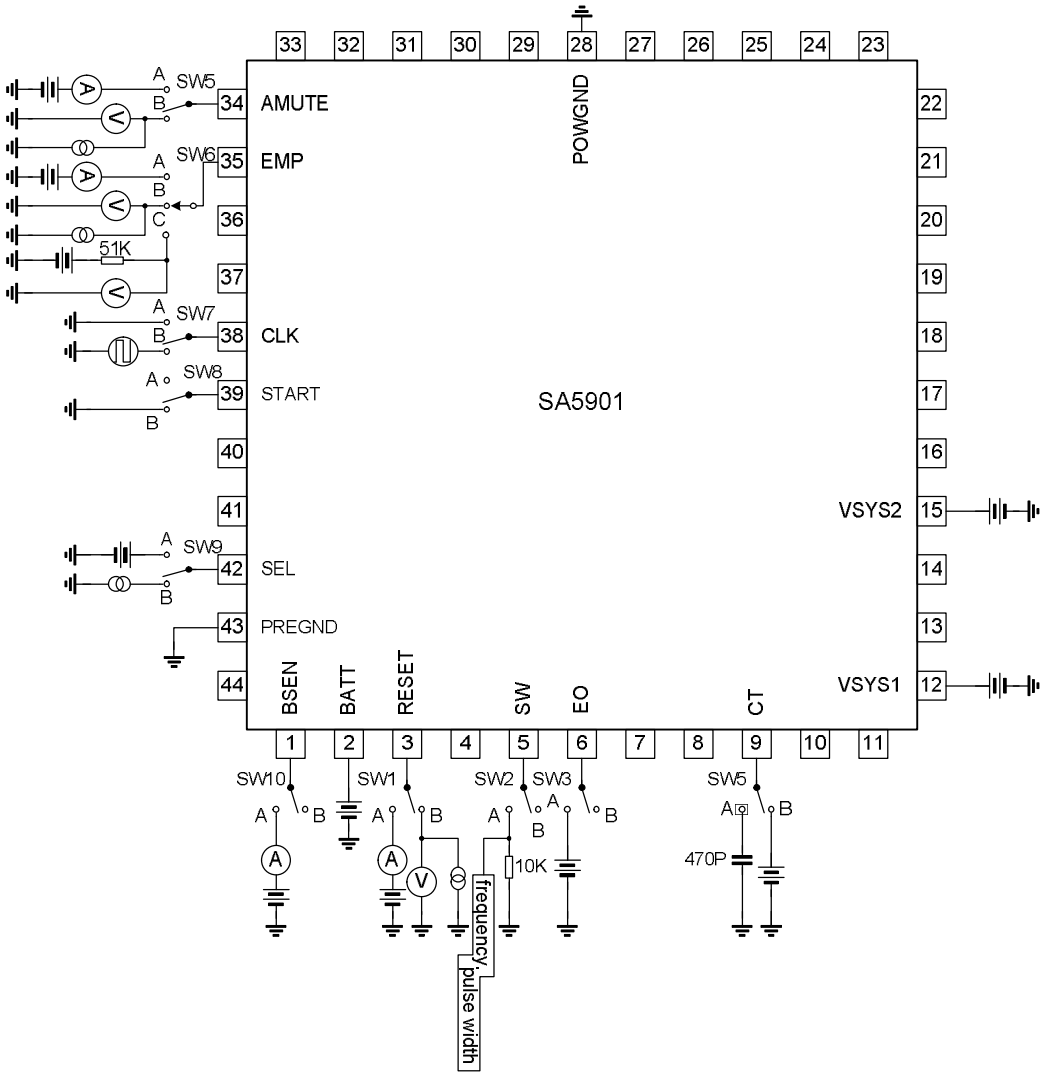


Table of test circuit 3 switches position

Measuring No.	SW No									
	1	2	3	4	5	6	7	8	9	10
41	--	A	--	A	--	--	A	B	--	--
42	--	A	--	A	--	--	A	A	--	--
43	--	A	--	A	--	--	B	A	--	--
55	--	A	--	A	--	--	B	A	--	--
56	--	A	--	A	--	--	B	A	--	--
44	--	A	A	A	--	--	B	A	--	--
45	--	A	--	A	--	--	A	B	--	--
46	--	A	--	A	--	--	A	A	--	--

(To be continued)

(Continued)

Measuring No.	SW No									
	1	2	3	4	5	6	7	8	9	10
47	--	A	--	A	--	--	B	A	--	--
61	--	--	--	--	--	C	--	--	A	A
62	--	--	--	--	--	C	--	--	B	A
63	--	--	--	--	--	C	--	--	A	A
64	--	--	--	--	--	C	--	--	B	A
65	--	--	--	--	--	B	--	--	--	A
66	--	--	--	--	--	A	--	--	--	A
67	--	--	--	--	--	--	--	--	A	A
68	--	--	--	--	--	--	--	--	--	A
69	--	--	--	--	--	C	--	--	A	A
70	--	--	--	--	--	C	--	--	B	A
71	B	--	--	--	B	--	--	--	--	--
72	B	--	--	--	B	--	--	--	--	--
73	A	--	--	--	B	--	--	--	--	--
74	B	--	--	--	B	--	--	--	--	--
75	B	--	--	--	B	--	--	--	--	--
76	B	--	--	--	B	--	--	B	--	--
77	B	--	--	--	A	--	--	--	--	--

--: Switch open

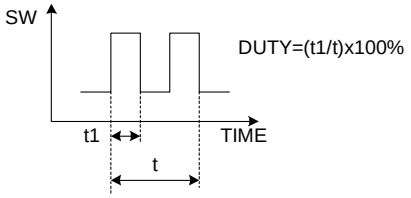
Supplementary explanation of test circuit

No. 41 Measure SW pin oscillation frequency upon VSYS1=0V and VSTART=0V.

No. 42 Measure SW pin oscillation frequency upon VSYS1=3.2V.

No. 43 Measure SW pin oscillation frequency when pulse wave of 88.2kHz has been inputted to CLK pin.

No. 44 Measure minimum pulse width outputted to SW pin upon increasing E0 pin voltage from 0.5V.



No. 45 Measure SW pin pulse duty upon VSYS1=0V and VSTART=0V.

No. 46 Measure SW pin pulse duty upon VSYS1=3.2V and CLK=0V.

No. 47 Measure SW pin pulse duty upon VSYS1=3.2V and CLK=88.2kHz.

No. 55 &56 Check the synchronization of SW pin when low level of pulse wave inputted to CLK pin has been 0.8V and high level has been 2.0V.

No. 61 &63 BSEN pin voltage when EMP pin varies from “H” to “L” upon decreasing the BSEN pin voltage (VSEL=0V).

The voltage width until EMP pin varies “L” to “H” upon increasing BSEN pin voltage from that voltage shall be hysteresis width.

No. 62 &64 BSEN pin voltage when EMP pin varies from “H” to “L” upon decreasing the BSEN pin voltage

(ISEL=-2μA).

The voltage width until EMP pin varies “L” to “H” upon increasing BSEN pin voltage from that voltage shall be hysteresis width.

No. 65 EMP pin voltage when 1mA has flowed into the EMP pin.

No. 66 Measure leak current of EMP pin.

No. 67 Current flowing into the BSEN pin when 2.4V has been impressed to this pin shall be IBSEN.

$$RBSEN = \frac{2.4V}{IBSEN}(\Omega)$$

No. 68 Measure leak current of BSEN pin. (VSYS1=0V)

No. 69 When 1.5V has been impressed between SEL pin and BATT pin, SEL pin shall judge it as “L”.

No. 70 When 2μA has been taken from SEL pin, SEL pin shall judge it as “Hi-z”.

No. 71 Ratio of VSYS1 voltage and error amplifier threshold voltage when RESET pin varies from “L” to “H” upon increasing VSYS1 voltage.

No. 72 Measure VSYS1 voltage when RESET pin varies from “L” to “H” upon increasing VSYS1 voltage, voltage width from VSYS1 until RESET pin varies from “H” to “L” upon decreasing VSYS1 voltage.

$$RRST = \frac{1.0V}{IRESET}(\Omega)$$

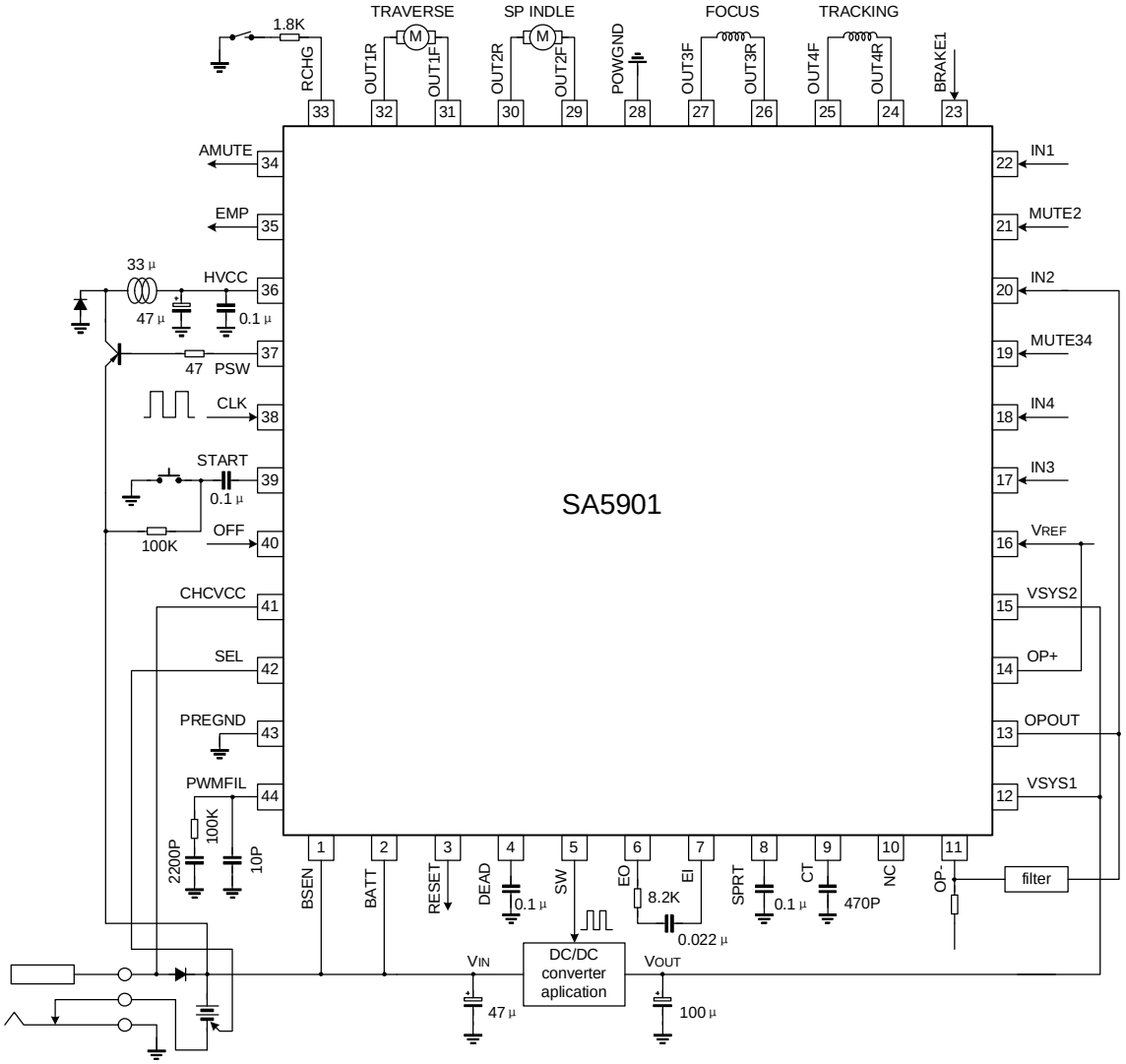
No. 75 AMUTE pin voltage when 1mA has been taken from the AMUTE pin.

No. 76 AMUTE pin voltage when 1mA has been taken from the AMUTE pin upon VSYS1=0V and VSTART=0V.

No. 77 Current flowing into AMUTE pin when 1.0V has been impressed to AMUTE pin shall be IAMUTE.

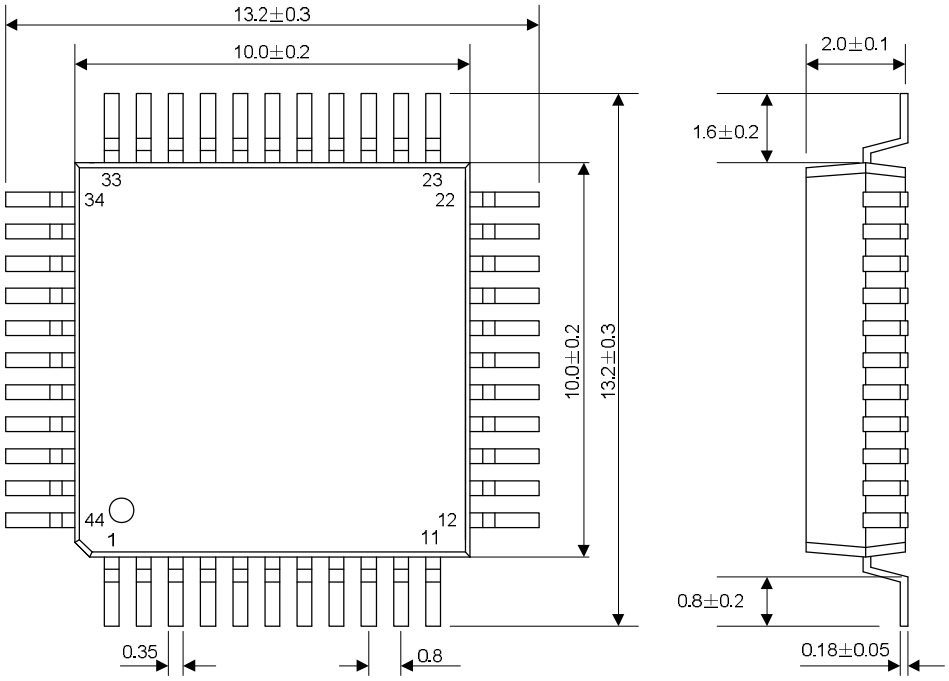
$$RAMUTE = \frac{1.0V}{IAMUTE}(\Omega)$$

TYPICAL APPLICATION CIRCUIT

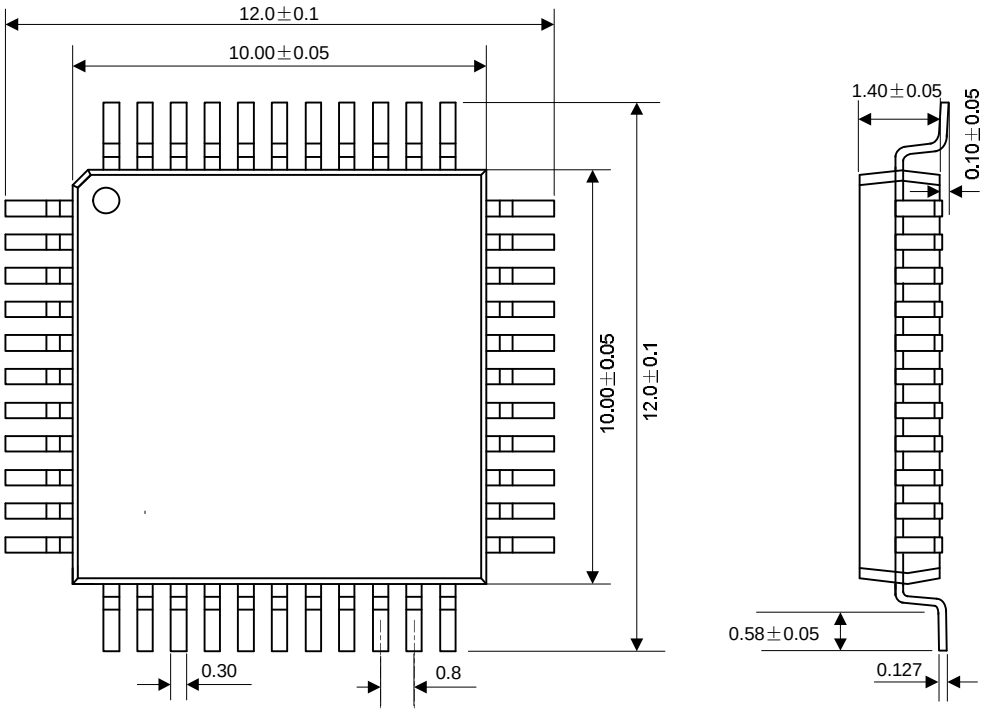


PACKAGE OUTLINE

QFP-44-10x10-0.8 UNIT: mm



LQFP-44-10x10-0.8 UNIT: mm



ATTACHMENT

Revision History

Data	REV	Description	Page
2003.04.08	1.0	Original	
2004.03.09	1.1	Add “QFP-44-10X10-0.8”	
2004.04.08	1.2	Modify the “TEST CIRCUIT(2)”	19
2006.02.27	1.3	Modify the package of “QFP-44-10X10-0.8” Add the package of “LQFP-44-10X10-0.8”	