

Silicon PNP Power Transistors

2SB1315

DESCRIPTION

- With TO-3PML package
- Low collector saturation voltage

APPLICATIONS

- For use in low frequency power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

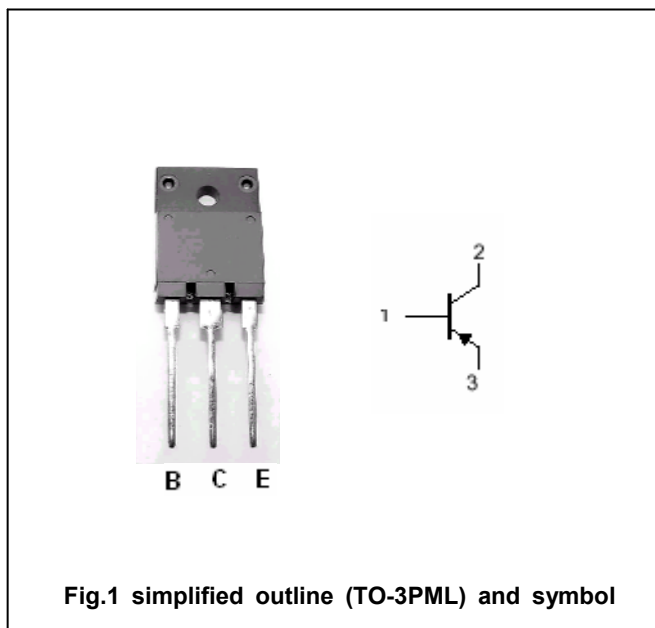


Fig.1 simplified outline (TO-3PML) and symbol

Absolute maximum ratings (Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-120	V
V _{CEO}	Collector-emitter voltage	Open base	-120	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-8	A
P _C	Collector dissipation	T _a =25°C	3.5	W
		T _C =25°C	65	
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-50mA ; I _B =0	-120			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA ; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A ; I _B =-0.5A			-1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A ; I _B =-0.5A			-2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-120V; I _E =0			-50	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-50	μA
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-5V	60		320	
f _T	Transition frequency	I _C =-1A ; V _{CE} =-5V		65		MHz
C _{OB}	Collector output capacitance	f=1MHz; V _{CB} =-10V		200		pF

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PACKAGE OUTLINE

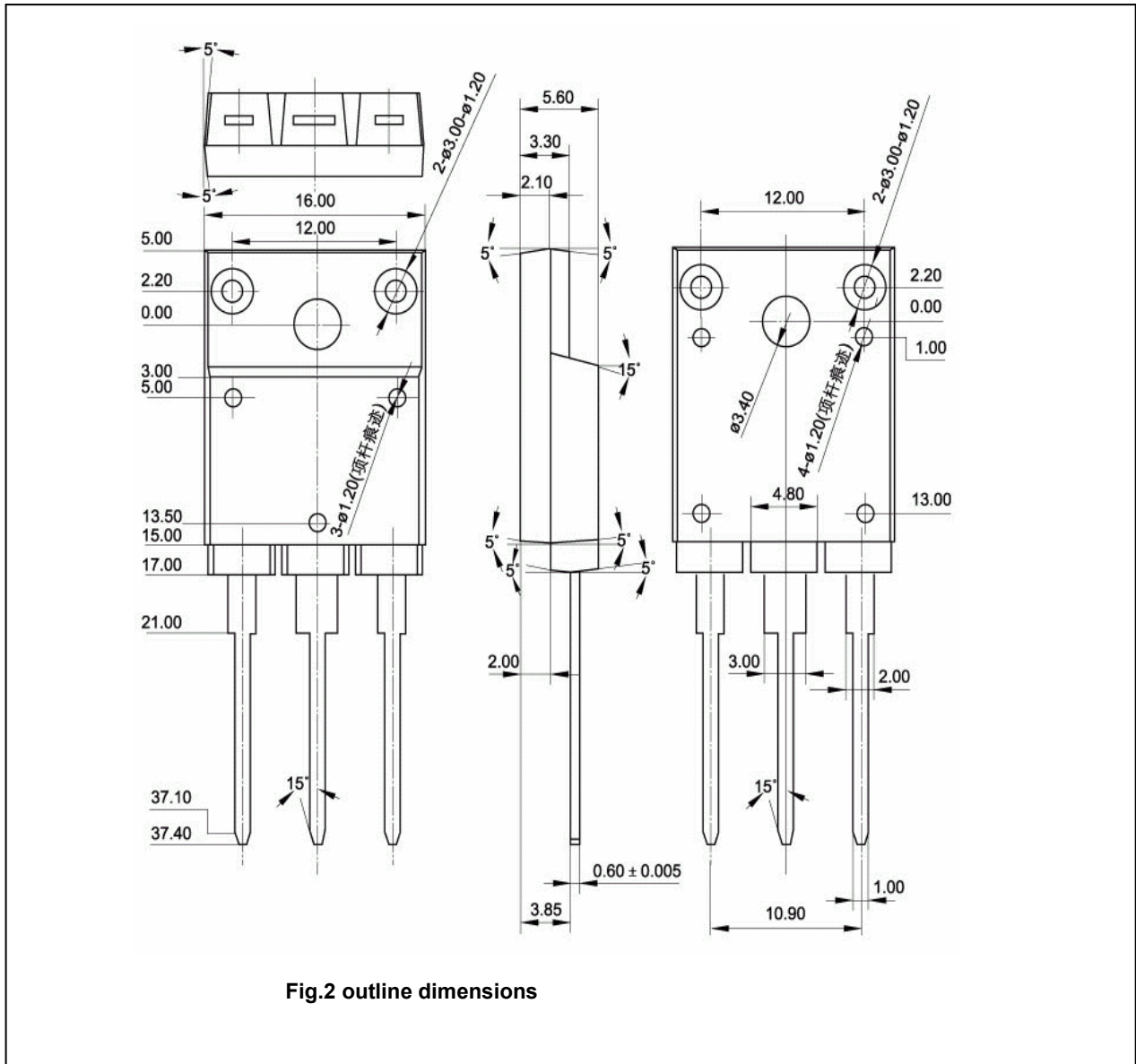


Fig.2 outline dimensions